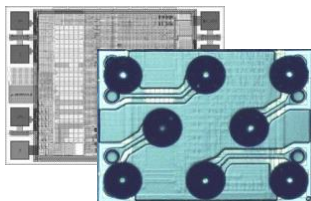


# MS8883C

Capacitive switch with auto-calibration, large voltage operating range and very low power consumption



## 1 General Description

The integrated circuit MS8883C is a capacitive switch that uses a patented (EDISEN) digital method to detect a change in capacitance on a remote sensing plate.

Changes in the static capacitance (as opposed to dynamic capacitance changes) are automatically compensated using continuous auto-calibration. Remote sensing plates (e.g. conductive foil) can be connected remotely to the IC using coaxial cable.

## 2 Applications

- Hermetically sealed keys on a keyboard
- Switch for medical applications
- Switch for use in explosive environments
- Vandal proof switches
- Automotive: Switches in or under upholstery, leather, handles, mats and glass
- Portable entertainment units
- Buildings: Switch in or under carpets, glass or tiles
- Sanitary applications:  
Use of standard metal sanitary parts (e.g. tap) as switch

## 3 Typical application

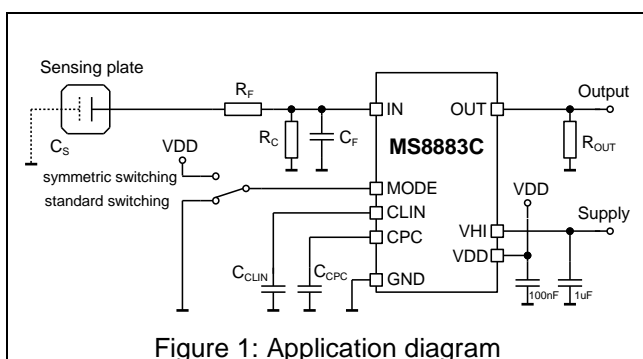


Figure 1: Application diagram

## 4 Features

- Dynamic proximity switch
- Digital processing method
- Automatic calibration
- Sensing plates can be connected remotely
- Open-drain output (P-type MOSFET, external load between pin and ground)
- Designed for battery powered applications ( $I_{HI}$  typ.  $3\mu A$ )
- Adjustable response time
- Adjustable sensitivity
- Configurable switching dynamics
- Large voltage operating range ( $V_{HI} = 2.7$  to  $9V$ )
- Large temperature operating range ( $T_{amb} = -40$  to  $85^\circ C$ )
- Internal voltage regulator
- Available in 3x3mm DFN8 (other packages available for larger quantities)

## 5 Pinout

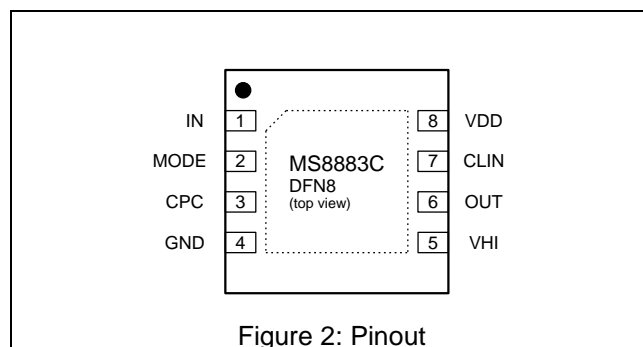


Figure 2: Pinout

## 6 Ordering Information

Table 1: Ordering information

Typ	Package	Shipping	Article No.
MS8883C	DFN8 3x3mm	Tape&Reel	9160178

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## 7 Pin description

Table 2: Pin description

Pin	Symbol	I/O <sup>1</sup>	Description
1	IN	I	Sensor-Input
2	MODE	I	Switching behaviour definition
3	CPC	A	Reservoir capacitor
4	GND	S	Negative supply
5	VHI	S	Positive supply
6	OUT	O	Switch output
7	CLIN	A	Oscillator capacitor
8	VDD	S	Internal supply

## 8 Description

### 8.1 Basic functionality

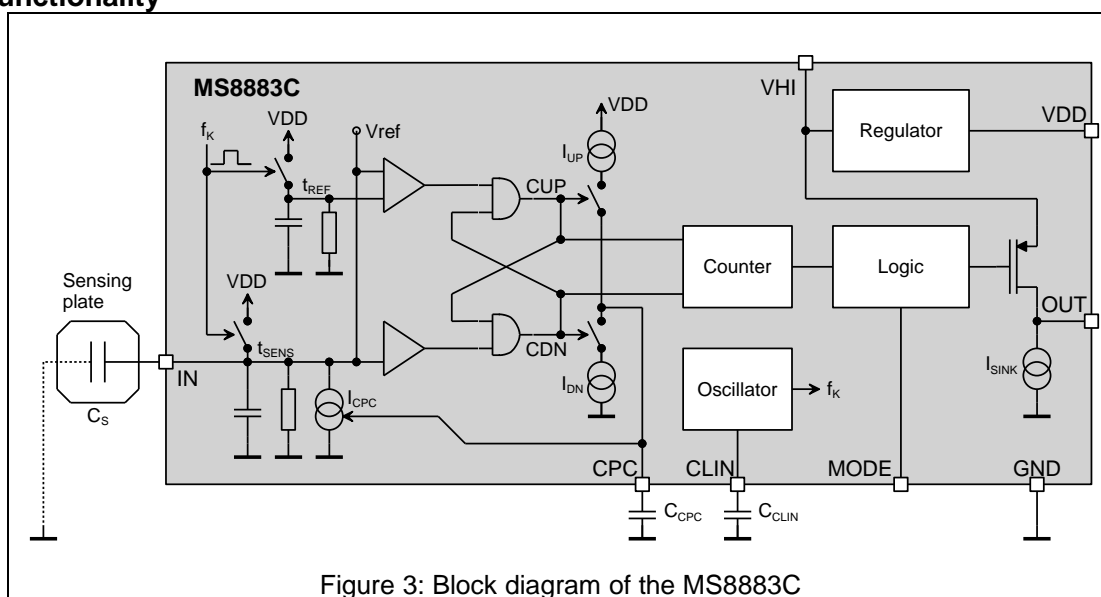


Figure 3: Block diagram of the MS8883C

Figure 3 illustrates the functional principle of the MS8883C

The discharge time  $t_{\text{SENS}}$  on input IN attached to the sensing plate capacitance is compared to the discharge time  $t_{\text{REF}}$  of an internal RC timing element. Both RC timing circuits are periodically charged to  $V_{\text{DD}}$  via MOS switches and then discharged via a resistor to ground (GND).

The charge discharge cycle is governed by the sampling rate ( $f_k$ ). When the voltage of an RC combination falls below the  $V_{\text{REF}}$  level, the appropriate comparator output will change. The logic following the comparators determines which comparator switched first. If the upper (reference) comparator switches, then a pulse is given on CUP. If the lower (input) comparator switches first then a pulse is given on CDN (see Figure 2).

The pulses control the charge on the external capacitor  $C_{\text{CPC}}$  on pin CPC. Every time a pulse is given on CUP, capacitor  $C_{\text{CPC}}$  is charged through a current source  $I_{\text{UP}}$  from  $V_{\text{DD}}$  for a fixed time causing the voltage on  $C_{\text{CPC}}$  to rise by a small increment. Likewise when a pulse occurs on CDN, capacitor  $C_{\text{CPC}}$  is discharged through a current sink  $I_{\text{DN}}$  towards ground for a fixed time, causing the voltage on  $C_{\text{CPC}}$  to fall by a small decrement.

The voltage on  $C_{\text{CPC}}$  controls an additional current sink  $I_{\text{CPC}}$  that causes the capacitance attached to the input pin IN to be discharged more quickly. This arrangement constitutes a closed-loop control system, that constantly tries to equalise the discharge time  $t_{\text{SENS}}$  with  $t_{\text{REF}}$ . In the equilibrium state, the discharge times are equal and the pulses alternate between CUP and CDN.

<sup>1</sup> I: Input, O: Output, S: Supply, A: Analogue

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The counter following this logic counts the pulses CUP or CDN respectively. The counter is reset every time the pulse sequence changes from CUP to CDN or vice versa. The output pin OUT will only be activated when a sufficient number of consecutive CUP or CDN pulses occur. Low level interference or slow changes in the input capacitance do not cause the output to switch.

Various measures, such as asymmetrical charge and discharge steps, are taken to ensure that the output switches off correctly. Two different switching dynamics can be chosen by connecting the MODE pin to either GND or VDD.

A special start-up circuit ensures that the device reaches equilibrium quickly when the supply is attached.

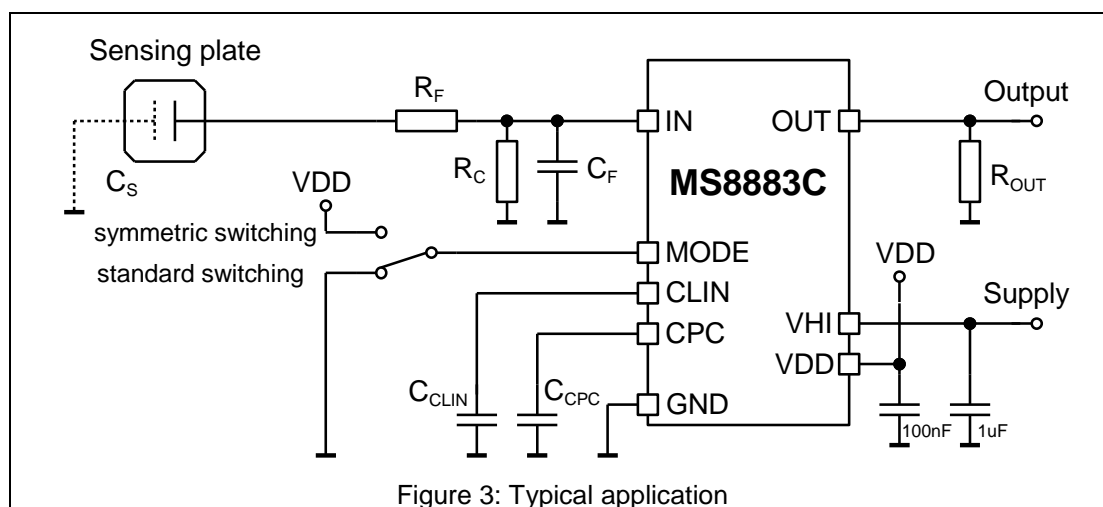
Pin OUT is an open drain output capable of pulling an external load  $R_{OUT}$  (up to 20mA) up to  $V_{HI}$ . The load resistor must be dimensioned appropriately, taking the maximum expected  $V_{HI}$  voltage into account.

A small internal 150nA current sink  $I_{SINK}$  enables a full voltage swing to take place on pin OUT, even if no load resistor is connected. This is useful for driving purely capacitive CMOS inputs. The falling slope can be fairly slow in this mode, depending on load capacitance.

The sampling rate ( $f_k$ ) corresponds to half of the frequency generated in the internal sawtooth oscillator. The sampling rate can be adjusted within a specified range by selecting the value of the  $C_{CLIN}$  capacitor.

### 8.2 Application notes

Figure 3 shows the typical connections for a general application of the MS8883C. The positive supply (3.0V to 9.0V) is connected to pin  $V_{HI}$ . It is recommended to connect smoothing capacitors to ground to both  $V_{HI}$  and  $V_{DD}$ .



The sampling rate is determined by the capacitance  $C_{CLIN}$  on pin CLIN. The rate can be adjusted from 300Hz to 3kHz. A 1kHz rate can be defined using  $C_{CLIN} = 22\text{pF}$ . A higher sampling rate reduces the reaction time and increases the current consumption.

The sensing plate capacitance  $C_S$  may consist of a small metal area, for example behind an isolating layer. The sensing plate is connected to a coaxial cable ( $C_{CABLE}$ ) which in turn is connected to the input pin IN. An internal low pass filter is used to reduce RF interference. An additional low pass filter consisting of a resistor  $R_F$  and capacitor  $C_F$  can be added to the input to further improve RF immunity as required. Typical values are  $R_F = 6.8\text{k}\Omega$  and  $C_F = 10\text{pF}$ . For good performance, the total amount of capacitance on the input ( $C_S + C_{CABLE} + C_F$ ) should be in the range 10pF to 60pF, the optimum point being around 30pF. These conditions allow the control loop to adapt to the static capacitance on  $C_S$  and to compensate for slow changes in the sensing plate capacitance. A higher capacitive input loading is possible (maximum 200pF) provided that an additional discharge resistor  $R_C$  is placed as shown in Figure 2. Resistor  $R_C$  simply reduces the discharge time such that the internal timing requirements are fulfilled. A typical value for  $R_C$  is between 5 and 50k $\Omega$ .

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The sensitivity of the sensor can be influenced by the sensing plate area and capacitor  $C_{CPC}$ . Typically  $C_{CPC}$  is 220nF. The sensitivity is significantly reduced when  $C_{CPC} = 100nF$ . Maximum sensitivity is reached when  $C_{CPC} = 2.2\mu F$  but this also increases sensitivity to interference. The CPC pin has high impedance and is sensitive to leakage currents. Therefore  $C_{CPC}$  should be a high quality foil or ceramic capacitor, for example an X7R type.

### 8.3 Switching dynamic selection

Two different switching dynamics can be selected using the pins MODE. For most applications the standard asymmetric switching behaviour is recommended. For proximity sensing applications with high sensitivity setting, it can be beneficial to use the symmetric switching behaviour.

- The standard switching mode (MODE pin connected to GND) implements an *asymmetry* between on-switching and off-switching requirements. For on-switching a relatively larger input capacitance increase is required, than the input capacitance decrease required for off-switching. This implementation assures robust off-switching performance even under noisy environmental conditions.
- In the *symmetric* switching mode (MODE pin connected to VDD), the input capacitance change required for on-switching is similar to the capacitance change needed for off-switching. This mode supports proximity applications, where symmetrical on- and off-switching sensitivity is required to avoid unexpected behaviour.

Important: When the symmetric switching mode is desired, the MODE pin has to be connected to the VDD pin. The MODE pin **must not** be connected to the external supply voltage.

### 8.4 Internal voltage regulator

The circuit has an integrated voltage regulator, supplied by pin  $V_{HI}$ , that provides an internal  $V_{DD}$  supply, limited to a maximum of 4.6 V. The lock-in voltage,  $V_{LOCK}$ , on  $V_{HI}$  is typically 4.0 V. The regulated supply is available at pin  $V_{DD}$  and can be used to supply power to external electronic components (0.5mA maximum). Figure 4 shows the relationship between  $V_{HI}$ ,  $V_{LOCK}$  and  $V_{DD}$ .

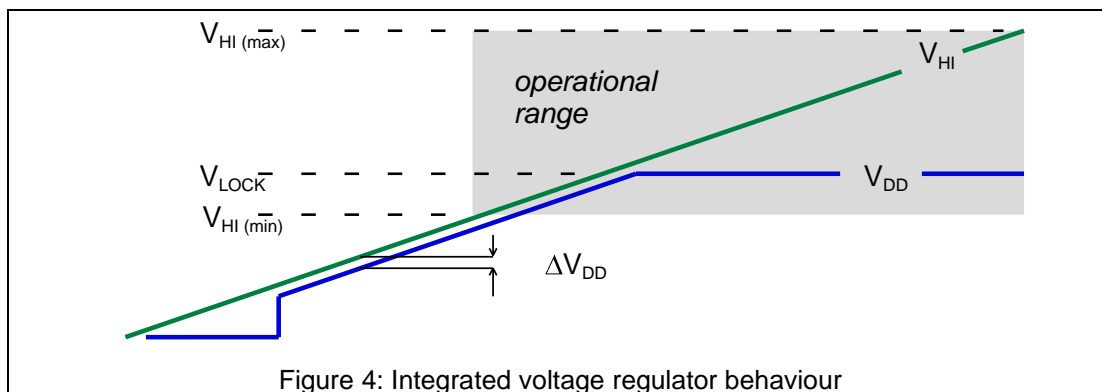


Figure 4: Integrated voltage regulator behaviour

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## 9 Electrical Characteristics

### 9.1 Limiting values and ESD protection

Name	Parameter	Min	Max	Unit
V <sub>HI</sub>	Positive supply wrt to GND	-0.5	9.0	V
V <sub>IN</sub> , V <sub>MODE</sub> , V <sub>CPC</sub>	Input voltage on pins IN, MODE, CPC	-0.5	V <sub>DD</sub> +0.5	V
I <sub>OUT</sub>	Output current on pins OUT to GND	-10	50	mA
I <sub>GND</sub>	Total current to GND	-10	50	mA
I <sub>PIN</sub>	Current through any pin	-10	10	mA
P <sub>TOT</sub>	Power dissipation		100	mW
T <sub>stg</sub>	Storage temperature	-60	+125	°C
V <sub>ESD</sub>	electrostatic discharge voltage		+/- 2000	V
	HBM		+/- 200	V
	MM			

### 9.2 DC Characteristics

Conditions: V<sub>HI</sub> = 5V DC, T = 25°C, if not stated otherwise

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>HI</sub>	Positive supply		2.7 <sup>2</sup>		9.0	V
V <sub>LOCK</sub>	Regulator lock-in voltage	No external load		4.0		V
V <sub>DD</sub>	Regulated internal supply	V <sub>HI</sub> > V <sub>LOCK</sub>	3.0	4.0	4.6	V
V <sub>DD</sub>	Internal supply	VDD connected to VHI	2.7 <sup>3</sup>		4.6	V
ΔV <sub>DD</sub>	Regulator voltage drop	V <sub>HI</sub> < V <sub>LOCK</sub> , no external load on V <sub>DD</sub>		10	50	mV
I <sub>HI</sub>	Operating current	Idle state <sup>3</sup> , output inactive, f <sub>k</sub> = 1 kHz		3	5	μA
		Idle state <sup>3</sup> , output inactive, f <sub>k</sub> = 1 kHz, V <sub>HI</sub> = 3.0V		2.2	3.5	μA
I <sub>SINK</sub>	Output sink current	Internal constant current to GND		150		nA
V <sub>IL</sub>	Input low level	MODE pin	0.7		V <sub>DD</sub>	V
V <sub>IH</sub>	Input high level	MODE pin	V <sub>SS</sub>		0.3 V <sub>DD</sub>	V
V <sub>OUT</sub>	Output voltage	OUT pin	0	V <sub>HI</sub>	9.0	V
I <sub>OUT</sub>	Output current	Operating range of output stage <sup>4</sup>	0	10	20	mA
V <sub>FOUT</sub>	Output saturation voltage	OUT pin: I <sub>OUT</sub> = 10 mA	0.1	0.2	0.4	V
		OUT pin: I <sub>OUT</sub> = 10 mA, V <sub>HI</sub> = 3.0V	0.1	0.3	0.5	V
C <sub>VDD</sub>	Ext. V <sub>DD</sub> decoupling capacitor	Ceramic chip capacitor recommended on pin VDD	100		220	nF
V <sub>CPC</sub>	Reservoir capacitor voltage	Usable control range on pin CPC	0.6		V <sub>DD</sub> -0.3	V
I <sub>L,CPC</sub>	Reservoir capacitor leakage current	Low leakage X7R ceramic type recommended			1	nA
T <sub>amb</sub>	Operating temperature range		-40	25	85	°C

<sup>2</sup> When the input capacitance range is limited to 10pF ≤ C<sub>IN</sub> ≤ 40pF, or an external pull down resistor R<sub>C</sub> is used, the device can be operated down to V<sub>HI</sub>=3.0V over the full temperature range.

When the input capacitance range is limited to 10pF ≤ C<sub>IN</sub> ≤ 30pF, or an external pull down resistor R<sub>C</sub> is used, the device can be operated down to V<sub>HI</sub>=2.7V over the reduced temperature range 0 ... 70°C.

<sup>3</sup> Idle state is the steady state after completed power-up, without any activity on the sensor plate, and the voltage on the reservoir capacitor C<sub>CPC</sub> settled.

<sup>4</sup> For reliability reasons the average output current must be limited to maximum 4.6mA@70°C and 3.0mA@85°C

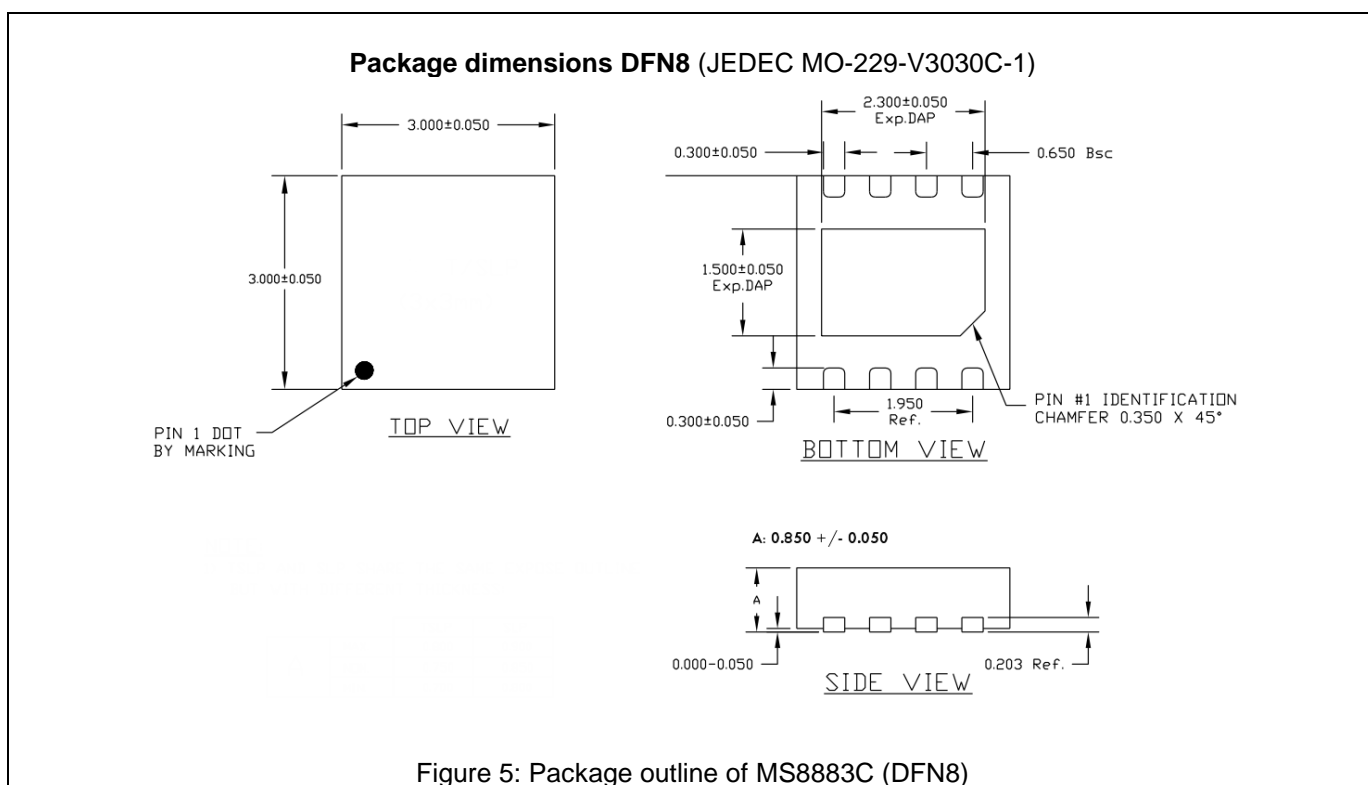
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## 9.3 AC Characteristics

Conditions:  $V_{HI} = 5V$  DC,  $C_{CLIN} = 22pF$ ,  $C_{CPC} = 220nF$ ,  $T = 25^{\circ}C$ , if not stated otherwise

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{CLIN}$	Oscillator capacitance	Operating range	0	22	100	pF
$C_{CPC}$	Reservoir capacitor	Low leakage X7R ceramic type recommended	47	220	2500	nF
$C_{IN}$	Input capacitance	Sensing plate + parasitic	10		60	pF
		Sensing plate + parasitic, $V_{HI}=3.0V$ , full temperature range	10		40	pF
		Sensing plate + parasitic, $V_{HI}=2.7V$ , over reduced temperature range 0...70°C	10		30	pF
$t_{WAIT}$	Power-on start-up time	Until idle state is established		0.5		s
$f_K$	Sampling rate	$C_{CLIN} = 0$		3.3		kHz
		$C_{CLIN} = 22 pF$		1		kHz
		$C_{CLIN} = 100 pF$		275		Hz
$t_{SW}$	Reaction time on sensor capacitance change	$f_K = 1$ kHz, MODE connected to GND		64		ms
		$f_K = 1$ kHz, MODE connected to VDD		32		ms

## 10 Package outlines



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## 11 Legal disclaimer

This product is not designed for use in life support appliances or systems where malfunction of these parts can reasonably be expected to result in personal injury. Customers using or selling this product for use in such appliances do so at their own risk and agree to fully indemnify Microdul AG for any damages resulting from such applications.

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