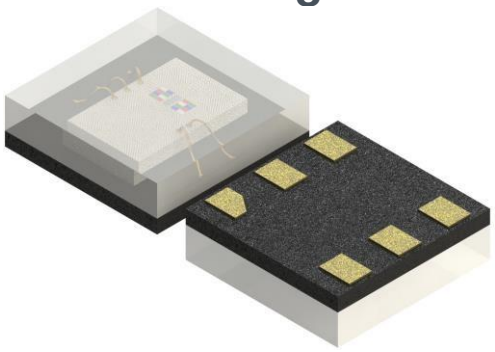
Digital RGBW-IR Color Sensor



Description

WH3620 is a color-based light to digital converter which combines photodiodes, current amplifiers, analog circuit and digital signal processor.

WH3620 provides red, green, blue, white and infrared light sensing. Each channel is parallel output at the same time, so it has excellent performance of illuminance & correlated color temperature under different light conditions such as white LED, CWF, TL84, D65, illuminant A and horizon. It can work from dark to direct sunlight, the selectable detect range is about 70dB.

WH3620 has programmable interrupt function with high / low threshold.

Features

- I2C interface (Fast Speed Mode at 400kHz/s)
- Supply voltage range from 2.4V to 3.6V
- Operating temperature from -40°C to +85°C
- Package level trimming.
- Power on reset & brown out reset.
- Waiting time function for reducing power consumption.
- R, G, B, W and IR five channel parallel output.
- Fluorescent light flicker immunity.
- Selectable analog gain.
- Selectable resolution (up to 16-bit).
- High sensitivity in low illumination.
- Wide detect range in high illumination.
- High accuracy of LUX & CCT.

Applications

- Handset device
  - Mobile phone, tablet, color matcher
- Consumer device
  - LCD TV, digital camera, toy
- Computing device
  - Laptop, LCD monitor
- Smart lighting
  - Ceiling light, panel light

Block Diagram

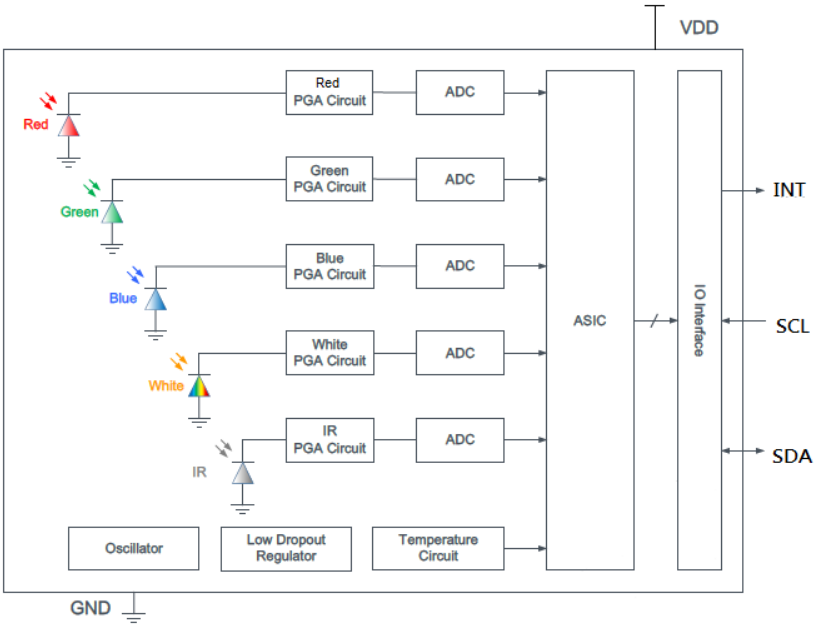
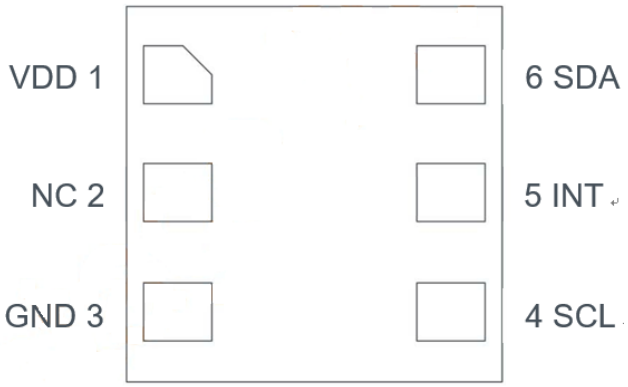


Fig. 1 Block Diagram

I/O Pins Configuration



Pin	I/O Type	Pin Name	Description
1		VDD	Power supply
2		NC	No connection
3		GND	Ground
4	I	SCL	I^2C serial clock line
5	O	INT	Interrupt pin
6	I/O	SDA	I^2C serial data line

Absolute Maximum Ratings*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	4.5	V
I²C Bus Pin Voltage	V_{SCL}, V_{SDA}, V_{INT}	-0.2 to 4.5	V
I²C Bus Pin Current	I_{SCL}, I_{SDA}, I_{INT}	10	mA
Operating Temperature	T_{ope}	-40 to +85	˚C
Storage Temperature	T_{stg}	-45 to +100	˚C
ESD Rating	Human Body Mode	2	KV

*Note : Exceeding these ratings could cause damage to the device. All voltages are with respect to ground. Currents are positive into, negative out of the specified terminal.

Recommended Operation Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply Voltage **Note1**	V_{DD}	2.4	3	3.6	V	
I²C Bus Pin Voltage **Note2**	V_{Bus}	1.62	1.8	V_{DD}	V	$V_{Bus} \leq V_{DD}$
Operating Temperature	T_{ope}	-40		+85	˚C	
I²C Bus Input High Voltage **Note2**	V_{IH_SCL}, V_{IH_SDA}	1.4			V	
I²C Bus Input Low Voltage **Note2**	V_{IL_SCL}, V_{IL_SDA}			0.5	V	
SDA Output Low Voltage	V_{OL_SDA}	0		0.4	V	3mA sinking current
		0		0.6	V	6mA sinking current
INT Output Low Voltage	V_{OL_INT}	0		0.4	V	3mA sinking current

Notes:

1. The power supply need to make sure the VDD slew rate at least 0.5V/ms. WH3620 have power on reset function. When VDD drops below 1.4V under room temp, the IC will be reset automatically. Then power back up at the requirement slew rate, and write registers to the desired values.
2. The specs are defined under VDD=3.3V, T=25°C

Electrical & Optical Specifications

Unless otherwise specified, the following specifications apply over the operating ambient temperature T=25˚C, VDD = 3.3V, and measure the output current by white light LED.

Electrical Characteristics	Symbol	MIN	TYP	MAX	Notes	Unit
Active Supply Current Note1	I_{DD}		210		Ev=0 Note1	μA
	I_{PD1}		2.5		Sleep mode Ev= 0 I^2C inactive	μA
	I_{PD2}		1.5		Sleep mode, Ev=0, I2C Inactive EN_FRST = 1	μA
Device Boot Time Note2	T_{boot}		20			ms

Waiting Characteristics	Symbol	MIN	TYP	MAX	Notes	Unit
Wait time unit	Wunit		10			ms
Wait time number	WTIME	1		256		Wunit

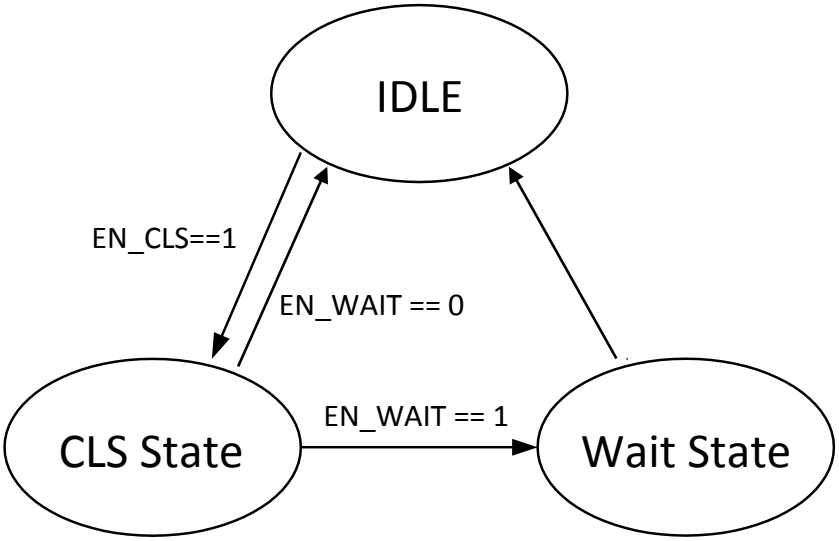
CLS Characteristics	Symbol	MIN	TYP	MAX	Notes	Unit
Sensing Gain Relative to x1 setting	PGA_CLA		4			
			8			
			32			
			96			
			192			
Sensing Area Relative to x1 setting	DIODE_SEL		2			
Unit of ADC integration time	INT_TIME	1		64	1T=2.06ms	T
Number of ADC integration time	CLSCONV	1		16		INT TIME
Full ADC counts per step		0		1023	INT_TIME=1	count
Dark ADC Count (White LED, Ev=0)			1	3	PGA_CLA=192 INT_TIME=64T CLSCONV=1	count
Sensitivity (White LED, Ev= 500 Lux)	RCH	4576	5200	5824	PGA_CLA=96 INT_TIME=64T CLSCONV=1	count
	GCH	7463	8480	9498		count
	BCH	2570	2920	3271		count
	WCH	12743	14480	16218		count

Notes1: The testing condition WTIME=6, INT_TIME=64T, CLSCONV=1

Notes2: The Device Boot Time (T_{boot}) is the delay time that the host can send the first I2C command after the VDD ready.

State Machine

There are two operation mode CLS. The state machine is shown below:



Typical Characteristics Curves

Unless otherwise specified, the following specifications apply over the operating ambient temperature T = 25˚C, VDD = 3.3V.

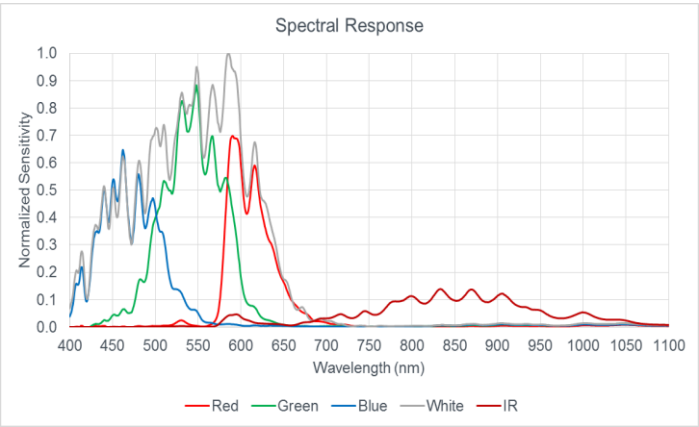


Fig. 2 Spectral Response

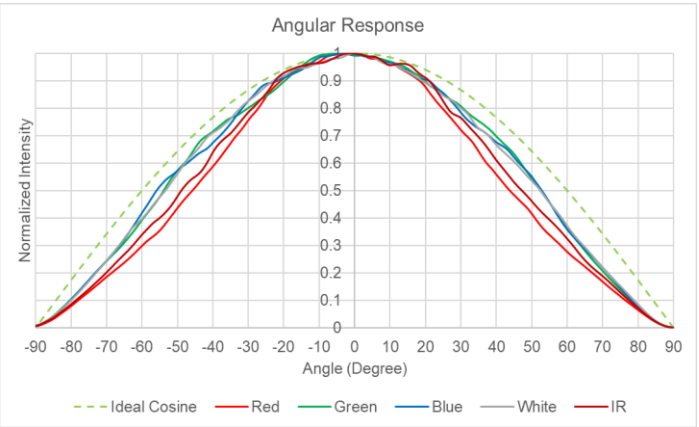
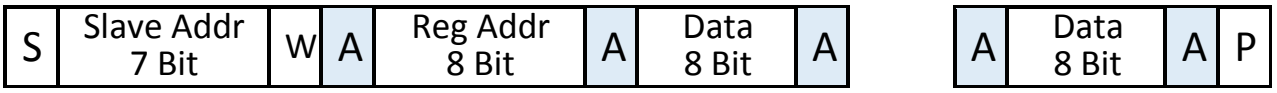


Fig. 3 Angular Response

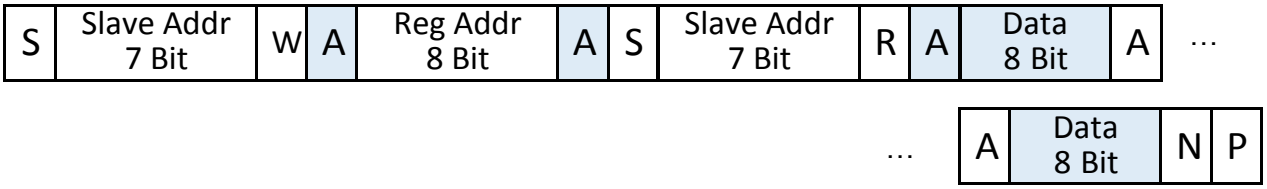
I²C Write

I²CBlock Write



I²CRead

I²CBlock Read



I²C Slave Address and R/W bit

This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). A ‘0’ indicates a transmission (WRITE), a ‘1’ indicates a request for data (READ). The slave address of this device is 0x38.

Register Set

The WH3620 is operated over the I2C bus with registers that contain configuration, status, and result information. All registers are 8 bits long.

Address	Name	Type	Default value	Description
0x00	SYSM_CTRL	RW	0x00	CLS operation mode control, waiting mode control, SW reset
0x01	INT_CTRL	RW	0x03	Interrupt pin control, interrupt persist control
0x02	INT_FLAG	RW	0x80	Interrupt flag, error flag, power on reset (POR) flag
0x03	WAIT_TIME	RW	0x00	Waiting time setting
0x04	CLS_GAIN	RW	0x81	CLS analog gain setting
0x05	CLS_TIME	RW	0x03	CLS integrated time setting
0x0B	PERSISTENCE	RW	0x01	CLS persistence setting
0x0C	CLS_THRES_LL	RW	0x00	CLS lower interrupt threshold - LSB
0x0D	CLS_THRES_LH	RW	0x00	CLS lower interrupt threshold - MSB
0x0E	CLS_THRES_HL	RW	0xFF	CLS higher interrupt threshold - LSB
0x0F	CLS_THRES_HH	RW	0xFF	CLS higher interrupt threshold - MSB
0x16	INT_SOURCE	RW	0x08	CLS interrupt source
0x17	ERROR_FLAG	RW	0x00	Error flag
0x1C	RCH_DATA_L	R	0x00	RCH output data - LSB
0x1D	RCH_DATA_H	R	0x00	RCH output data - MSB
0x1E	GCH_DATA_L	R	0x00	GCH output data - LSB
0x1F	GCH_DATA_H	R	0x00	GCH output data - MSB
0x20	BCH_DATA_L	R	0x00	BCH output data - LSB
0x21	BCH_DATA_H	R	0x00	BCH output data - MSB
0x22	WCH_DATA_L	R	0x00	WCH output data - LSB
0x23	WCH_DATA_H	R	0x00	WCH output data - MSB
0x24	IRCH_DATA_L	R	0x00	IRCH output data - LSB
0x25	IRCH_DATA_H	R	0x00	IRCH output data - MSB

0x00 SYSM_CTRL

0x00	SYSM_CTRL, System Control (Default = 0x00)							
BIT	7	6	5	4	3	2	1	0
R/W	SWRST	EN_WAIT	EN_FRST	0	0	0	EN_IR	EN_CLS

SWRST： Software reset. Reset all register to default value.

0: (Default)

1: Reset will be triggered.

EN_WAIT： Waiting time will be inserted between two measurements.

0: Disable waiting function. (Default)

1: Enable waiting function.

EN_FRST：

0: Enable (Brown Out Reset circuit enable)

1: Disable (Brown Out Reset circuit disable)

EN_IR ： Enables IR function.

0: Disable IR function. (Default)

1: Enable IR function.

EN_CLS： Enables CLS function.

0: Disable CLS function. (Default)

1: Enable CLS function.

0x01 INT_CTRL

0x01	Interrupt Pin Control (Default = 0x03)							
BIT	7	6	5	4	3	2	1	0
R/W	0	0	0	CLS_ SYNC	0	0	1	EN_CINT

CLS_SYNC ： Measurement is pended when CLS interrupt is triggered. Until clear the interrupt then start the next measurement.

0: Disable pending CLS function. (Default)

1: Enable pending CLS function.

EN_CINT ： The CLS interrupt (INT_CLS) flag can trigger the INT pin to low.

0: Disable **INT_CLS** effect INT pin.

1: Enable **INT_CLS** effect INT pin. (Default)

0x02 INT_FLAG

0x02	INT_FLAG, System Control (Default = 0x80)							
BIT	7	6	5	4	3	2	1	0
R/W	INT_POR	DATA_FLAG	0	0	0	0	0	INT_CLS

INT_POR： Power-On-Reset Interrupt flag trigger the INT pin when the flag sets to one. Write zero to clear the flag.

0:

1: This bit will be set to one when it satisfy one of the following conditions:

- Power On
- VDD < 1.4V
- SWRST

DATA_FLAG ： It shows if any data is invalid after completion of each conversion cycle. This bit is read-only.

0: data valid.

1: data invalid.

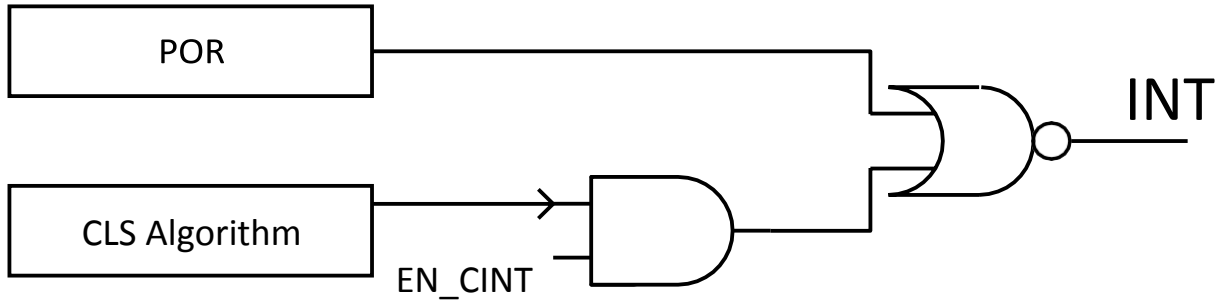
INT_CLS ： CLS Interrupt flag. It correlation with sensor data and CLS high/low threshold. Write zero to clear the flag.

0: CLS Interrupt not trigger or be cleared.

1: CLS interrupt triggered

Interrupt Behavior

The interrupt pin will be pulled low when POR occur or ALS interrupt trigger.



CLS Interrupt Algorithm

Correlative register:

The CLS Interrupt (**INT_CLS, register 0x02, bit0),**

The CLS Persistence (**PRS_CLS**, register 0x0B, bit0 to bit3),

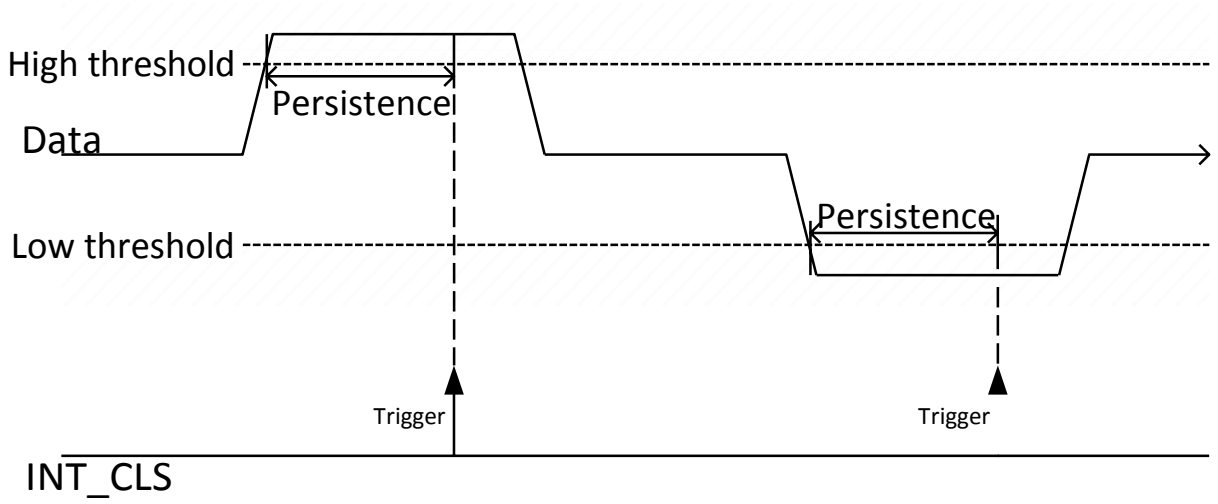
The CLS Data (**W channel data**, register 0x22 to 0x23),

The CLS Low Threshold (**ALS_THRES_L**, register 0x0C to 0x0D),

The CLS High Threshold (**ALS_THRES_H**, register 0x0E to 0x0F).

INT_CLS triggered condition:

1. Rule of active interrupt: **DATA** > **CLS_THRES_H** or **DATA** < **CLS_THRES_L.**
2. If the **DATA** meets the rule, the **interrupt** count increases one.
   If the **DATA** fails in the rule, the interrupt count will be clear.
3. When the **interrupt** count equal to **PRS_CLS setting**, **INT_CLS** will be triggered and reset the interrupt counter.
4. If **PRS_CLS** is set to zero, **threshold** will be ignored and **DATA** will meets the active interrupt rule forcibly.



0x03 WAIT_TIME

0x02	WAIT_TIME, waiting time (Default = 0x00)							
BIT	7	6	5	4	3	2	1	0
R/W	WTIME							

WTIME : This register controls the time unit of waiting state which is inserted between any two measurements. It is 10ms per time unit.

0x00: 1 time unit.

0x01: 2 time units

……

0x7f: 256 time units

0x04 CLS_GAIN

0x04	CLS_GAIN, ALS analog gain (Default = 0x81)							
BIT	7	6	5	4	3	2	1	0
R/W	DIOD_SELT	0	PGA_ALS					

DIOD_SELT ： CLS sensor area select.

0: x1

1: x2 (default)

PGA_ALS ： CLS sensing gain.

0x01: x1 (default)

0x02: x4

0x04: x8

0x08: x32

0x10: x96

0x20: x192

0x05 CLS_TIME

0x05	CLS_TIME, CLS integrated time (Default = 0x03)							
BIT	7	6	5	4	3	2	1	0
R/W	CLSCONV				0	0	INT_TIME	

CLSCONV： This register controls the conversion time of AD converter at CLS mode (T_{CLS}), and the resolution of output dat.

0x00: The maximum count of output data is 1023, T_{ALS} = 1* INT_TIME (default)

0x01: The maximum count of output data is 2047, T_{ALS} = 2* INT_TIME

……

0x0f: The maximum count of output data is 16384, T_{ALS} = 16* INT_TIME

INT_TIME： This register controls the integrated time.

0x0: 1 INT_TIME = 2.0667 ms.

0x1: 1 INT_TIME = 8.2668 ms.

0x2: 1 INT_TIME = 33.0672 ms.
0x3: 1 INT_TIME = 132.2688 ms.

The maximum count of **output data is** minimum of [1024 x (**ATIME** + 1) – 1, 65535].

The conversion time of CLS function (T_{CLS}) is decided by **CLSCONV and INT_TIME**.
T_{CLS} = **INT_TIME** x (**CLSCONV** + 1) (ms)

0x0B PERSISTENCE

0x0B	PERSISTENCE, CLS persistence setting (Default = 0x01)							
BIT	7	6	5	4	3	2	1	0
R/W	0	0	0	0	PRS_CLS			

PRS_CLS：This register sets the numbers of similar consecutive CLS interrupt events before the interrupt pin is triggered.

0x0: Every CLS conversion is done.
0x1: 1 CLS interrupt event is asserted.
……
0xf: 15 consecutive CLS interrupt events are asserted.

0x0C/0X0D CLS_THRES_L

0x0C 0x0D	CLS_THRES_L, CLS low interrupt threshold (Default = 0x0000)							
BIT	7	6	5	4	3	2	1	0
R/W	CLS_THRE_LL							
R/W	CLS_THRE_LH							

This register sets the lower threshold value of CLS interrupt. The interrupt algorithm compares the selected CLS data and CLS threshold value.

CLS_THRE_LL：CLS lower interrupt threshold value, LSB. (Reg. 0x0C)
CLS_THRE_LH：CLS lower interrupt threshold value, MSB. (Reg. 0x0D)

0x0E/0x0F CLS_THRES_H

0x0E 0x0F	CLS_THRES_H, CLS high interrupt threshold (Default = 0xFFFF)							
BIT	7	6	5	4	3	2	1	0
R/W	CLS_THRE_HL							
R/W	CLS_THRE_HH							

This register sets the high threshold value of CLS interrupt. The interrupt algorithm compares the selected CLS data and CLS threshold value.

CLS_THRE_HL：CLS high interrupt threshold value, LSB. (Reg. 0x0E)
CLS_THRE_HH：CLS high interrupt threshold value, MSB. (Reg. 0x0F)

0x16 INT_SOURCE

0x16	INT_SOURCE, ALS interrupt source (Default = 0x08)							
BIT	7	6	5	4	3	2	1	0
R/W	0	0	0	INT_SRC				

INT_SRC = This register sets to select the CLS data for the CLS Interrupt algorithm.

0x01: Select RCH_DATA.
0x02: Select GCH_DATA.
0x04: Select BCH_DATA.
0x08: Select WCH_DATA.
0x10: Select IRCH_DATA.

0x17 ERROR_FLAG

0x17	ERROR_FLAG, Error flag status							
BIT	7	6	5	4	3	2	1	0
R/W	0	0	0	ERR_IRCH	ERR_WCH	ERR_BCH	ERR_GCH	ERR_RCH

This register indicates the CLS data status. If the CLS data is outside of measurable range, the corresponding error flag (ERR_RCH, ERR_GCH, ERR_BCH, ERR_WCH, and ERR_IRCH) will set to one. That also means the data is invalid.

0x1C/0x1D RCH_DATA

0x1C 0x1D	RCH_DATA, R channel output data.							
BIT	7	6	5	4	3	2	1	0
R/W	RCH_DATA _L							
R/W	RCH_DATA_H							

The R channel conversion result is written into RCH_DATA when CLS conversion is done.

For insuring the data in the register comes the same measurement, the high byte data will be latched when the low byte data has been accessed until the high byte data has been read.

0x1E/0x1F GCH_DATA

0x1E 0x1F	GCH_DATA, G channel output data.							
BIT	7	6	5	4	3	2	1	0
R/W	GCH_DATA_L							
R/W	GCH_DATA_H							

The G channel sensor result is written into GCH_DATA when CLS conversion is done.

For insuring the data in the register comes the same measurement, the high byte data will be latched when the low byte data has been accessed until the high byte data has been read.

0x20/0x21 BCH_DATA

0x20 0x21	BCH_DATA, B channel output data.							
BIT	7	6	5	4	3	2	1	0
R/W	BCH_DATA_L							
R/W	BCH_DATA_H							

The B channel sensor result is written into BCH_DATA when CLS conversion is done.

For insuring the data in the register comes the same measurement, the high byte data will be latched when the low byte data has been accessed until the high byte data has been read.

0x22/0x23 WCH_DATA

0x22 0x23	WCH_DATA, W channel output data.							
BIT	7	6	5	4	3	2	1	0
R/W	WCH_DATA_L							
R/W	WCH_DATA_H							

The W channel sensor result is written into WCH_DATA when CLS conversion is done.

For insuring the data in the register comes the same measurement, the high byte data will be latched when the low byte data has been accessed until the high byte data has been read.

0x24/0x25 IRCH_DATA

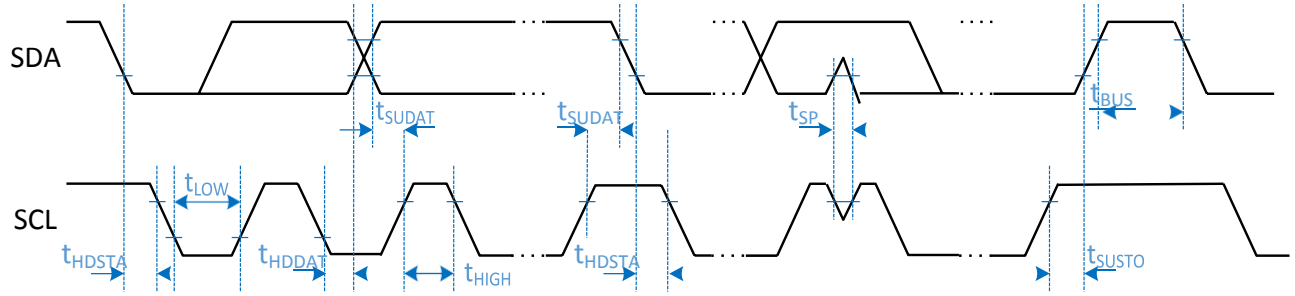
0x24 0x25	IRCH_DATA, IR channel output data.							
BIT	7	6	5	4	3	2	1	0
R/W	IRCH_DATA_L							
R/W	IRCH_DATA_H							

The IR channel sensor result is written into IRCH_DATA when CLS conversion is done.

For insuring the data in the register comes the same measurement, the high byte data will be latched when the low byte data has been accessed until the high byte data has been read.

I²C Interface Timing Characteristics

This section will describe the protocol of the I²C bus. For more details and timing diagrams please refer to the I²C specification.



Parameter (*)	Symbol	Fast mode		Unit
		Min	Max	
SCL clock frequency	f_{SCL}	100	400	kHz
Bus free time between STOP condition and START condition	t_{BUS}	1.3	--	μs
LOW period of the SCL clock	t_{LOW}	1.3	--	μs
HIGH period of the SCL clock	t_{HIGH}	0.6	--	μs
Hold time (repeated) START condition	t_{HDSTA}	0.6	--	μs
Set-up time (repeated) START condition	t_{SUSTA}	0.6	--	μs
Set-up time for STOP condition	t_{SUSTO}	0.6	--	μs
Data hold time	t_{HDDAT}	50	--	ns
Data set-up time	t_{SUDAT}	100	--	ns
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	0	50	ns
Rise time of both SDA and SCL signals		20 x VDD/5.5	300	ns
Fall time of both SDA and SCL signals		20 x VDD/5.5	300	ns

(*) Specified by design and characterization; not production tested.

(**) All specifications are at V_{Bus} = 3.3V, T_{ope}=25°C, unless otherwise noted.

I²CBus Clear

In the unlikely event where the clock (SCL) is stuck LOW, the preferential procedure is to reset the bus using the HW reset signal if your I2C devices have HW reset inputs. If theI2C devices do not have HW reset inputs, cycle power to the devices to activate the mandatory Internal Power-On Reset (POR) circuit.

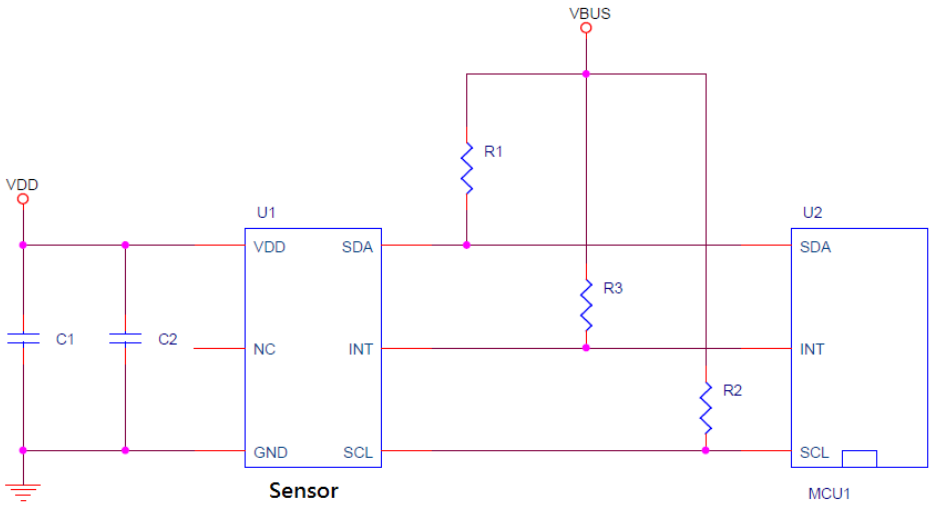
If the data line (SDA) is stuck LOW, the master should send nine clock pulses. The device that held the bus LOW should release it sometime within those nine clocks.

I²C General Call Software Reset

Following a General Call, (0000 0000), sending 0000 0110 (06h) as the second byte causes software reset. This feature is optional and not all devices will respond to this command. On receiving this 2-byte sequence, all devices designed to respond to the general call address will reset and take in the programmable part of their address.

Precautions have to be taken to ensure that a device is not pulling down the SDA or SCL line after applying the supply voltage, since these low levels would block the bus.

Application Circuit

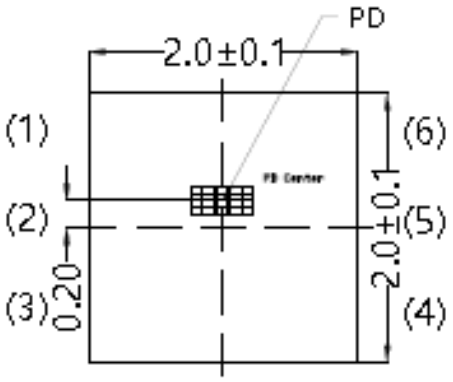


The capacitors (C1, C2) are required for power supply. The capacitors should be placed as close as possible to the device. The high frequency AC noises can be shunted to the ground by the capacitors. The transient current caused by digital circuit switching also can be handled by the capacitors. A typical value 0.1 / 1 μF can be used.

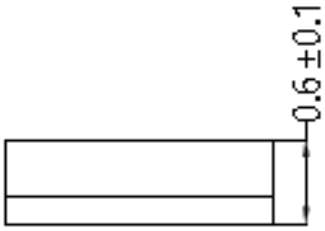
The pull-up resistors (R1, R2) are required for I²C communication. At fast speed mode (400kHz/s) and VBUS = 3V, 1.5kΩ resistors can be used. The pull-up resistor (R3) is also required for the interrupt, a typical value between 10 kΩ and 100 kΩ can be used.

Package Outline Drawing

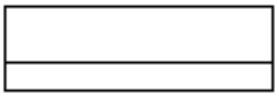
Top View



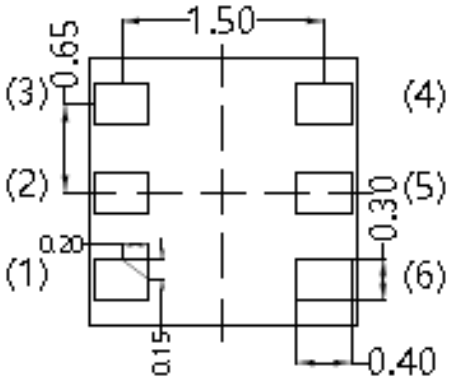
Front View



Right Side View

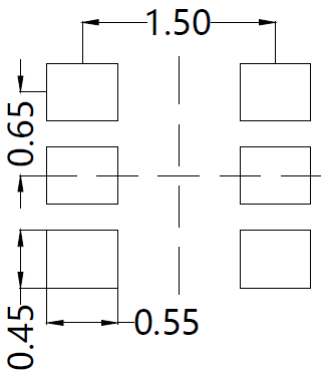


Bottom View



Pin-out	Name
(1)	VDD
(2)	NC
(3)	GND
(4)	SCL
(5)	INT
(6)	SDA

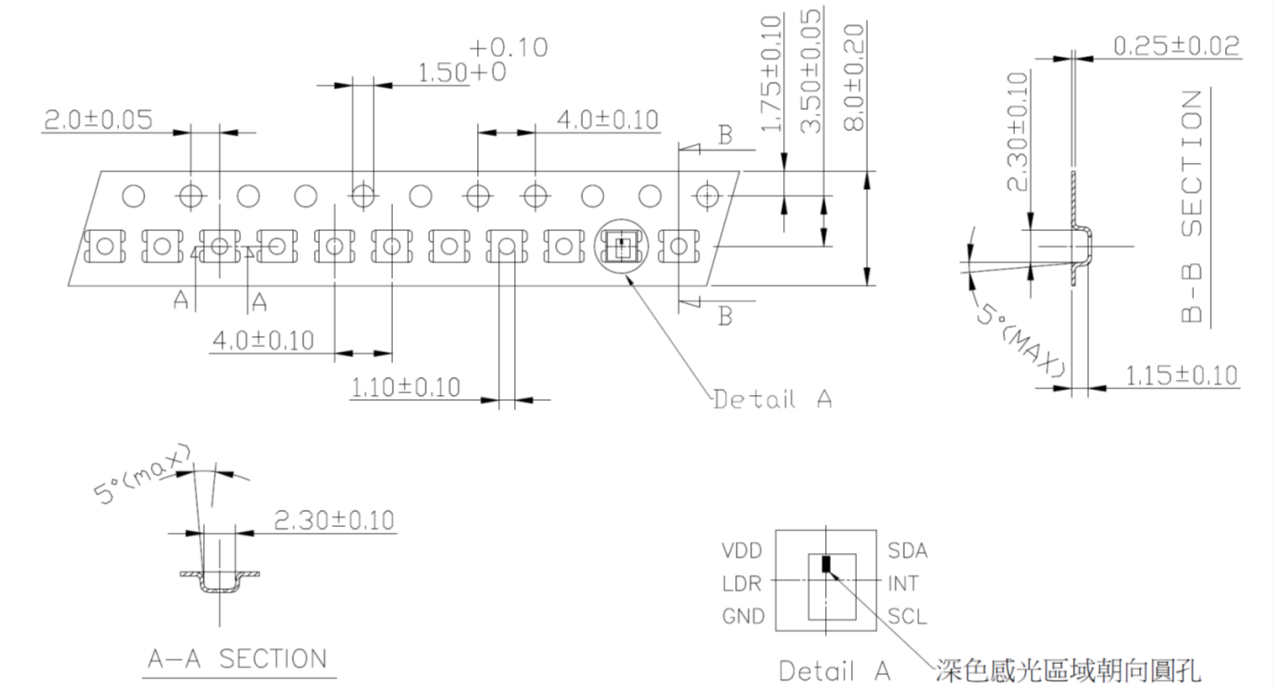
Recommended Land Pattern



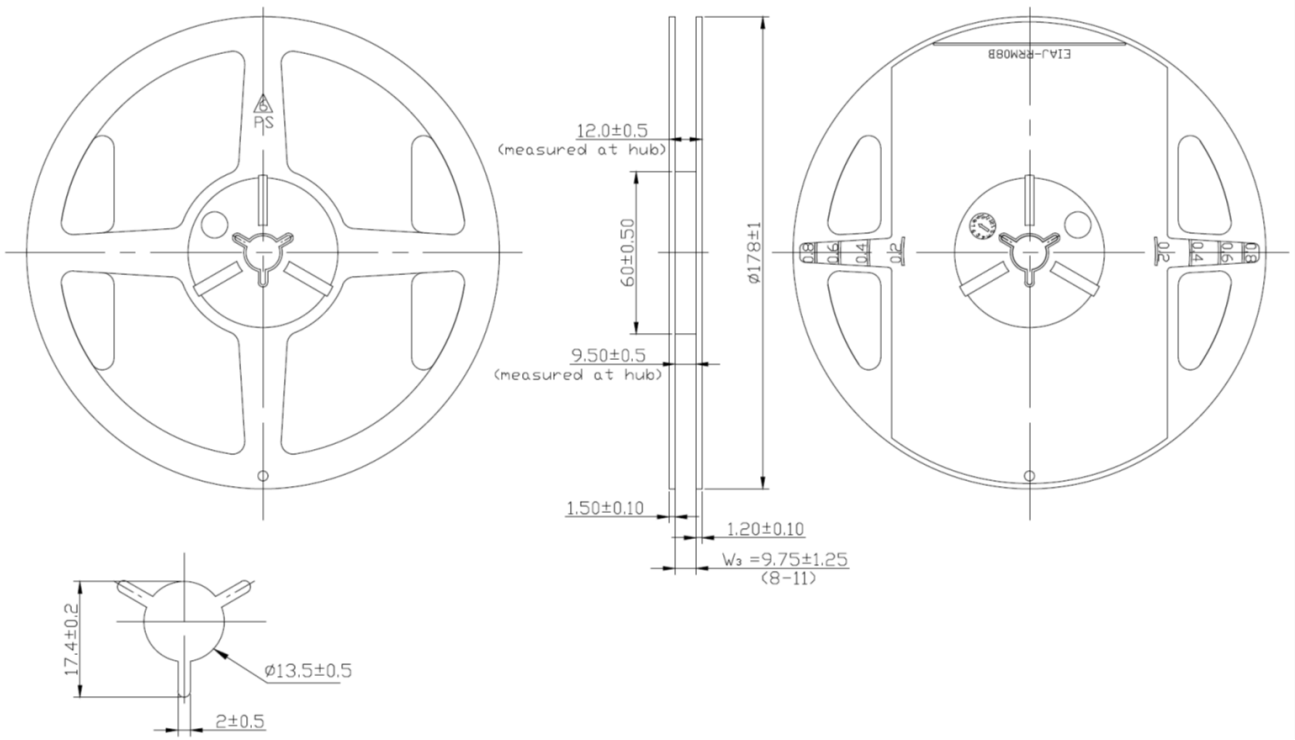
Notes :

1. All dimensions in millimeters.
2. Dimension tolerance is ± 100 μm unless otherwise noted.

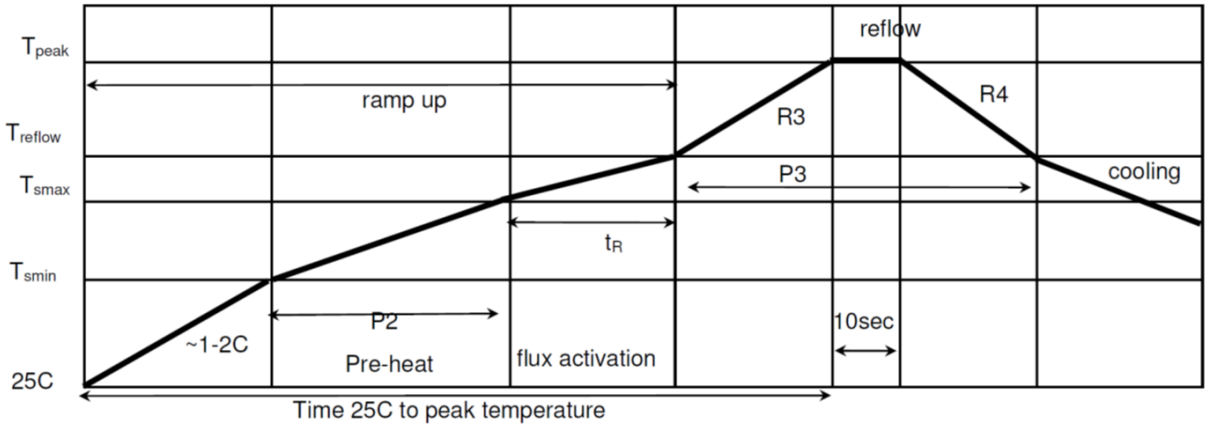
Package Tape and Reel



Unit: mm



Recommended Reflow Profile



	Peak temperature (Tpeak)	255-260C (max) ; 10sec
Pre-Heat	Temperature min (Tsmin) Temperature max (Tsmax) P2: (Ts min to Ts max)	150C 2C/sec 150C-217C 100s to 180s 90-110s
Time maintain above	Temperature (T_{reflow}) Time (P3) R3 slope (from 217C -> peak) R4 slope (from peak -> 217C)	217C 60-90sec 2C/sec [typ] -> 2.5C/sec (max) -1.5C/sec [typ]-> -4C/sec (max)
	Time to peak temperature	480s max
	Cooling down slope (peak to 217C)	2-4C/ sec