CJC8988

Stereo CODEC for Portable Audio Applications

Edition	Author	Date	Description
V1.0	By tf	2012.01	Stereo CODEC for Portable Audio Applications
V2.0	By tf	2012.09	Complete function
V3.0	By tf	2013.05	Complete function
V3.1	By tf	2013.05	Complete version

1. DESCRIPTION

The CJC8988 is a low power, high quality stereo CODEC designed for portable digital audio applications.

The device integrates complete interfaces to 2 stereo headphone or line out ports. External component requirements are drastically reduced as no separate headphone amplifiers are required. Advanced on-chip digital signal processing performs graphic equaliser, 3-D sound enhancement and automatic level control for the microphone or line input.

The CJC8988 can operate as a master or a slave, with various master clock frequencies including 12 or 24MHz for USB devices, or standard 256fs rates like 12.288MHz and 24.576MHz. Different audio sample rates such as 96kHz, 48kHz, 44.1kHz are generated directly from the master clock without the need for an external PLL.

The CJC8988 operates at supply voltages down to 1.8V, although the digital core can operate at voltages down to 1.5V to save power, and the maximum for all supplies is 3.3Volts. Different sections of the chip can also be powered down under software control. The CJC8988 is supplied in a very small and thin 4x4mm COL package, ideal for use in hand-held and portable systems.

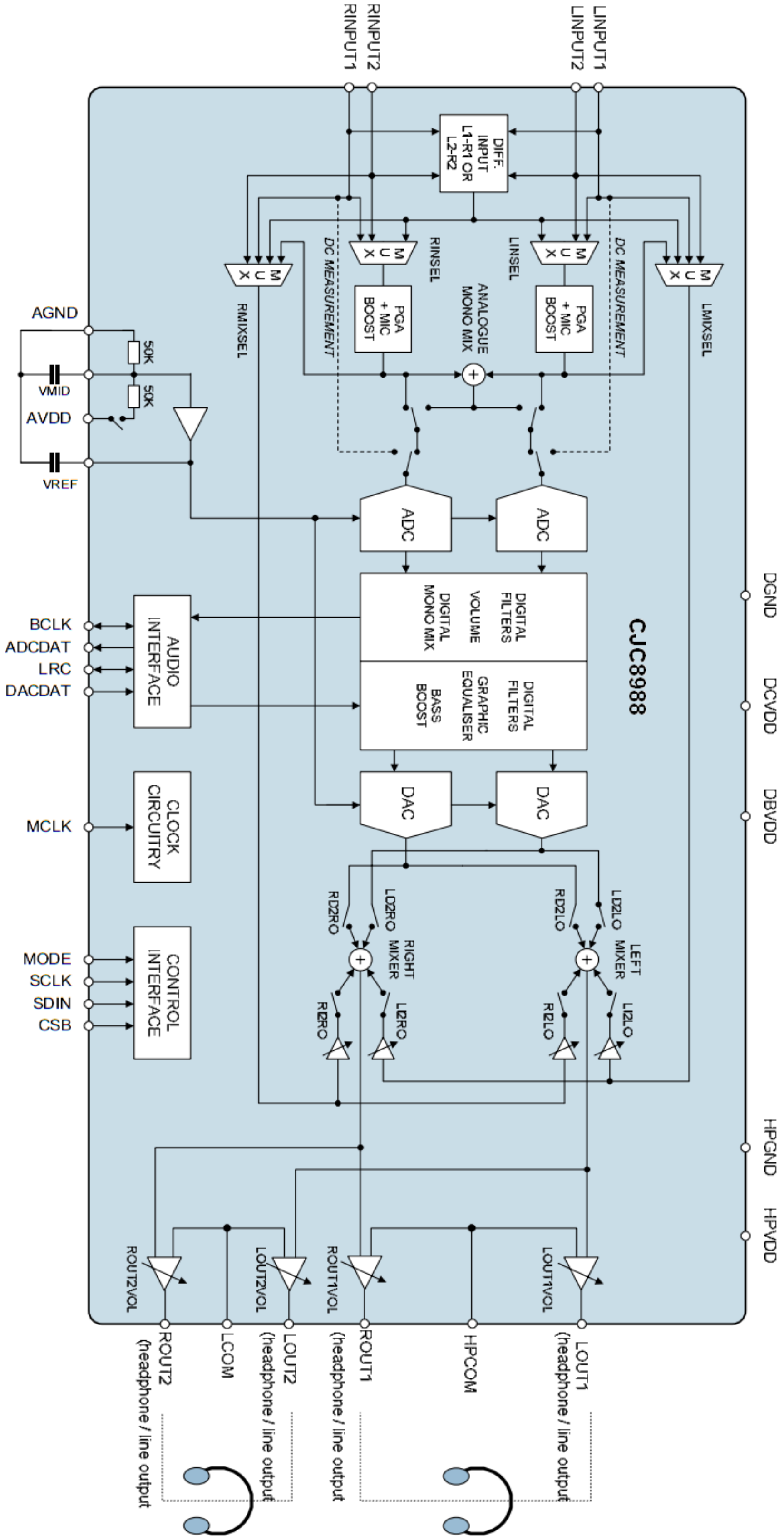
2. FEATURES

- DAC SNR 93dB ('A' weighted), THD –87dB at 48kHz, 1.8V
- ADC SNR 91dB ('A' weighted), THD -81dB at 48kHz, 1.8V
- 2x On-chip Headphone Drivers
  -THD –78dB , SNR 93dB with 16Ω load Hz, 1.8V
- Digital Graphic Equaliser
- Low Power
  -7.8mW stereo playback (1.8V supplies)
  -16.8mW record and playback (1.8V supplies)
- Low Supply Voltages
  -Analogue 1.8V to 3.3V
  -Digital core: 1.5V to 3.3V
  -Digital I/O: 1.8V to 3.3V
- 256fs / 384fs or USB master clock rates: 12MHz, 24MHz
- Audio sample rates: 8, 11.025, 16, 22.05, 24, 32, 44.1, 48,
- 88.2, 96kHz generated internally from master clock
- 4x4mm COL package

3. APPLICATIONS

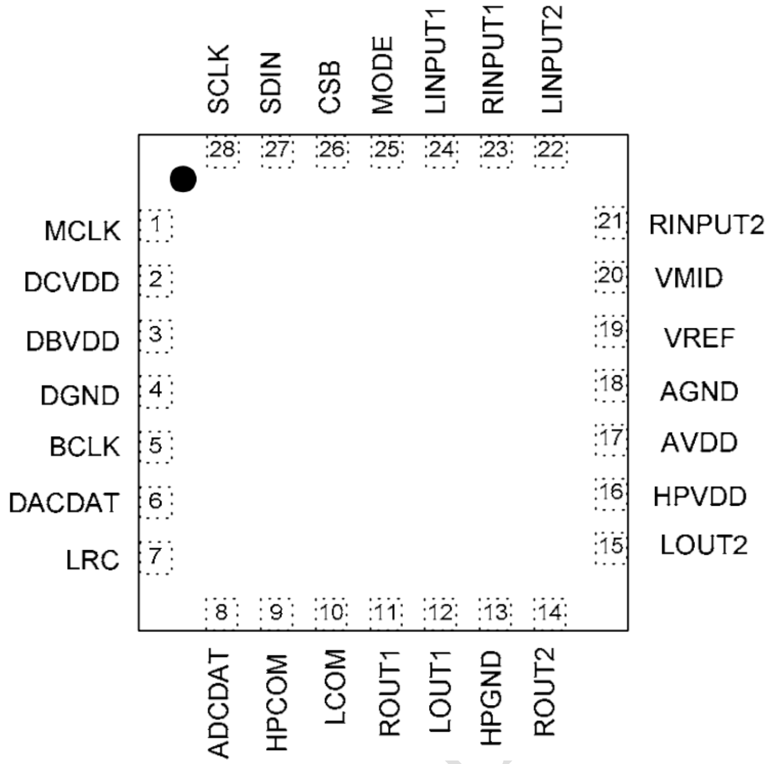
- Portable Multimedia players
- Multimedia handsets
- Handheld gaming

4. BLOCK DIAGRAM



5. TABLE OF CONTENTS

6. PIN CONFIGURATION AND DEVICE MARKING



7. PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
1	MCLK	Digital Input	Master Clock
2	DCVDD	Supply	Digital Core Supply
3	DBVDD	Supply	Digital Buffer (I/O) Supply
4	DGND	Supply	Digital Ground (return path for both DCVDD and DBVDD)
5	BCLK	Digital Input / Output	Audio Interface Bit Clock
6	DACDAT	Digital Input	DAC Digital Audio Data
7	LRC	Digital Input / Output	Audio Interface Left / Right Clock
8	ADCDAT	Digital Output	ADC Digital Audio Data
9	HPCOM	Analogue Input	LOUT1 and ROUT1 common mode feedback
10	LCOM	Analogue Input	LOUT2 and ROUT2 common mode feedback
11	ROUT1	Analogue Output	Right Output 1 (Line or Headphone)
12	LOUT1	Analogue Output	Left Output 1 (Line or Headphone)
13	HPGND	Supply	Supply for Analogue Output Drivers (LOUT1/2, ROUT1/2)
14	ROUT2	Analogue Output	Right Output 1 (Line or Headphone)
15	LOUT2	Analogue Output	Left Output 1 (Line or Headphone)
16	HPVDD	Supply	Supply for Analogue Output Drivers (LOUT1/2, ROUT1/2, MONOUT)
17	AVDD	Supply	Analogue Supply
18	AGND	Supply	Analogue Ground (return path for AVDD)
19	VREF	Analogue Output	Reference Voltage Decoupling Capacitor
20	VMID	Analogue Output	Midrail Voltage Decoupling Capacitor
21	RINPUT2	Analogue Input	Right Channel Input 2
22	LINPUT2	Analogue Input	Left Channel Input 2
23	RINPUT1	Analogue Input	Right Channel Input 1
24	LINPUT1	Analogue Input	Left Channel Input 1
25	MODE	Digital Input	Control Interface Selection
26	CSB	Digital Input	Chip Select / Device Address Selection
27	SDIN	Digital Input / Output	Control Interface Data Input / 2-wire Acknowledge output
28	SCLK	Digital Input	Control Interface Clock Input

8. ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuous operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically to damage from excessive static voltages. Proper ESD precautions must be taken during handling of this device.

Chinaic Semiconductor tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30 ℃ / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30 ℃ / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30 ℃ / 60% Relative Humidity. Supplied in moisture barrier bag.
The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltages	**-0.3V**	**+3.6V**
Voltage range digital inputs	**DGND -0.3V**	**DBVDD +0.3V**
Voltage range analogue inputs	**AGND -0.3V**	**AVDD +0.3V**
Operating temperature range, TA	**-25 ℃**	**+85 ℃**
Storage temperature after soldering	**-65 ℃**	**+150 ℃**

Notes:

1. Analogue and digital grounds must always be within 0.3V of each other.
2. All digital and analogue supplies are completely independent from each other.
3. DCVDD must be less than or equal to AVDD and DBVDD.

9. RECOMMENDED OPERATION CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital supply range (Core)	**DCVDD**	**1.5**		**3.3**	**V**
Digital supply range (Buffer)	**DBVDD**	**1.8**		**3.3**	**V**
Analogue supplies range	**AVDD, HPVDD**	**1.8**		**3.3**	**V**
Ground	**DGND,AGND, HPGND**		**0**		**V**

10. ELECTRICAL CHARACTERISTICS

Test Conditions

DCVDD = DBVDD = AVDD = HPVDD =1.8V , TA = +25℃, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Inputs (LINPUT1, RINPUT1, LINPUT2, RINPUT2) to ADC out						
Full Scale Input Signal Level (for ADC 0dB Input at 0dB Gain)	**VINFS**	**AVDD = 2.4V**	**0.690**	**0.727**	**0.763**	**Vrms**
		AVDD = 1.8V	**0.480**	**0.545**	**0.610**	
Input Resistance	**RIN**	**L/RINPUT1 to ADC, PGA gain = 0dB**	**16**	**22**		**kΩ**
		L/RINPUT1 to ADC, PGA gain = +30dB	**1.5**	**2.8**		
		L/RINPUT2 to ADC PGA gain = 0dB	**16**	**22**		
		L/RINPUT2 to ADC PGA gain = 30dB	**1.5**	**2.8**		
Input Capacitance				**10**		**pF**
Signal to Noise Ratio (A-weighted)	**SNR**	**AVDD = 2.4V**		**93**		**dB**
		AVDD = 1.8V		**91**		
Total Harmonic Distortion + Noise	**THD+N**	**-6dBr input, AVDD = 2.4V**		**-84**		**dB**
		-1dBr input, AVDD = 1.8V		**-81**		
ADC Channel Separation		**min**		**89**		**dB**
		1kHz signal		**116**		
Analogue Outputs (LOUT1/2, ROUT1/2)						
0dB Full scale output voltage	**VOUTFS**	**AVDD = 2.4V**	**0.690**	**0.727**	**0.763**	**Vrms**
		AVDD = 1.8V	**0.507**	**0.545**	**0.583**	
Signal to Noise Ratio (A-weighted)	**SNR**	**AVDD = 2.4V**		**96**		**dB**
		AVDD = 1.8V		**93**		
Total Harmonic Distortion + Noise	**THD+N**	**-0dBr input, AVDD = 2.4V**		**86**		**dB**
		-2dBr input, AVDD = 2.4V		**88**		
		-0dBr input, AVDD = 1.8V		**78**		
		-4dBr input, AVDD = 1.8V		**85**		

Test Conditions

DCVDD = DBVDD = AVDD = HPVDD =1.8V , TA = +25 ℃, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Headphone Output (LOUT1/ROUT1, LOUT2/ROUT2 AC coupled to load)						
Total Harmonic Distortion + Noise	**THD+N**	**HPVDD=2.4V, RL=16 Ω PO=5mW HPCOM=LCOM=1 DACMIXBIAS=1**		**77**		**dB**
		HPVDD=1.8V, RL=16 Ω PO=5mW HPCOM=LCOM=0 DACMIXBIAS=1		**78**		**dB**
Signal to Noise Ratio (A-weighted)	**SNR**	**HPVDD=2.4V, HPCOM=LCOM=1 DACMIXBIAS=1**		**90**		**dB**
		HPVDD=1.8V, HPCOM=LCOM=0 DACMIXBIAS=0		**93**		**dB**
Analogue Reference Levels						
Midrail Reference Voltage	**VMID**		**–3%**	**AVDD/2**	**+3%**	**V**
Buffered Reference Voltage	**VREF**		**–3%**	**AVDD/2**	**+3%**	**V**
Digital Input / Output						
Input HIGH Level	**VIH**		**0.7×DBVDD**			**V**
Input LOW Level	**VIL**				**0.3×DBVDD**	**V**
Output HIGH Level	**VOH**	**IOH = +1mA**	**0.9×DBVDD**			**V**
Output LOW Level	**VOL**	**IOL = -1mA**			**0.1×DBVDD**	**V**

Test Conditions

DCVDD = DBVDD = AVDD = HPVDD =1.8V , TA = +25 ℃ , 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to Line-Out (L/ROUT1 or L/ROUT2 with 10kΩ load)						
Signal to Noise Ratio (A-weighted)	**SNR**	**AVDD = 2.4V HPCOM=LCOM=1**		**96**		**dB**
		AVDD=1.8V HPCOM=LCOM=0		**93**		
Total Harmonic Distortion + Noise	**THD+N**	**AVDD = 2.4V HPCOM=LCOM=1**		**86**		**dB**
		AVDD=1.8V HPCOM=LCOM=0		**87**		
Channel Separation		**min**		**102**		**dB**
		1kHz signal		**110**		

11. POWER CONSUMPTION

The power consumption of the CJC8988 depends on the following factors.

- Supply voltages: Reducing the supply voltages also reduces supply currents, and therefore results in significant power savings, especially in the digital sections of the CJC8988.

- Operating mode: Significant power savings can be achieved by always disabling parts of the CJC8988 that are not used (e.g. mic pre-amps, unused outputs, DAC, ADC, etc.)

AVDD=HPVDD=DCVDD=DBVDD=1.8V									
MODE	DACMIX BIAS	VSEL	ADC OSR	DAC OSR	AVDD	HP VDD	DC VDD	DB VDD	UNIT
playback	1	11	1	1	1.639	0.318	1.16	0.104	mA
	0	0	0	0	2.361	0.558	1.216	0.187	
	0	1	0	0	2.359	0.455	1.219	0.187	
	0	10	0	0	2.354	0.351	1.219	0.187	
	1	0	0	0	2.08	0.558	1.229	0.187	
	0	11	0	0	2.326	0.351	1.2	0.187	
record & playback	0	0	0	0	6.511	0.558	2	0.206	mA
	0	1	0	0	6.516	0.455	1.98	0.206	
	0	10	0	0	6.488	0.351	1.99	0.206	
	1	11	1	1	4.437	0.351	1.84	0.123	
	0	11	1	1	4.7	0.351	1.79	0.123	
	0	11	0	0	6.341	0.351	1.952	0.206	

Notes:

1. All figures are at TA = +25 ℃, Slave Mode, fs = 48kHz, MCLK = 12.288 MHz (256fs),
2. The power dissipated in the headphone is not included in the above table.

12. SIGNAL TIMING REQUIREMENTS

12.1. SYSTEM CLOCK TIMING

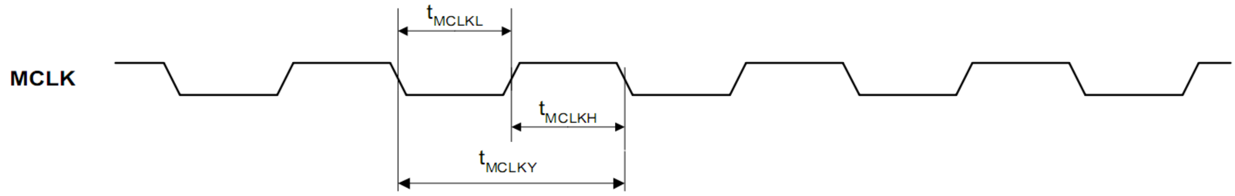


Figure 1 System Clock Timing Requirements

Test Conditions

CLKDIV2=0, DCVDD = 1.8V, DBVDD = 1.8V, DGND = 0V, TA = +25℃, Slave Mode fs = 48kHz, MCLK = 384fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
System Clock Timing Information					
MCLK System clock pulse width high	**TMCLKL**	**21**			**ns**
MCLK System clock pulse width low	**TMCLKH**	**21**			**ns**
MCLK System clock cycle time	**TMCLKY**	**54**			**ns**
MCLK duty cycle	**TMCLKDS**	**60:40**		**40:60**	**ns**

Test Conditions

CLKDIV2=1, DCVDD = 1.8V, DBVDD = 1.8V, DGND = 0V, TA = +25 C, Slave Mode fs = 48kHz, MCLK = 384fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
System Clock Timing Information					
MCLK System clock pulse width high	**TMCLKL**	**10**			**ns**
MCLK System clock pulse width low	**TMCLKH**	**10**			**ns**
MCLK System clock cycle time	**TMCLKY**	**27**			**ns**

12.2.AUDIO INTERFACE TIMING – MASTER MODE

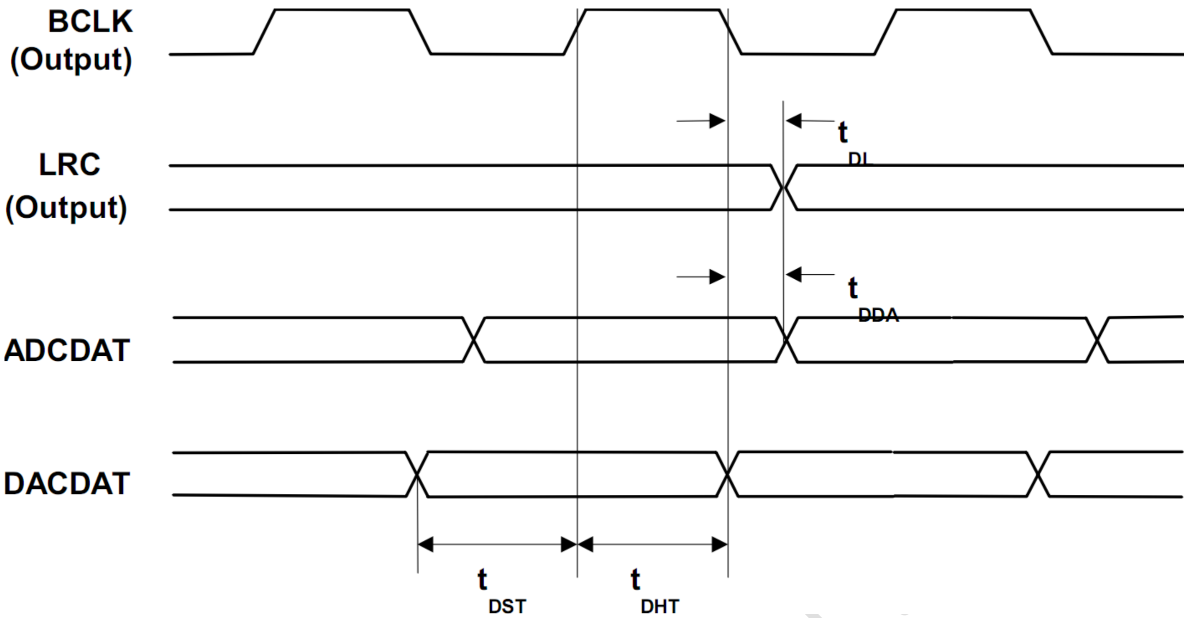


Figure 2 Digital Audio Data Timing – Master Mode

Test Conditions

DCVDD = 1.8V, DBVDD = 1.8V, DGND = 0V, TA = +25 C, Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Bit Clock Timing Information					
BCLK rise time (10pF load)	**tBCLKR**			**3**	**ns**
BCLK fall time (10pF load)	**tBCLKF**			**3**	**ns**
BCLK duty cycle (normal mode, BCLK = MCLK/n)	**tBCLKDS**		**50:50**		
BCLK duty cycle (USB mode, BCLK = MCLK)	**tBCLKDS**		**Tmclkds**		
Audio Data Input Timing Information					
DACLRC propagation delay from BCLK falling edge	**tDL**			**10**	**ns**
ADCDAT propagation delay from BCLK falling edge	**tDDA**			**10**	**ns**
DACDAT setup time to BCLK rising edge	**tDST**	**10**			**ns**
DACDAT hold time from BCLK rising edge	**tDHT**	**10**			**ns**

12.3.AUDIO INTERFACE TIMING – SLAVE MODE

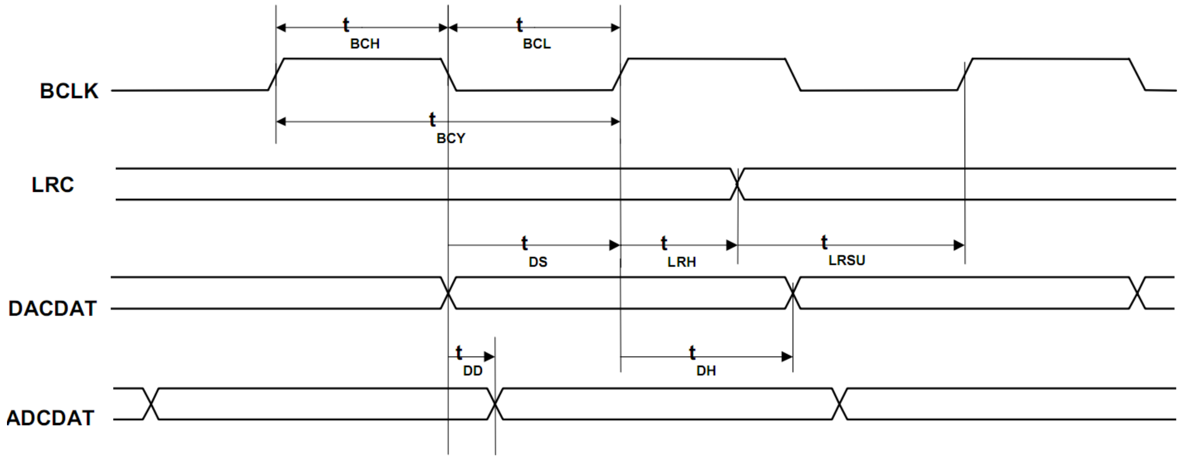


Figure 3 Digital Audio Data Timing – Slave Mode

Test Conditions

DCVDD = 1.8V, DBVDD = 1.8V, DGND = 0V, TA = +25 C, Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
BCLK cycle time	**tBCY**	**50**			**ns**
BCLK pulse width high	**tBCH**	**20**			**ns**
BCLK pulse width low	**tBCL**	**20**			**ns**
DACLRC set-up time to BCLK rising edge	**tLRSU**	**10**			**ns**
DACLRC hold time from BCLK rising edge	**tLRH**	**10**			**ns**
DACDAT hold time from BCLK rising edge	**tDH**	**10**			**ns**
ADCDAT propagation delay from BCLK falling edge	**tDD**			**10**	**ns**

Note:

BCLK period should always be greater than or equal to MCLK period.

12.4. CONTROL INTERFACE TIMING – 3-WIRE MODE

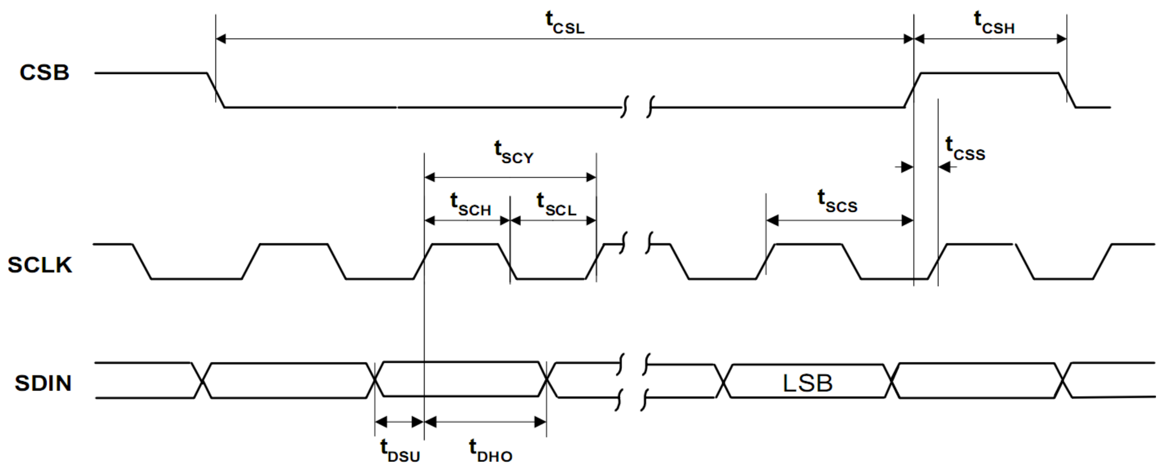


Figure 4 Control Interface Timing – 3-Wire Serial Control Mode

Test Conditions

DCVDD = 1.8V, DBVDD = 1.8V, DGND = 0V, TA = +25 C, Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK rising edge to CSB rising edge	**tSCS**	**80**			**ns**
SCLK pulse cycle time	**tSCY**	**200**			**ns**
SCLK pulse width low	**tSCL**	**80**			**ns**
SCLK pulse width high	**tSCH**	**80**			**ns**
SDIN to SCLK set-up time	**tDSU**	**40**			**ns**
SCLK to SDIN hold time	**tDHO**	**40**			**ns**
CSB pulse width low	**tCSL**	**40**			**ns**
CSB pulse width high	**tCSH**	**40**			**ns**
CSB rising to SCLK rising	**tCSS**	**40**			**ns**
Pulse width of spikes that will be suppressed	**tps**	**0**		**5**	**ns**

12.5. CONTROL INTERFACE TIMING – 2-WIRE MODE

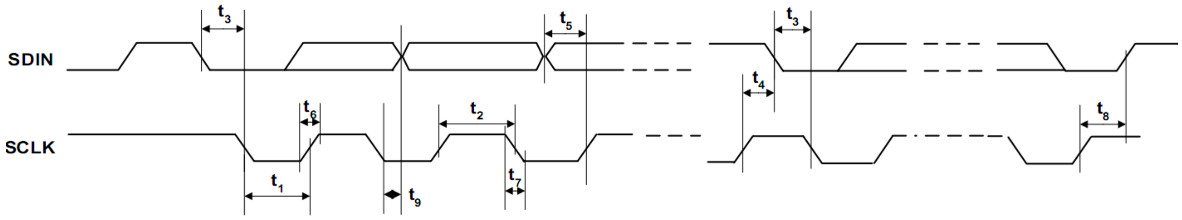


Figure 5 Control Interface Timing – 2-Wire Serial Control Mode

Test Conditions

DCVDD = 1.8V, DBVDD = 1.8V, DGND = 0V, TA = +25 C, Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK Frequency		**0**		**526**	**KHZ**
SCLK Low Pulse-Width	**t1**	**1.3**			**us**
SCLK High Pulse-Width	**t2**	**600**			**ns**
Hold Time (Start Condition)	**t3**	**600**			**ns**
Setup Time (Start Condition)	**t4**	**600**			**ns**
Data Setup Time	**t5**	**100**			**ns**
SDIN, SCLK Rise Time	**t6**			**300**	**ns**
SDIN, SCLK Fall Time	**t7**			**300**	**ns**
Setup Time (Stop Condition)	**t8**	**600**			**ns**
Data Hold Time	**t9**			**900**	**ns**
Pulse width of spikes that will be suppressed	**tps**	**0**		**5**	**ns**

13. INTERNAL POWER ON RESET CIRCUIT

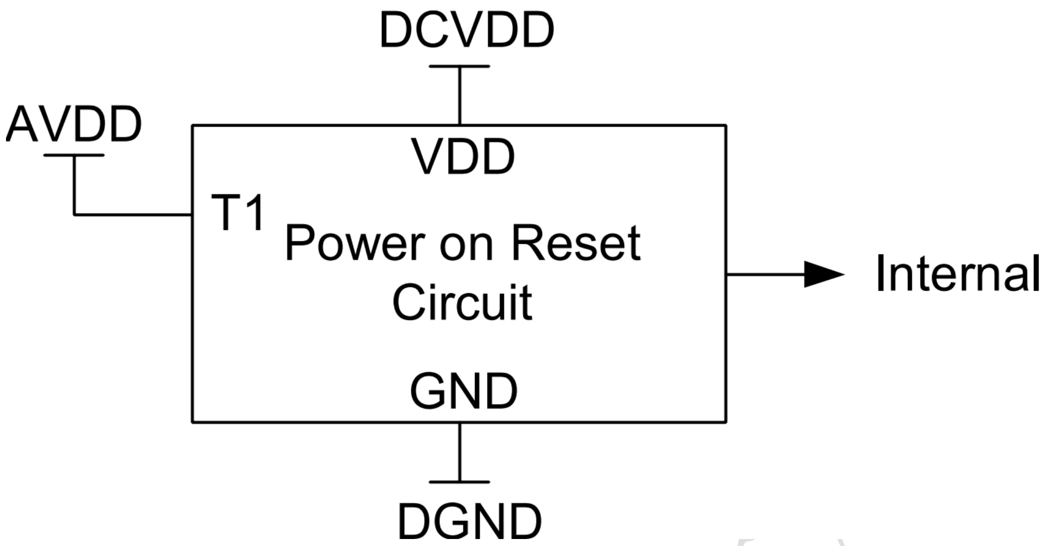


Figure 6 Internal Power on Reset Circuit Schematic

The CJC8988 includes an internal Power-On-Reset Circuit, as shown in Figure 6, which is used to reset the digital logic into a default state after power up. The power on reset circuit is powered from DCVDD and monitors DCVDD and AVDD. It asserts PORB low if DCVDD or AVDD are below a minimum threshold.

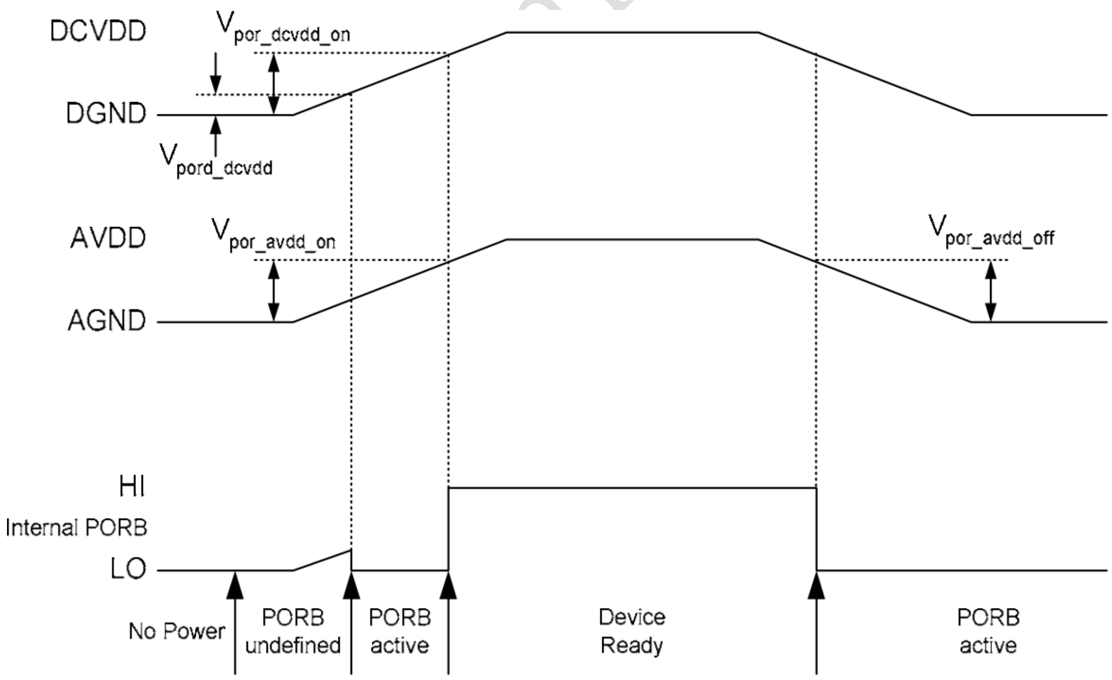


Figure 7 Typical Power-Up Sequence

Figure 7 shows a typical power-up sequence. When DCVDD and AVDD rise above the minimum thresholds, Vpord_dcvdd and Vpord_avdd, there is enough voltage for the circuit to guarantee the Power on Reset is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. When DCVDD rises to Vpor_dcvdd_on and AVDD rises to Vpor_avdd_on, PORB is released high and all registers are in their default state and writes to the control interface may take place. If DCVDD and AVDD rise at different rates then PORB will only be released when DCVDD and AVDD have both exceeded the Vpor_dcvdd_on and Vpor_avdd_on thresholds.

On power down, PORB is asserted low whenever DCVDD drops below the minimum threshold Vpor_dcvdd_off or AVDD drops below the minimum threshold Vpor_avdd_off.

SYMBOL	MIN	TYP	MAX	UNIT
Vpord_dcvdd	**0.4**	**0.6**	**0.8**	**V**
Vpor_dcvdd_on	**0.9**	**1.26**	**1.6**	**V**
Vpor_avdd_on	**0.5**	**0.7**	**0.9**	**V**
Vpor_avdd_off	**0.4**	**0.6**	**0.8**	**V**

Table 3 Typical POR Operation (typical values, not tested)

14. DEVICE DESCRIPTION

14.1. INTRODUCTION

The CJC8988 is a low power audio codec offering a combination of high quality audio, advanced features, low power and small size. These characteristics make it ideal for portable digital audio applications such as MP3 and minidisk player / recorders. Stereo 24-bit multi-bit delta sigma ADCs and DACs are used with oversampling digital interpolation and decimation filters.

The device includes three stereo analogue inputs that can be switched internally. Each can be used as either a line level input or microphone input and LINPUT1/RINPUT1 and LINPUT2/RINPUT2 can be configured as mono differential inputs. The on-chip stereo ADC and DAC are of a high quality using a multi-bit, low-order oversampling architecture to deliver optimum performance with low power consumption.

The DAC output signal first enters an analogue mixer where an analogue input can be added to it. This mix is available on line and headphone outputs.

The CJC8988 has a configurable digital audio interface where ADC data can be read and digital audio playback data fed to the DAC. It supports a number of audio data formats including I2 S, DSP Mode (a burst mode in which frame sync plus 2 data packed words are transmitted), MSB-First, left justified and and can operate in master or slave modes.

The CJC8988 uses a unique clocking scheme that can generate many commonly used audio sample rates from either a 12.00MHz USB clock or an industry standard 256/384 fs clock. This feature eliminates the common requirement for an external phase-locked loop (PLL) in applications where the master clock is not an integer multiple of the sample rate. Sample rates of 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz, 88.2kHz and 96kHz can be generated.

The digital filters used for recording and playback are optimised for each sampling rate used.

To allow full software control over all its features, the CJC8988 offers a choice of 2 or 3 wire MPU control interface. It is fully compatible and an ideal partner for a wide range of industry standard microprocessors, controllers and DSPs.

The design of the CJC8988 has given much attention to power consumption without compromising performance. It operates at very low voltages, and includes the ability to power off parts of the circuitry under software control, including standby and power off modes.

14.2. INPUT SIGNAL PATH

The input signal path for each channel consists of a switch to select between three analogue inputs, followed by a PGA (programmable gain amplifier) and an optional microphone gain boost. A differential input of either (LINPUT1 – RINPUT1) or (LINPUT2 – RINPUT2) may also be selected. The gain of the PGA can be controlled either by the user.

The signal then enters an ADC where it is digitised. Alternatively, the two channels can also be mixed in the analogue domain and digitised in one ADC while the other ADC is switched off. The mono-mix signal appears on both digital output channels.

14.3. SIGNAL INPUTS

The CJC8988 has two sets of high impedance, low capacitance AC coupled analogue inputs, LINPUT1/RINPUT1 and LINPUT2/RINPUT2. Inputs can be configured as microphone or line level by enabling or disabling the microphone gain boost.

LINSEL and RINSEL control bits (see Table 4) are used to select independently between external inputs and internally generated differential products (LINPUT1-RINPUT1 or LINPUT2-RINPUT2). The choice of differential signal, LINPUT1-RINPUT1 or LINPUT2-RINPUT2 is made using DS (refer to Table 6).

As an example, the CJC8988 can be set up to convert one differential and one single ended mono signal by applying the differential signal to LINPUT1/RINPUT1 and the single ended signal to RINPUT2. By setting LINSEL to L-R Differential (see Table 4), DS to LINPUT1 – RINPUT1 (see Table 6) and RINSEL to RINPUT2, each mono signal can then be routed to a separate ADC or Bypass path.

The signal inputs are biased internally to the reference voltage VREF. Whenever the line inputs are muted or the device placed into standby mode, the inputs are kept biased to VREF using special anti-thump circuitry. This reduces any audible clicks that may otherwise be heard when changing inputs.

14.4. DC MEASUREMENT

For DC measurements (for example, battery voltage monitoring), the input signal at the LINPUT1 and/or RINPUT1 pins can be taken directly into the respective ADC, bypassing both PGA and microphone boost. The ADC output then becomes unsigned relative to AVDD, instead of being a signed (two's complement) number relative to VREF. Setting L/RDCM will override L/RINSEL. The input range for dc measurement is AGND to AVDD.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R32 (20h) ADC Signal Path Control (Left)	7:6	LINSEL	00	Left Channel Input Select 00 = LINPUT1 01 = LINPUT2 10 = Reserved 11 = L-R Differential (either LINPUT1- RINPUT1 or LINPUT2-RINPUT2, selected by DS)
	5:4	LMIC BOOST	00	Left Channel Microphone Gain Boost 00 = Boost off (bypassed) 01 = 13dB boost 10 = 20dB boost 11 = 29dB boost
R33 (21h) ADC Signal Path Control (Right)	7:6	RINSEL	00	Right Channel Input Select 00 = RINPUT1 01 = RINPUT2 10 = Reserved 11 = L-R Differential (either LINPUT1- RINPUT1 or LINPUT2-RINPUT2, selected by DS)
	5:4	RMIC BOOST	00	Right Channel Microphone Gain Boost 00 = Boost off (bypassed) 01 = 13dB boost 10 = 20dB boost 11 = 29dB boost

Table 4 Input Software Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R31 (1Fh) ADC input Mode	5	RDCM	0	Right Channel DC Measurement 0 = Normal Operation, PGA Enabled 1 = Measure DC level on RINPUT1
	4	LDCM	0	Left Channel DC Measurement 0 = Normal Operation, PGA Enabled 1 = Measure DC level on LINPUT1

Table 5 DC Measurement Select

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R31 (1Fh) ADC input Mode	8	DS	0	Differential input select 0: LINPUT1 – RINPUT1 1: LINPUT2 – RINPUT2

Table 6 Differential Input Select

14.5. MONO MIXING

The stereo ADC can operate as a stereo or mono device, or the two channels can be mixed to mono, either in the analogue domain (i.e. before the ADC) or in the digital domain (after the ADC). MONOMIX selects the mode of operation. For analogue mono mix either the left or right channel ADC can be used, allowing the unused ADC to be powered off or used for a dc measurement conversion. The user also has the flexibility to select the data output from the audio interface using DATSEL. The default is for left and right channel ADC data to be output, but the interface may also be configured so that e.g. left channel ADC data is output as both left and right data for when an analogue mono mix is selected.

Note:
If DC measurement is selected this overrides the MONOMIX selection.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R31 (1Fh) ADC input Mode	7:6	MONOMIX [1:0]	00	00: Stereo 01: Analogue Mono Mix (using left ADC) 10: Analogue Mono Mix (using right ADC) 11: Digital Mono Mix

Table 7 Mono Mixing

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R23 (17h) Additional Control (1)	3:2	DATSEL [1:0]	00	00: left data=left ADC; right data =right ADC 01: left data =left ADC; right data = left ADC 10: left data = right ADC; right data =right ADC 11: left data = right ADC; right data = left ADC

Table 8 ADC Data Output Configuration

14.6. PGA CONTROL

The PGA matches the input signal level to the ADC input range. The PGA gain is logarithmically adjustable from +30dB to –17.25dB in 0.75dB steps. Each PGA can be controlled by the user.

The gain is independently adjustable on both Right and Left Line Inputs. Additionally, by controlling the register bits LIVU and RIVU, the left and right gain settings can be simultaneously updated. Setting the LZCEN and RZCEN bits enables a zero-cross detector which ensures that PGA gain changes only occur when the signal is at zero, eliminating any zipper noise. If zero cross is enabled a timeout is also available to update the gain if a zero cross does not occur. This function may be enabled by setting TOEN in register R23 (17h).

The inputs can also be muted in the analogue domain under software control. The software control registers are shown in Table 9.If zero crossing is enabled, it is necessary to enable zero cross timeout to un-mute the input PGAs.This is because their outputs will not cross zero when muted. Alternatively, zero cross can be disabled before sending the un-mute command.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 (00h) Left Channel PGA	8	LIVU	0	Left Volume Update 0 = Store LINVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = LINVOL, right = intermediate latch)
	7	LINMUTE	1	Left Channel Input Analogue Mute 1 = Enable Mute 0 = Disable Mute Note: LIVU must be set to un-mute.
	6	LZCEN	0	Left Channel Zero Cross Detector 1 = Change gain on zero cross only 0 = Change gain immediately
	5:0	LINVOL [5:0]	010111 (0dB)	Left Channel Input Volume Control 111111 = +30dB 111110 = +29.25dB . . 0.75dB steps down to 000000 = -17.25dB
R1 (01h) Right Channel PGA	8	RIVU	0	Right Volume Update 0 = Store RINVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (right = RINVOL, left = intermediate latch)
	7	RINMUTE	1	Right Channel Input Analogue Mute 1 = Enable Mute 0 = Disable Mute Note: RIVU must be set to un-mute.
	6	RZCEN	0	Right Channel Zero Cross Detector 1 = Change gain on zero cross only 0 = Change gain immediately
	5:0	RINVOL [5:0]	010111 (0dB)	Right Channel Input Volume Control 111111 = +30dB 111110 = +29.25dB . . 0.75dB steps down to 000000 = -17.25dB
R23 (17h) Additional Control (1)	0	TOEN	0	Timeout Enable 0 : Timeout Disabled 1 : Timeout Enabled

Table 9 Input PGA Software Control

14.7. ANALOGUE TO DIGITAL CONVERTER (ADC)

The CJC8988 uses a multi-bit, oversampled sigma-delta ADC for each channel. The use of multi-bit feedback and high oversampling rates reduces the effects of jitter and high frequency noise. The ADC Full Scale input level is proportional to AVDD. With a 1.8V supply voltage, the full scale level is 1.0 Volts r.m.s. Any voltage greater than full scale may overload the ADC and cause distortion.

14.8. ADC DIGITAL FILTER

The ADC filters perform true 24 bit signal processing to convert the raw multi-bit oversampled data from the ADC to the correct sampling frequency to be output on the digital audio interface. The digital filter path is illustrated in Figure 8.

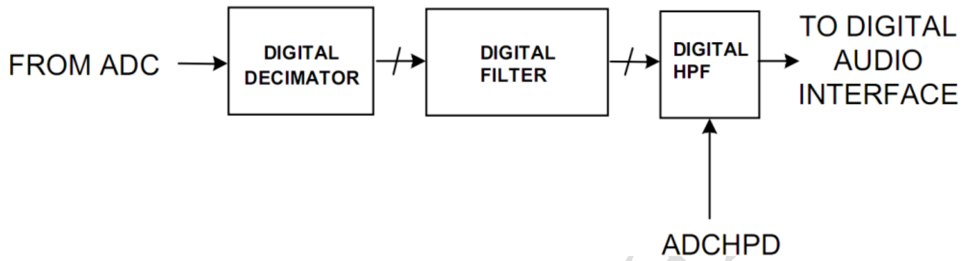


Figure 8 ADC Digital Filter

The ADC digital filters contain a digital high-pass filter, selectable via software control. The high-pass filter response is detailed in the Digital Filter Characteristics section. When the high-pass filter is enabled the DC offset is continuously calculated and subtracted from the input signal. By setting HPOR, the last calculated DC offset value is stored when the high-pass filter is disabled and will continue to be subtracted from the input signal. If the DC offset is changed, the stored and subtracted value will not change unless the high-pass filter is enabled. This feature can be used for calibration purposes. In addition the high-pass filter may be enabled separately on the left and right channels (see Table 11).

The output data format can be programmed by the user to accommodate stereo or monophonic recording on both inputs. The polarity of the output signal can also be changed under software control. The software control is shown in Table 10.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) ADC and DAC Control	6:5	ADCPOL [1:0]	00	00 = Polarity not inverted 01 = L polarity invert 10 = R polarity invert 11 = L and R polarity invert
	4	HPOR	0	Store dc offset when high-pass filter disabled 1 = store offset 0 = clear offset
	0	ADCHPD	0	ADCHPD and HPFLREN together determine high-pass filter behaviour (see Table 11)
R27 (1Bh)	5	HPFLREN	0	

Table 10 ADC Signal Path Control

HPFLREN	ADCHPD	LEFT CHANNEL	RIGHT CHANNEL
0	**0**	**HPF**	**ON**
0	**1**	**HPF**	**OFF**
1	**0**	**HPF**	**ON**
1	**1**	**HPF**	**OFF**

Table 11 ADC High Pass Filter Modes

14.9. DIGITAL ADC VOLUME CONTROL

The output of the ADCs can be digitally amplified or attenuated over a range from –97dB to +30dB in 0.5dB steps. The volume of each channel can be controlled separately. The gain for a given eight-bit code X is given by:

0.5 × (X-195) dB for 1 ≤ X ≤ 255; MUTE for X = 0

The LAVU and RAVU control bits control the loading of digital volume control data. When LAVU or RAVU are set to 0, the LADCVOL or RADCVOL control data will be loaded into the respective control register, but will not actually change the digital gain setting. Both left and right gain settings are updated when either LAVU or RAVU are set to 1. This makes it possible to update the gain of both channels simultaneously.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R21 (15h) Left ADC Digital Volume	7:0	LADCVOL [7:0]	11000011 (0dB)	Left ADC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -97dB 0000 0010 = -96.5dB ... 0.5dB steps up to 1111 1111 = +30dB
	8	LAVU	0	Left ADC Volume Update 0 = Store LADCVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = LADCVOL, right = intermediate latch)
R22 (16h) Right ADC Digital Volume	7:0	RADCVOL [7:0]	11000011 (0dB)	Right ADC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -97dB 0000 0010 = -96.5dB ... 0.5dB steps up to 1111 1111 = +30dB
	8	RAVU	0	Right ADC Volume Update 0 = Store RADCVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = intermediate latch, right = RADCVOL)

Table 12 ADC Digital Volume Control

14.10. 3D STEREO ENHANCEMENT

The CJC8988 has a digital 3D enhancement option to artificially increase the separation between the left and right channels. This effect can be used for recording or playback, but not for both simultaneously. Selection of 3D for record or playback is controlled by register bit MODE3D.

Important:

Switching the 3D filter from record to playback or from playback to record may only be done when ADC and DAC are disabled. The CJC8988 control interface will only allow MODE3D to be changed when ADC and DAC are disabled (i.e. bits ADCL, ADCR, DACL and DACR in reg. 26 / 1Ah are all zero).

The 3D enhancement function is activated by the 3DEN bit, and has two programmable parameters. The 3DDEPTH setting controls the degree of stereo expansion. Additionally, one of four filter characteristics can be selected for the 3D processing, using the 3DVC and 3DLC control bits.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16 (10h) 3D enhance	7	MODE3D	0	Playback/Record 3D select 0 = 3D selected for Record 1 = 3D selected for Playback
	6	3DUC	0	Upper Cut-off frequency 0 = High (2.2kHz at 48kHz sampling) 1 = Low (1.5kHz at 48kHz sampling)
	5	3DLC	0	Lower Cut-off frequency 0 = Low (200Hz at 48kHz sampling) 1 = High (500Hz at 48kHz sampling)
	4:1	3DDEPTH [3:0]	0000	Stereo depth 0000: 0% (minimum 3D effect) 0001: 6.67% .... 1110: 93.3% 1111: 100% (maximum 3D effect)
	0	3DEN	0	3D function enable 1: enabled 0: disabled

Table 15 3D Stereo Enhancement Function

When 3D enhancement is enabled (and/or the graphic equaliser for playback) it may be necessary to attenuate the signal by 6dB to avoid limiting. This is a user selectable function, enabled by setting ADCDIV2 for the record path and DACDIV2 for the playback path.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) ADC and DAC control	8	ADCDIV2	0	ADC 6dB attenuate enable 0 = disabled (0dB) 1 = -6dB enabled
	7	DACDIV2	0	DAC 6dB attenuate enable 0 = disabled (0dB) 1 = -6dB enabled

Table 16 ADC and DAC 6dB Attenuation Select

14.11. OUTPUT SIGNAL PATH

The CJC8988 output signal paths consist of digital filters, DACs, analogue mixers and output drivers. The digital filters and DACs are enabled when the CJC8988 is in 'playback only' or 'record and playback' mode. The mixers and output drivers can be separately enabled by individual control bits (see Analogue Outputs). Thus it is possible to utilise the analogue mixing and amplification provided by the CJC8988, irrespective of whether the DACs are running or not.

The CJC8988 receives digital input data on the DACDAT pin. The digital filter block processes the data to provide the following functions:

- Digital volume control
- Graphic equaliser and Dynamic Bass Boost
- Sigma-Delta Modulation

Two high performance sigma-delta audio DACs convert the digital data into two analogue signals (left and right). These can then be mixed with analogue signals from the LINPUT1/2 and RINPUT1/2 pins, and the mix is fed to the output drivers, LOUT1/ROUT1 and LOUT2/ROUT2.

- LOUT1/ROUT1: can drive a 16Ω or 32Ω stereo headphone or stereo line output.
- LOUT2/ROUT2: can drive a 16Ω or 32Ω stereo headphone or stereo line output

14.12. DIGITAL DAC VOLUME CONTROL

The signal volume from each DAC can be controlled digitally, in the same way as the ADC volume (see Digital ADC Volume Control). The gain and attenuation range is –127dB to 0dB in 0.5dB steps. The level of attenuation for an eight-bit code X is given by:

$$0.5 \times (X-255)\ dB \quad for \quad 1 \leqslant X \leqslant 255; \quad MUTE \quad for \quad X = 0$$

The LDVU and RDVU control bits control the loading of digital volume control data. When LDVU or RDVU are set to 0, the LDACVOL or RDACVOL control data is loaded into an intermediate register, but the actual gain does not change. Both left and right gain settings are updated simultaneously when either LDVU or RDVU are set to 1.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R10 (0Ah) Left Channel Digital Volume	8	LDVU	0	Left DAC Volume Update 0 = Store LDACVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = LDACVOL, right = intermediate latch)
	7:0	LDACVOL [7:0]	11111111 (0dB)	Left DAC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -127dB 0000 0010 = -126.5dB ... 0.5dB steps up to 1111 1111 = 0dB
R11 (0Bh) Right Channel Digital Volume	8	RDVU	0	Right DAC Volume Update 0 = Store RDACVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = intermediate latch, right = RDACVOL)
	8	RDVU	0	Right DAC Volume Update latch (no gain change) 1 = Update left and right channel gains (left = intermediate latch, right = RDACVOL)
	7:0	RDACVOL [7:0]	11111111 (0dB)	Right DAC Digital Volume Control similar to LDACVOL

Table 17 Digital Volume Control

14.13. GRAPHIC EQUALISER

The CJC8988 has a digital graphic equaliser and adaptive bass boost function. This function operates on digital audio data before it is passed to the audio DACs. Bass enhancement can take two different forms:

- Linear bass control: bass signals are amplified or attenuated by a user programmable gain. This is independent of signal volume, and very high bass gains on loud signals may lead to signal clipping.
- Adaptive bass boost: The bass volume is amplified by a variable gain. When the bass volume is low, it is boosted more than when the bass volume is high. This method is recommended because it prevents clipping, and usually sounds more pleasant to the human ear.

Treble control applies a user programmable gain, without any adaptive boost function. Bass and treble control are completely independent with separately programmable gains and filter characteristics.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION		
R12 (0Ch) Bass Control	7	BB	0	Bass Boost 0 = Linear bass control 1 = Adaptive bass boost		
	6	BC	11111111 (0dB)	Bass Filter Characteristic 0 = Low Cutoff (130Hz at 48kHz sampling) 1 = High Cutoff (200Hz at 48kHz sampling)		
	3:0	BASS [3:0]	1111 (Disabled)	Bass Intensity		
				Code	BB=0	BB=1
				0000	+9dB	15
				0001	+9dB	14
				0010	+7.5dB	13
				0011	+6dB	12
				0100	+4.5dB	11
				0101	+3dB	10
				0110	+1.5dB	9
				0111	0dB	8
				1000	-1.5dB	7
				1001	-3dB	6
				1010	-4.5dB	5
				1011	-6dB	4
				1100	-6dB	3
				1101	-6dB	2
				1110	-6dB	1
				1111	Bypass (OFF)	

R13 (0Dh) Treble Control	6	TC	0	Treble Filter Characteristic 0 = High Cutoff (8kHz at 48kHz sampling) 1 = Low Cutoff (4kHz at 48kHz sampling)
	3:0	TRBL [3:0]	1111 (Disabled)	Treble Intensity 0000 or 0001 = +9dB 0010 = +7.5dB ··· (1.5dB steps) 1011 to 1110 = -6dB 1111 = Disable

Table 18 Graphic Equaliser

14.14. DIGITAL TO ANALOGUE CONVERTER (DAC)

After passing through the graphic equaliser filters, digital 'de-emphasis' can be applied to the audio data if necessary (e.g. when the data comes from a CD with pre-emphasis used in the recording). De-emphasis filtering is available for sample rates of 48kHz, 44.1kHz and 32kHz.

The CJC8988 also has a Soft Mute function, which gradually attenuates the volume of the digital signal to zero. When removed, the gain will return to the original setting. This function is enabled by default. To play back an audio signal, it must first be disabled by setting the DACMU bit to zero.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) ADC and DAC control	2:1	DEEMP [1:0]	00	De-emphasis Control 11 = 48kHz sample rate 10 = 44.1kHz sample rate 01 = 32kHz sample rate 00 = No De-emphasis
	3	DACMU	1	Digital Soft Mute 1 = mute 0 = no mute (signal active)

Table 19 DAC Control

The digital audio data is converted to oversampled bit streams in the on-chip, true 24-bit digital interpolation filters.

The bitstream data enters two multi-bit, sigma-delta DACs, which convert them to high quality analogue audio signals.

The multi-bit DAC architecture reduces high frequency noise and sensitivity to clock jitter. It also uses a

Dynamic Element Matching technique for high linearity and low distortion. In normal operation, the left and right channel digital audio data is converted to analogue in two separate DACs.

However, it is also possible to disable one channel, so that the same signal (left or right) appears on both analogue output channels.

Additionally, there is a mono-mix mode where the two audio channels are mixed together digitally and then converted to analogue using only one DAC, while the other DAC is switched off.

The mono-mix signal can be selected to appear on both analogue output channels.

The DAC output defaults to non-inverted. Setting DACINV will invert the DAC output phase on both left and right channels.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R23 (17h) Additional Control (1)	5:4	DMONOMIX [1:0]	00	DAC mono mix 00: stereo 01: mono ((L+R)/2) into DACL, ‘0’ into DACR 10: mono ((L+R)/2) into DACR, ‘0’ into DACL 11: mono ((L+R)/2) into DACL and DACR
	1	DACINV	1	DAC phase invert 0 : non-inverted 1 : inverted

Table 20 DAC Mono Mix and Phase Invert Select

14.15. OUTPUT MIXERS

The CJC8988 provides the option to mix the DAC output signal with analogue line-in signals from the LINPUT1/2, RINPUT1/2 pins or a mono differential input (LINPUT1 – RINPUT1) or (LINPUT2 – RINPUT2), selected by DS (see Table 6) . The level of the mixed-in signals can be controlled with PGAs (Programmable Gain Amplifiers).

The mono mixer is designed to allow a number of signal combinations to be mixed, including the possibility of mixing both the right and left channels together to produce a mono output. To prevent overloading of the mixer when full-scale DAC left and right signals are input, the mixer inputs from the DAC outputs each have a fixed gain of -6dB. The bypass path inputs to the mono mixer have variable gain as determined by R38/R39 bits [6:4].

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R34 (22h) Left Mixer (1)	2:0	LMIXSEL	000	Left Input Selection for Output Mix 000 = LINPUT1 001 = LINPUT2 010 = Reserved 011 = Left ADC Input (after PGA / MICBOOST) 100 = Differential input
R36 (24h) Right Mixer(1)	2:0	RMIXSEL	000	Right Input Selection for Output Mix 000 = RINPUT1 001 = RINPUT2 010 = Reserved 011 = Right ADC Input (after PGA / MICBOOST) 100 = Differential input

Table 21 Output Mixer Signal Selection

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R34 (22h) Left Mixer Control (1)	8	LD2LO	0	Left DAC to Left Mixer 0 = Disable (Mute) 1 = Enable Path
	7	LI2LO	0	LMIXSEL Signal to Left Mixer 0 = Disable (Mute) 1 = Enable Path
	6:4	LI2LOVOL [2:0]	101 (-9dB)	LMIXSEL Signal to Left Mixer Volume 000 = +6dB ··· (3dB steps) 111 = -15dB
R35 (23h) Left Mixer Control (2)	8	RD2LO	0	Right DAC to Left Mixer 0 = Disable (Mute) 1 = Enable Path
	7	RI2LO	0	RMIXSEL Signal to Left Mixer 0 = Disable (Mute) 1 = Enable Path
	6:4	RI2LOVOL [2:0]	101 (-9dB)	RMIXSEL Signal to Left Mixer Volume 000 = +6dB ··· (3dB steps) 111 = -15dB

Table 22 Left Output Mixer Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R36 (24h) Right Mixer Control (1)	8	LD2RO	0	Left DAC to Right Mixer 0 = Disable (Mute) 1 = Enable Path
	7	LI2RO	0	LMIXSEL Signal to Right Mixer 0 = Disable (Mute) 1 = Enable Path
	6:4	LI2ROVOL [2:0]	101 (-9dB)	LMIXSEL Signal to Right Mixer Volume 000 = +6dB ··· (3dB steps) 111 = -15dB
R37 (25h) Right Mixer Control (2)	8	RD2RO	0	Right DAC to Right Mixer 0 = Disable (Mute) 1 = Enable Path
	7	RI2RO	0	RMIXSEL Signal to Right Mixer 0 = Disable (Mute) 1 = Enable Path
	6:4	RI2ROVOL [2:0]	101 (-9dB)	RMIXSEL Signal to Right Mixer Volume 000 = +6dB ··· (3dB steps) 111 = -15dB

Table 23 Right Output Mixer Control

14.16. ANALOGUE OUTPUTS

LOUT1/ROUT1 OUTPUTS

The LOUT1 and ROUT1 pins can drive a 16Ω headphone or a line output (see Headphone Output and Line Output sections, respectively). The signal volume on LOUT1 and ROUT1 can be independently adjusted under software control by writing to LOUT1VOL and ROUT1VOL, respectively. Note that gains over 0dB may cause clipping if the signal is large. Any gain setting below 0101111 (minimum) mutes the output driver. The corresponding output pin remains at the same DC level (the reference voltage on the VREF pin), so that no click noise is produced when muting or un-muting.

A zero cross detect on the analogue output may also be enabled when changing the gain setting to minimize audible clicks and zipper noise as the gain updates. If zero cross is enabled a timeout is also available to update the gain if a zero cross does not occur. This function may be enabled by setting TOEN in register R23 (17h).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h) LOUT1 Volume	8	LO1VU	0	Left Volume Update 0 = Store LOUT1VOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = LOUT1VOL, right = intermediate latch)
	7	LO1ZC	0	Left zero cross enable 1 = Change gain on zero cross only 0 = Change gain immediately
	6:0	LOUT1VOL [6:0]	1111001 (0dB)	LOUT1 Volume 1111111 = +6dB ··· (80 steps) 0110000 = -67dB 0111111 to 0000000 = Analogue MUTE
R3 (03h) ROUT1 Volume	8	RO1VU	0	Right Volume Update 0 = Store ROUT1VOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = intermediate latch, right = ROUT1VOL)
	7	RO1ZC	0	Right zero cross enable 1 = Change gain on zero cross only 0 = Change gain immediately
	6:0	ROUT1VOL [6:0]	1111001	ROUT1 Volume 1111111 = +6dB ··· (80 steps) 0110000 = -67dB 0111111 to 0000000 = Analogue MUTE

Table 24 LOUT1/ROUT1 Volume Control

14.17. LOUT1/ROUT1 COMMON GROUND FEEDBACK (HPCOM)

The LOUT1/ROUT1 outputs also have the option of incorporating common ground feedback from the output signal ground, via a connection to the HPCOM input. This common ground feedback signal should be AC-coupled via a 4.7uF capacitor for the headphone loads. AC coupling of these outputs if they are used as LINE level outputs requires similar 1 to 4.7uF AC coupling capacitors depending upon LINE load resistance.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24 (18h) HPCOM Control	7	HPCOMEN	0	Enables common mode feedback on LOUT1 and ROUT1 0: Disable Common Mode Feedback 1: Enable Common Mode Feedback

Table 25 HPCOM Control

14.18. LOUT2/ROUT2 OUTPUTS

The LOUT2 and ROUT2 output pins are essentially similar to LOUT1 and ROUT1, but they are independently controlled .

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R40 (28h) LOUT2 Volume	6:0	LOUT2VOL [6:0]	1111001 (0dB)	LOUT2 Volume 1111111 = +6dB ··· (80 steps) 0110000 = -67dB 0111111 to 0000000 = Analogue MUTE
	7	LO2ZC	0	Left zero cross enable 1 = Change gain on zero cross only 0 = Change gain immediately
	8	LO2VU	0	Same as LO1VU
R41 (29h) ROUT2 Volume	6:0	ROUT2VOL [6:0]	1111001 (0dB)	ROUT2 Volume 1111111 = +6dB ··· (80 steps) 0110000 = -67dB 0111111 to 0000000 = Analogue MUTE
	7	RO2ZC	0	Right zero cross enable 1 = Change gain on zero cross only 0 = Change gain immediately
	8	RO2VU	0	Same as RO1VU
R24 (18h) Additional Control (2)	4	ROUT2INV	0	ROUT2 Invert 0 = No Inversion (0 °phase shift) 1 = Signal inverted (180 °phase shift)

Table 26 LOUT2/ROUT2 Volume Control

14.19. LOUT2/ROUT2 COMMON GROUND FEEDBACK (LCOM)

The LOUT2/ROUT2 outputs also have the option of incorporating common ground feedback from the output signal ground, via a connection to the LCOM input. This common ground feedback signal should be AC-coupled via a 4.7uF capacitor for headphone loads. AC coupling of these outputs if they are used as LINE level outputs requires similar 1 to 4.7uF AC coupling capacitors depending upon LINE load resistance.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24 (18h) LCOM Control	8	LCOMEN	0	Enables common mode feedback on LOUT2 and ROUT2 0: Disable Common Mode Feedback 1: Enable Common Mode Feedback

Table 27 LCOM Control

14.20. ENABLING THE OUTPUTS

Each analogue output of the CJC8988 can be separately enabled or disabled. The analogue mixer associated with each output is powered on or off along with the output pin. All outputs are disabled by default. To save power, unused outputs should remain disabled.

Outputs can be enabled at any time, except when VREF is disabled (VR=0), as this may cause pop noise (see “Power Management” and “Applications Information” sections)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R26 (1Ah) Power Management (2)	6	LOUT1	0	LOUT1 Enable
	5	ROUT1	0	ROUT1 Enable
	4	LOUT2	0	LOUT2 Enable
	3	ROUT2	0	ROUT2 Enable
Note: All “Enable” bits are 1 = Enabled, 0 = Disabled				

Table 28 Analogue Output Control

Whenever an analogue output is disabled, it remains connected to VREF (pin 20) through a resistor. This helps to prevent pop noise when the output is re-enabled. The resistance between VREF and each output can be controlled using the VROI bit in register 27. The default is low (1.5kΩ), so that any capacitors on the outputs can charge up quickly at start-up. If a high impedance is desired for disabled outputs, VROI can then be set to 1, increasing the resistance to about 40Kω

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R27 (1Bh) Additional (1)	6	VROI	0	VREF to analogue output resistance 0: 1.5 kΩ 1: 40 kΩ

Table 29 Disabled Outputs to VREF Resistance

14.21. THERMAL SHUTDOWN

The headphone outputs can drive very large currents. To protect the CJC8988 from overheating a thermal shutdown circuit is included. If the device temperature reaches approximately 150 C and the thermal shutdown circuit is enabled (TSDEN = 1) then the headphone amplifiers (outputs OUT1L/R and OUT2L/R) will be disabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R23 (17h) Additional Control (1)	8	TSDEN	0	Thermal Shutdown Enable 0 : thermal shutdown disabled 1 : thermal shutdown enabled

Table 30 Thermal Shutdown

14.22. DIGITAL AUDIO INTERFACE

The digital audio interface is used for inputting DAC data into the CJC8988 and outputting ADC data from it. It uses four pins:

- ADCDAT: ADC data output
- DACDAT: DAC data input
- LRC: DAC and ADC data alignment clock
- BCLK: Bit clock, for synchronisation

The clock signals BCLK and LRC can be an output when the CJC8988 operates as a master, or an input when it is a slave (see Master and Slave Mode Operation, below).
Four different audio data formats are supported:

- Left justified
- I2S
- DSP mode

All four of these modes are MSB first. They are described in Audio Data Formats, below. Refer to the Electrical Characteristic section for timing information.

14.23. MASTER AND SLAVE MODE OPERATION

The CJC8988 can be configured as either a master or slave mode device. As a master device the CJC8988 generates BCLK, ADCLRC and DACLRC and thus controls sequencing of the data transfer on ADCDAT and DACDAT. In slave mode, the CJC8988 responds with data to clocks it receives over the digital audio interface. The mode can be selected by writing to the MS bit (see Table 23). Master and slave modes are illustrated below.

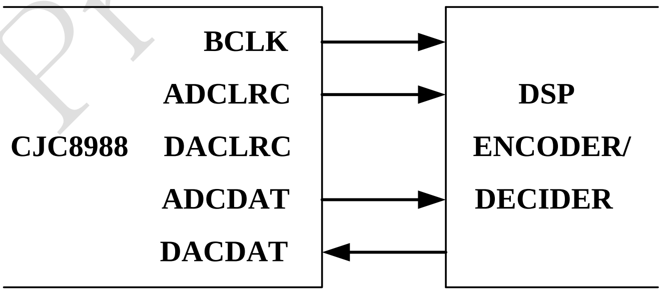


Figure 10 Master Mode

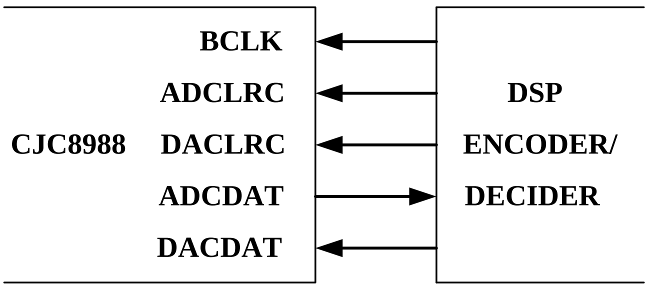


Figure 11 Slave Mode

14.24. AUDIO DATA FORMATS

In Left Justified mode, the MSB is available on the first rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRCLK transition

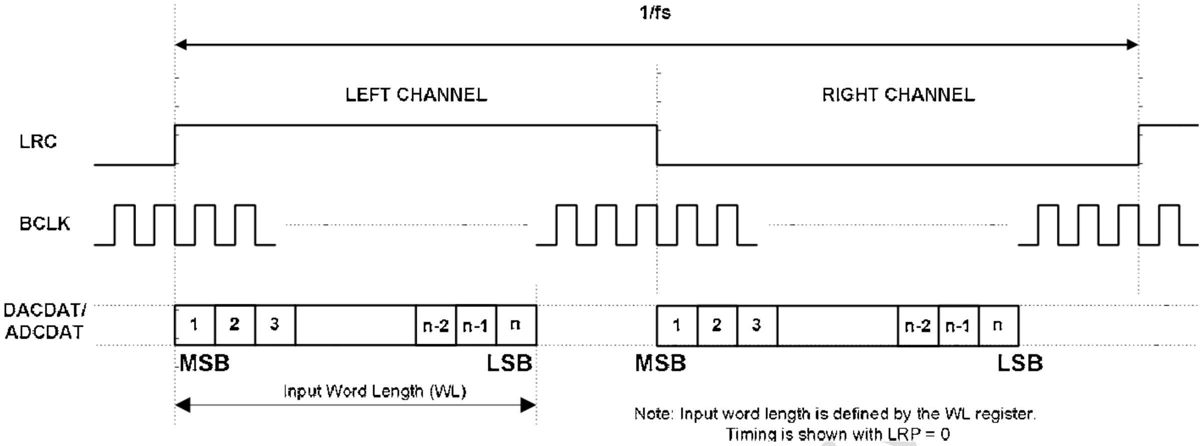


Figure 12 Left Justified Audio Interface (assuming n-bit word length)

In I2S mode, the MSB is available on the second rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

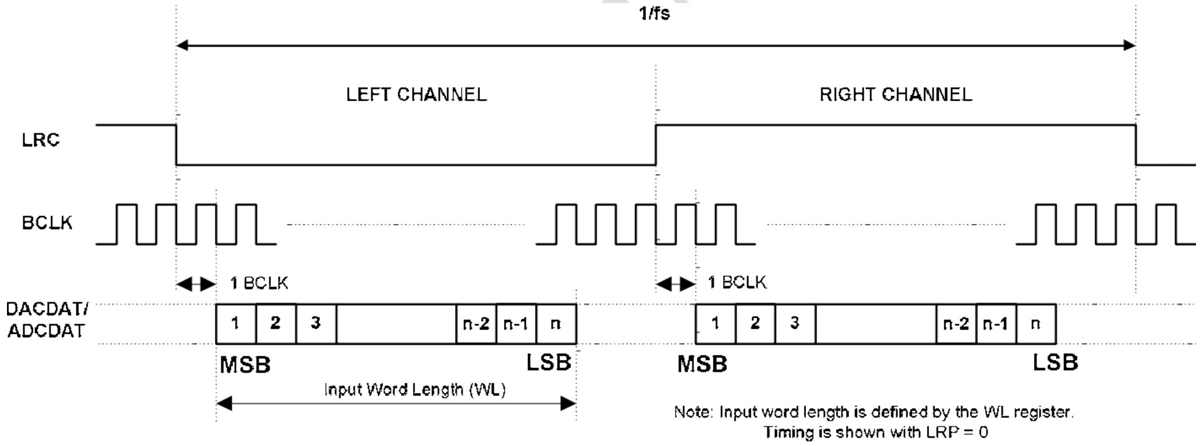


Figure 13 I2S Justified Audio Interface (assuming n-bit word length)

In DSP/PCM mode, the left channel MSB is available on either the 1 (mode B) or 2 (mode A) rising edge of BCLK (selectable by LRP) following a rising edge of LRC. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample. In device master mode, the LRC output will resemble the frame pulse shown in Figure 14 and Figure 15. In device slave mode, Figure 16 and Figure 17, it is possible to use any length of frame pulse

less than 1/fs, providing the falling edge of the frame pulse occurs greater than one BCLK period before the rising edge of the next frame pulse.

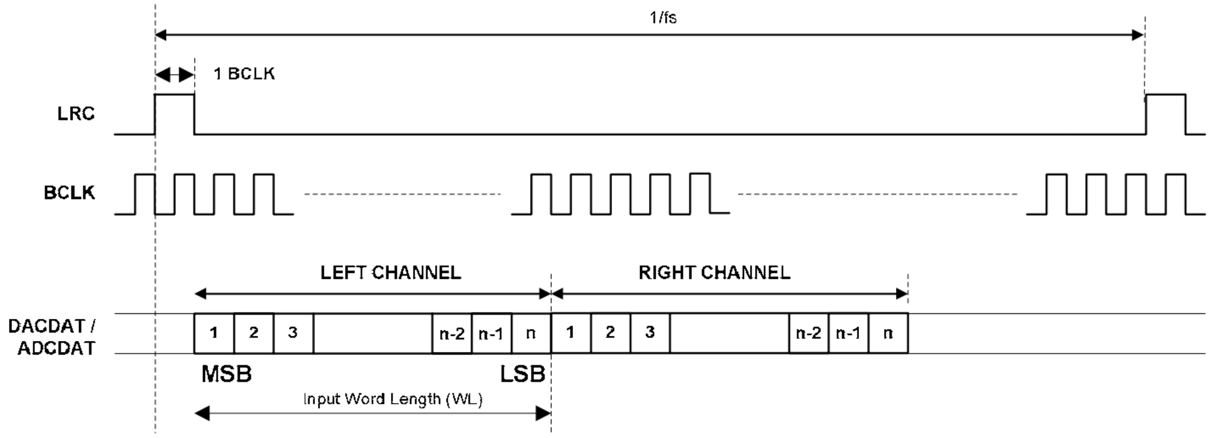


Figure 14 DSP/PCM Mode Audio Interface (mode A, LRP=0, Master)

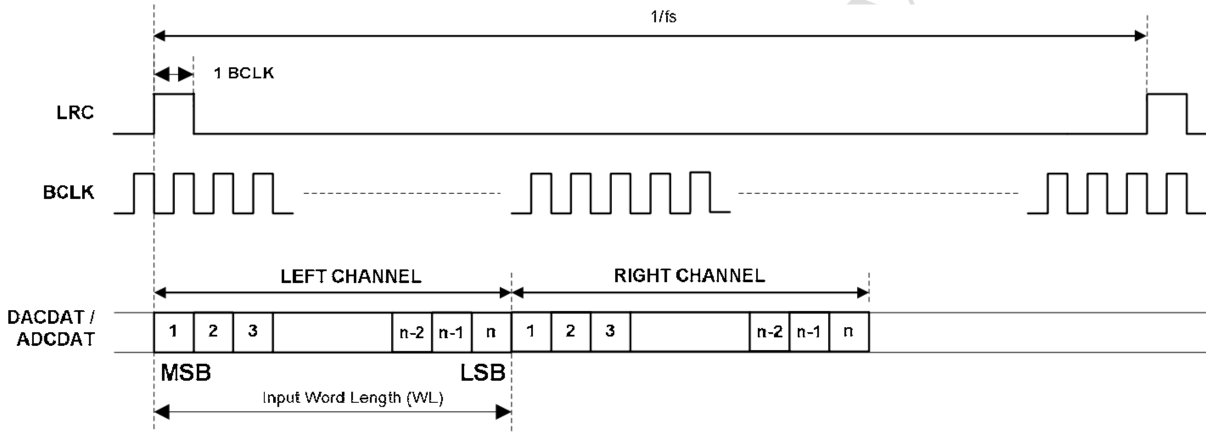


Figure 15 DSP/PCM Mode Audio Interface (mode B, LRP=1, Master)

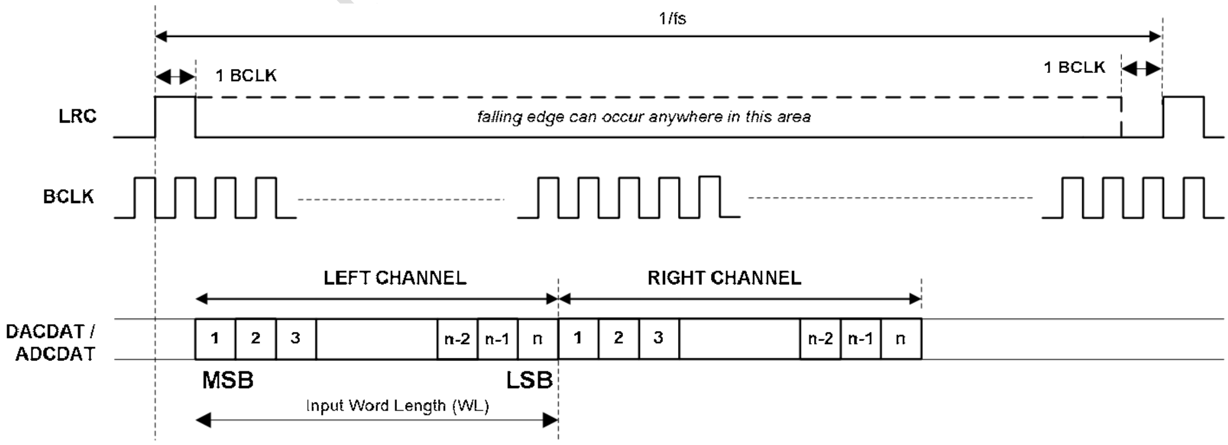


Figure 16 DSP/PCM Mode Audio Interface (mode A, LRP=0, Slave)

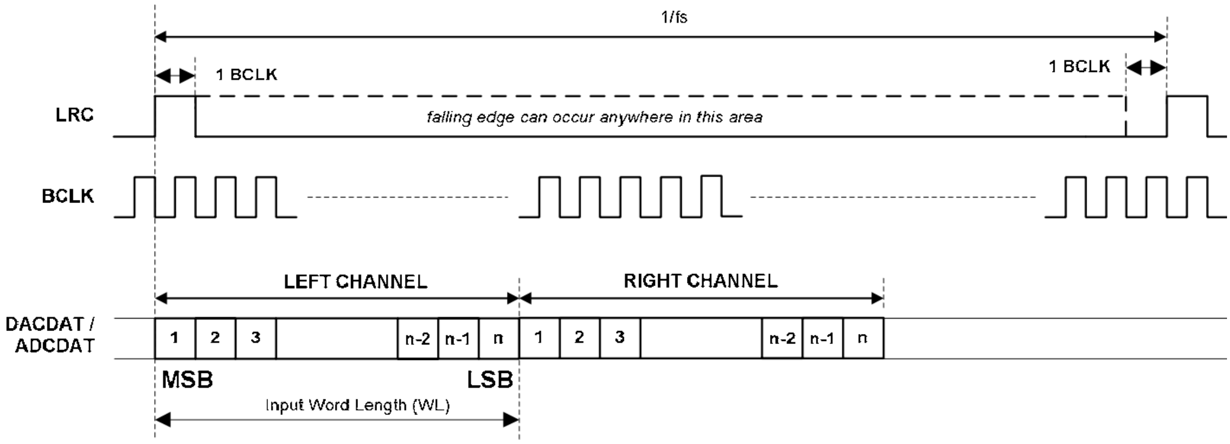


Figure 17 DSP/PCM Mode Audio Interface (mode B, LRP=0, Slave)

14.25. AUDIO INTERFACE CONTROL

The register bits controlling audio format, word length and master / slave mode are summarised in Table 31. MS selects audio interface operation in master or slave mode. In Master mode BCLK and LRC are outputs. The frequency of LRC is set by the sample rate control bits SR[4:0] and USB. In Slave mode BCLK and LRC are inputs.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 (07h) Digital Audio Interface Format	7	BCLKINV	0	BCLK invert bit (for master and slave modes) 0 = BCLK not inverted 1 = BCLK inverted
	6	MS	0	Master / Slave Mode Control 1 = Enable Master Mode 0 = Enable Slave Mode
	5	LRSWAP	0	Left/Right channel swap 1 = swap left and right DAC data in audio interface 0 = output left and right data as normal
	4	LRP	0	right, left and I^2S modes – LRCLK polarity 1 = invert LRCLK polarity 0 = normal LRCLK polarity
				DSP Mode – mode A/B select 1 = MSB is available on 1 BCLK rising edge after LRC rising edge (mode B) 0 = MSB is available on 2 BCLK rising edge after LRC rising edge (mode A)
	3:2	WL[1:0]	10	Audio Data Word Length 11 = 32 bits (see Note) 10 = 24 bits 01 = 20 bits 00 = 16 bits
	1:0	FORMAT[1:0]	10	Audio Data Format Select 11 = DSP Mode 10 = I^2S Format 01 = Left justified 00 = reserved (do not use this setting)

Table 31 Audio Data Format Control

14.26. AUDIO INTERFACE OUTPUT TRISTATE

Register bit TRI, register 24(18h) bit[3] can be used to tristate the ADCDAT pin and switch ADCLRC, DACLRC and BCLK to inputs. In Slave mode (MASTER=0) LRC and BCLK are by default configured as inputs and only ADCDAT will be tri-stated, (see Table 32).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24(18h) Additional Control (2)	3	TRI	0	Tristates ADCDAT and switches ADCLRC, DACLRC and BCLK to inputs. 0 = ADCDAT is an output, LRC and BCLK are inputs (slave mode) or outputs (master mode) 1 = ADCDAT is tristated, LRC and BCLK are inputs

Table 32 Tri-stating the Audio Interface

14.27. MASTER MODE LRC ENABLE

In Master mode the lrclk (LRC) is enabled by default only when the DAC is enabled. If ADC only operation in Master mode is required register bit LRCM must be set in oder to generate an lrclk. For DAC only operation LRCM may be set to '0'.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24(18h) Additional Control (2)	2	LRCM	0	Selects disable mode for LRC 0 = LRC disabled when DAC (Left and Right) disabled. 1 = LRC disabled only when ADC (Left and Right) and DAC (Left and Right) are disabled.

Table 33 LRC Enable

14.28. BIT CLOCK MODE

The default master mode bit clock generator produces a bit clock frequency based on the sample rate and input MCLK frequency as shown in Table 36.When enabled by setting the appropriate BCM[1:0] bits, the bit clock mode (BCM) function overrides the default master mode bit clock generator to produce the bit clock frequency shown in the table below:

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 (08h) Clocking and Sample Rate Control	8:7	BCM[1:0]	00	BCLK Frequency 00 = BCM function disabled 01 = MCLK/4 10 = MCLK/8 11 = MCLK/16

Table 34 Master Mode BCLK Frequency Control

The BCM mode bit clock generator produces 16 or 24 bit clock cycles per sample. The number of bit clock cycles per sample in this mode is determined by the word length bits (WL[1:0]) in the Digital Audio Interface Format register (R7). When these bits are set to 00, there will be 16 bit clock cycles per sample. When these bits are set to 01, 10 or 11, there will be 24 bit clock cycles per sample. Please refer to Figure 18.

In order to use BCM either the ADC must be enabled or, if the ADC is disabled, the LRCM bit must be set and the DAC enabled.

When the BCM function is enabled, the following restrictions apply:

1. The bit clock invert (BCLKINV) function is not available.
2. DSP late digital audio interface mode is not available and must not be enabled.

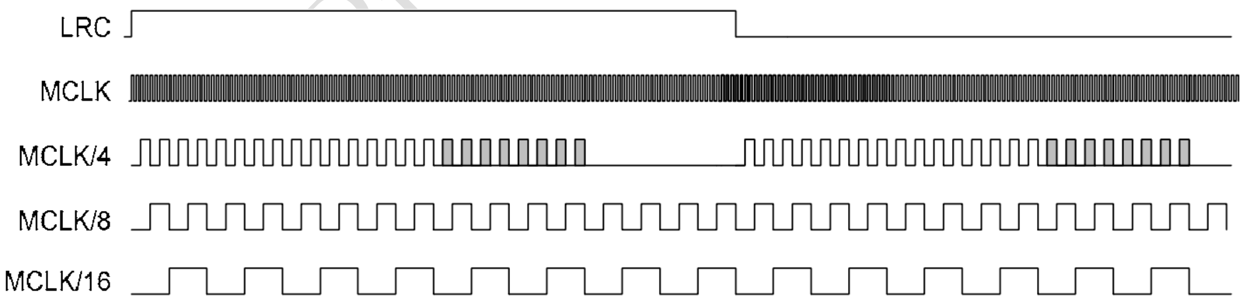


Figure 18 Bit Clock Mode

Note:
The shaded bit clock cycles are present only when 24-bit mode is selected. Please refer to the “Bit Clock Mode” description for details.

14.29. CLOCKING AND SAMPLE RATES

The CJC8988 supports a wide range of master clock frequencies on the MCLK pin, and can generate many commonly used audio sample rates directly from the master clock. The ADC and DAC must always run at the same sample rate.

There are two clocking modes:

- 'Normal' mode supports master clocks of 128fs, 192fs, 256fs, 384fs, and their multiples (Note: fs refers to the ADC or DAC sample rate, whichever is faster)
-
- USB mode supports 12MHz or 24MHz master clocks. This mode is intended for use in systems with a USB interface, and eliminates the need for an external PLL to generate another clock frequency for the audio codec.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 (08h) Clocking and Sample Rate Control	6	CLKDIV2	0	Master Clock Divide by 2 1 = MCLK is divided by 2 0 = MCLK is not divided
	5:1	SR [4:0]	00000	Sample Rate Control
	0	USB	0	Clocking Mode Select 1 = USB Mode 0 = 'Normal' Mode

Table 35 Clocking and Sample Rate Control

The clocking of the CJC8988 is controlled using the CLKDIV2, USB, and SR control bits. Setting the CLKDIV2 bit divides MCLK by two internally. The USB bit selects between 'Normal' and USB mode. Each value of SR[4:0] selects one combination of MCLK division ratios and hence one combination of sample rates (see next page). Since all sample rates are generated by dividing MCLK, their accuracy depends on the accuracy of MCLK. If MCLK changes, the sample rates change proportionately.

Note that some sample rates (e.g. 44.1kHz in USB mode) are approximated, i.e. they differ from their target value by a very small amount. This is not audible, as the maximum deviation is only 0.27% (8.0214kHz instead of 8kHz in USB mode). By comparison, a half-tone step corresponds to a 5.9% change in pitch.

The SR[4:0] bits must be set to configure the appropriate ADC and DAC sample rates in both master and slave mode.

MCLK CLKDIV2=0	MCLK CLKDIV2=1	ADC SAMPLE RATE (ADCLRC)	DAC SAMPLE RATE (DACLRC)	USB	SR [4:0]	FILTER TYPE	BCLK (MS=1)
'Normal' Clock Mode ('*' indicates backward compatibility with CJC8731)							
12.288 MHz	24.576 MHz	8 kHz (MCLK/1536)	8 kHz (MCLK/1536)	0	00110*	1	MCLK/4
		12 kHz (MCLK/1024)	12 kHz (MCLK/1024)	0	01000	1	MCLK/4
		16 kHz (MCLK/768)	16 kHz (MCLK/768)	0	01010	1	MCLK/4
		24 kHz (MCLK/512)	24 kHz (MCLK/512)	0	11100	1	MCLK/4
		32 kHz (MCLK/384)	32 kHz (MCLK/384)	0	01100*	1	MCLK/4
		48 kHz (MCLK/256)	48 kHz (MCLK/256)	0	00000*	1	MCLK/4
		96 kHz (MCLK/128)	96 kHz (MCLK/128)	0	01110*	3	MCLK/2
11.2896MHz	22.5792MHz	8.0182 kHz (MCLK/1408)	8.0182 kHz (MCLK/1408)	0	10110*	1	MCLK/4
		11.025 kHz (MCLK/1024)	11.025 kHz (MCLK/1024)	0	11000	1	MCLK/4
		22.05 kHz (MCLK/512)	22.05 kHz (MCLK/512)	0	11010	1	MCLK/4
		44.1 kHz (MCLK/256)	44.1 kHz (MCLK/256)	0	10000*	1	MCLK/4
		88.2 kHz (MCLK/128)	88.2 kHz (MCLK/128)	0	11110*	3	MCLK/2
18.432MHz	36.864MHz	8 kHz (MCLK/2304)	8 kHz (MCLK/2304)	0	00111*	1	MCLK/6
		12 kHz (MCLK/1536)	12 kHz (MCLK/1536)	0	01001	1	MCLK/6
		16kHz (MCLK/1152)	16 kHz (MCLK/1152)	0	01011	1	MCLK/6
		24kHz (MCLK/768)	24 kHz (MCLK/768)	0	11101	1	MCLK/6
		32 kHz (MCLK/576)	32 kHz (MCLK/576)	0	01101*	1	MCLK/6
		48 kHz (MCLK/384)	48 kHz (MCLK/384)	0	00001*	1	MCLK/6
		96 kHz (MCLK/192)	96 kHz (MCLK/192)	0	01111*	3	MCLK/3
16.9344MHz	33.8688MHz	8.0182 kHz (MCLK/2112)	8.0182 kHz (MCLK/2112)	0	10111*	1	MCLK/6
		11.025 kHz (MCLK/1536)	11.025 kHz (MCLK/1536)	0	11001	1	MCLK/6
		22.05 kHz (MCLK/768)	22.05 kHz (MCLK/768)	0	11011	1	MCLK/6
		44.1 kHz (MCLK/384)	44.1 kHz (MCLK/384)	0	10001*	1	MCLK/6
		88.2 kHz (MCLK/192)	88.2 kHz (MCLK/192)	0	11111*	3	MCLK/3

Table 36a Master Clock and Sample Rates

MCLK CLKDIV2=0	MCLK CLKDIV2=1	ADC SAMPLE RATE (ADCLRC)	DAC SAMPLE RATE (DACLRC)	USB	SR [4:0]	FILTER TYPE	BCLK (MS=1)
USB Mode ('*' indicates backward compatibility with CJC8731)							
12.000MHz	24.000MHz	8 kHz (MCLK/1500)	8 kHz (MCLK/1500)	1	00110*	0	MCLK
		8.0214 kHz (MCLK/1496)	8.0214kHz (MCLK/1496)	1	10111*	1	MCLK
		11.0259 kHz (MCLK/1088)	11.0259kHz (MCLK/1088)	1	11001	1	MCLK
		12 kHz (MCLK/1000)	12 kHz (MCLK/1000)	1	01000	0	MCLK
		16kHz (MCLK/750)	16kHz (MCLK/750)	1	01010	0	MCLK
		22.0588kHz (MCLK/544)	22.0588kHz (MCLK/544)	1	11011	1	MCLK
		24kHz (MCLK/500)	24kHz (MCLK/500)	1	11100	0	MCLK
		32 kHz (MCLK/375)	32 kHz (MCLK/375)	1	01100*	0	MCLK
		44.118 kHz (MCLK/272)	44.118 kHz (MCLK/272)	1	10001*	1	MCLK
		48 kHz (MCLK/250)	48 kHz (MCLK/250)	1	00000*	0	MCLK
		88.235kHz (MCLK/136)	88.235kHz (MCLK/136)	1	11111*	3	MCLK
		96 kHz (MCLK/125)	96 kHz (MCLK/125)	1	01110*	2	MCLK

Table 36b Master Clock and Sample Rates

14.30. CONTROL INTERFACE

SELECTION OF CONTROL MODE

The CJC8988 is controlled by writing to registers through a serial control interface. A control word consists of 16 bits. The first 7 bits (B15 to B9) are address bits that select which control register is accessed. The remaining 9 bits (B8 to B0) are data bits, corresponding to the 9 bits in each control register. The control interface can operate as either a 3-wire or 2-wire MPU interface. The MODE pin selects the interface format.

MODE	INTERFACE FORMAT
Low	2
High	3

Table 37 Control Interface Mode Selection

3-WIRE SERIAL CONTROL MODE

In 3-wire mode, every rising edge of SCLK clocks in one data bit from the SDIN pin. A rising edge on CSB latches in a complete control word consisting of the last 16 bits.

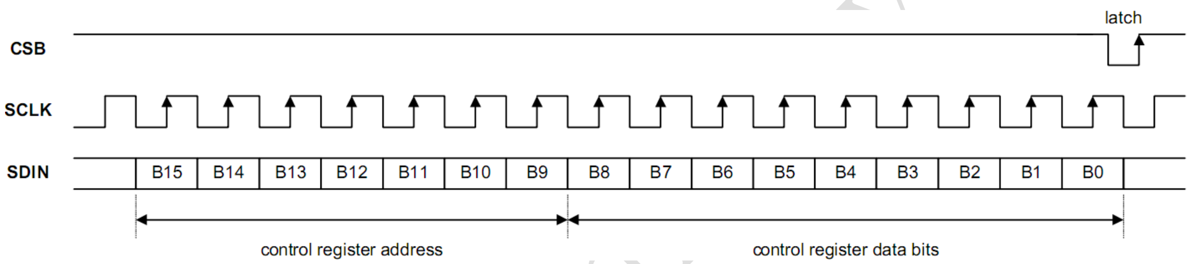


Figure 19 3-Wire Serial Control Interface

2-WIRE SERIAL CONTROL MODE

The CJC8988 supports software control via a 2-wire serial bus. Many devices can be controlled by the same bus, and each device has a unique 7-bit address (this is not the same as the 7-bit address of each register in the CJC8988).

The CJC8988 operates as a slave device only. The controller indicates the start of data transfer with a high to low transition on SDIN while SCLK remains high. This indicates that a device address and data will follow. All devices on the 2-wire bus respond to the start condition and shift in the next eight bits on SDIN (7-bit address + Read/Write bit, MSB first). If the device address received matches the address of the CJC8988 and the R/W bit is ‘0’, indicating a write, then the CJC8988 responds by pulling SDIN low on the next clock pulse (ACK). If the address is not recognised or the R/W bit is ‘1’, the CJC8988 returns to the idle condition and wait for a new start condition and valid address.

Once the CJC8988 has acknowledged a correct address, the controller sends the first byte of control data (B15 to B8, i.e. the CJC8988 register address plus the first bit of register data). The CJC8988 then acknowledges the first data byte by pulling SDIN low for one clock pulse. The controller then sends the second byte of control data (B7 to B0, i.e. the remaining 8 bits of register data), and the CJC8988 acknowledges again by pulling SDIN low.

The transfer of data is complete when there is a low to high transition on SDIN while SCLK is high. After receiving a complete address and data sequence the CJC8988 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. SDIN changes while SCLK is high), the device jumps to the idle condition.

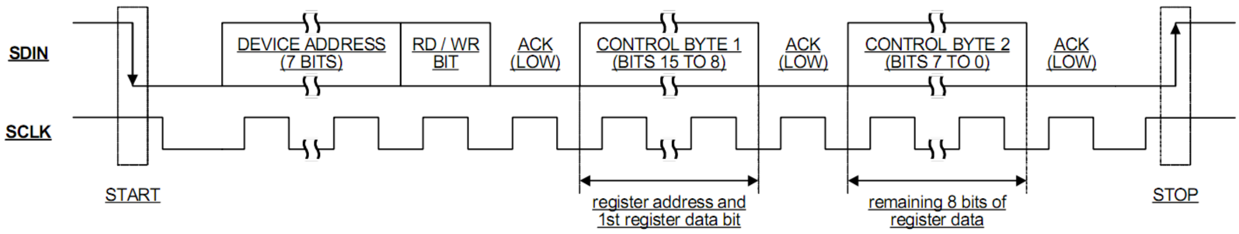


Figure 20 2-Wire Serial Control Interface

Note:
MCLK must be provided before initializing registers.

The CJC8988 has two possible device addresses, which can be selected using the CSB pin.

CSB STATE	DEVICE ADDRESS(8BIT)
Low	**Write 00110100 (0x34h)**
	Read 00110101(0x35h)
High	**Write 00110110 (0x36h)**
	Read 00110111(0x37h)

Table 38 2-Wire MPU Interface Address Selection

14.31. POWER SUPPLIES

The CJC8988 can use up to four separate power supplies:

- AVDD / AGND: Analogue supply, powers all analogue functions except the headphone drivers. AVDD can range from 1.8V to 3.3V and has the most significant impact on overall power consumption (except for power consumed in the headphone). A large AVDD slightly improves audio quality.

- HPVDD / HPGND: Headphone supply, powers the headphone drivers. HPVDD is normally tied to AVDD, but it requires separate layout and decoupling capacitors to curb harmonic distortion. If HPVDD is lower than AVDD, the output signal may be clipped.

- DCVDD: Digital core supply, powers all digital functions except the audio and control interfaces. DCVDD can range from 1.5V to 3.3V, and has no effect on audio quality. The return path for DCVDD is DGND, which is shared with DBVDD.

- DBVDD: Digital buffer supply, powers the audio and control interface buffers. This makes it possible to run the digital core at very low voltages, saving power, while interfacing to other digital devices using a higher voltage. DBVDD draws much less power than DCVDD, and has no effect on audio quality. DBVDD can range from 1.8V to 3.3V. The return path for DBVDD is DGND, which is shared with DCVDD.

It is possible to use the same supply voltage on all four. However, digital and analogue supplies should be routed and decoupled separately to keep digital switching noise out of the analogue signal paths.

14.32. POWER MANAGEMENT

The CJC8988 has two control registers that allow users to select which functions are active. For minimum power consumption, unused functions should be disabled. To avoid any pop or click noise, it is important to enable or disable functions in the correct order (see Applications Information). VMIDSEL is the enable for the Vmid reference, which defaults to disabled and can be enabled as a 50kΩ potential divider or, for low power maintenance of Vref when all other blocks are disabled, as a 500kΩ potential divider.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R25 (19h) Power Management (1)	8:7	VMIDSEL	00	Vmid divider enable and select 00 – Vmid disabled (for OFF mode) 01 – 50kΩ divider enabled (for playback/record) 10 – 500kΩ divider enabled (for low-power standby) 11 – 5kΩ divider enabled (for fast start-up)
	6	VREF	0	VREF (necessary for all other functions) 0 = Power down 1 = Power up
	5	AINL	0	Analogue in PGA Left 0 = Power down 1 = Power up
	4	AINR	0	Analogue in PGA Right 0 = Power down 1 = Power up
	3	ADCL	0	ADC Left 0 = Power down 1 = Power up
	2	ADCR	0	ADC Right 0 = Power down 1 = Power up
R26 (1Ah) Power Management (2)	8	DACL	0	DAC Left 0 = Power down 1 = Power up
	7	DACR	0	DAC Right 0 = Power down 1 = Power up
	6	LOUT1	0	LOUT1 Output Buffer* 0 = Power down 1 = Power up
	5	ROUT1	0	ROUT1 Output Buffer* 0 = Power down 1 = Power up
	4	LOUT2	0	LOUT2 Output Buffer* 0 = Power down 1 = Power up
	3	ROUT2	0	ROUT2 Output Buffer* 0 = Power down 1 = Power up

* The left mixer is enabled when LOUT1=1 or LOUT2=1. The right mixer is enabled when ROUT1=1 or ROUT2=1.

Table 39 Power Management

14.33. STOPPING THE MASTER CLOCK

In order to minimise power consumed in the digital core of the CJC8988, the master clock may be stopped in Standby and OFF modes. If this cannot be done externally at the clock source, the DIGENB bit (R25, bit 0) can be set to stop the MCLK signal from propagating into the device core. In Standby mode, setting DIGENB will typically provide an additional power saving on DCVDD of 20uA.

However, since setting DIGENB has no effect on the power consumption of other system components external to the CJC8988, it is preferable to disable the master clock at its source wherever possible.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R25 (19h) Additional Control (1)	0	DIGENB	0	Master clock disable 0: master clock enabled 1: master clock disabled

Table 40 ADC and DAC Oversampling Rate Selection

Note:

Before DIGENB can be set, the control bits ADCL, ADCR, DACL and DACR must be set to zero and a waiting time of 1ms must be observed. Any failure to follow this procedure may prevent DACs and ADCs from re-starting correctly.

14.34. SAVING POWER BY REDUCING BIAS CURRENTS

The design of the DAC allows user trade-off between power consumption and performance, using the DACMIXBIAS bit. The default setting (DACMIXBIAS=0) delivers the best audio performance. Setting DACMIXBIAS=1 reduces AVDD current consumption, at the cost of marginally reduced performance (see “Electrical Characteristics” for details).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R67 (43h)	3	DACMIX BIAS	0	DAC biasing 0 = high bias current (results in higher performance and power consumption) 1 = low bias current (results in lower performance and power consumption)

Table 41 DAC Biasing

14.35. SAVING POWER BY REDUCING OVERSAMPLING RATE

The default mode of operation of the ADC and DAC digital filters is in 128x oversampling mode. Under the control of ADCOSR and DACOSR the oversampling rate may be halved. This will result in a slight decrease in noise performance but will also reduce the power consumption of the device. In USB mode ADCOSR must be set to 0, i.e. 128x oversampling.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24 (18h) Additional Control (2)	1	ADCOSR	0	ADC oversample rate select 1 = 64x (lowest power) 0 = 128x (best SNR)
	0	DACOSR	0	DAC oversample rate select 1 = 64x (lowest power) 0 = 128x (best SNR)

Table 42 ADC and DAC Oversampling Rate Selection

ADCOSR set to '1', 64x oversample mode, is not supported in USB mode (USB=1).

14.36. SAVING POWER AT HIGHER SUPPLY VOLTAGES

The analogue supplies to the CJC8988 can run from 1.8V to 3.3V. By default, all analogue circuitry on the device is optimized to run at 3.3V. This set-up is also good for all other supply voltages down to 1.8V. At lower voltages, performance can be improved by increasing the bias current. If low power operation is preferred the bias current can be left at the default setting. This is controlled as shown below.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R23 (17h) Additional Control (1)	7:6	VSEL [1:0]	11	Analogue Bias optimization 00: Highest bias current, optimized for AVDD=1.8V 01: Bias current optimized for AVDD=2.4V 1X: Lowest bias current, optimized for AVDD=3.3V

15. REGISTER MAP

REGISTER	ADDRESS (Bit 15 – 9)	remarks	Bit[8]	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	default	page ref
R0 (00h)	0000000	Left Input volume	LIVU	LINMUTE	LIZC	LINVOL						10010111	19
R1 (01h)	0000001	Right Input volume	RIVU	RINMUTE	RIZC	RINVOL						10010111	19
R2 (02h)	0000010	LOUT1 volume	LO1VU	LO1ZC	LOUT1VOL[6:0]							01111001	31
R3 (03h)	0000011	ROUT1 volume	RO1VU	RO1ZC	ROUT1VOL[6:0]							01111001	31
R4 (04h)	0000100	Reserved	0	0	0	0	0	0	0	0	0	00000000	-
R5 (05h)	0000101	ADC & DAC Control	ADCDIV2	DACDIV2	ADCPOL[1:0]		HPOR	DACMU	DEEMPH[1:0]		ADCHPD	00001000	19,25,28
R6 (06h)	0000110	Reserved	0	0	0	0	0	0	0	0	0	00000000	-
R7 (07h)	0000111	Audio Interface	0	BCLKINV	MS	LRSWAP	LRP	WL[1:0]		FORMAT[1:0]		00001010	37
R8 (08h)	0001000	Sample rate	BCM[1:0]		CLKDIV2	SR[4:0]					USB	00000000	39
R9 (09h)	0001001	Reserved	0	0	0	0	0	0	0	0	0	00000000	-
R10 (0Ah)	0001010	Left DAC volume	LDVU	LDACVOL[7:0]								11111111	26
R11 (0Bh)	0001011	Right DAC volume	RDVU	RDACVOL[7:0]								11111111	26
R12 (0Ch)	0001100	Bass control	0	BB	BC	0	0	BASS[3:0]				00001111	27
R13 (0Dh)	0001101	Treble control	0	0	TC	0	0	TRBL[3:0]				00001111	27
R15 (0Fh)	0001111	Reset	writing to this register resets all registers to their default state									not reset	-
R16 (10h)	0010000	3D control	0	MODE3D	3DUC	3DLC	3DDEPTH[3:0]				3DEN	00000000	25
R17 (11h)	0010001	Reserved	0	0	1	1	1	1	0	1	1	01111011	23
R18 (12h)	0010010	Reserved	0	0	0	0	0	0	0	0	0	00000000	23
R19 (13h)	0010011	Reserved	0	0	0	1	1	0	0	1	0	00110010	23
R20 (14h)	0010100	Reserved	0	0	0	0	0	0	0	0	0	00000000	24
R21 (15h)	0010101	Left ADC volume	LAVU	LADCVOL[7:0]								11000011	21
R22 (16h)	0010110	Right ADC volume	RAVU	RADCVOL[7:0]								11000011	21

R23 (17h)	0010111	Additional control(1)	TSDEN	VSEL[1:0]		DMONOMIX[1:0]		DATSEL[1:0]		DACINV	TOEN	11000000	18,19,28,33
R24 (18h)	0011000	Additional control(2)	LCOMEN	HPCOMEN	0	0	0	TRI	LRCM	ADCOSR	DACOSR	00000000	
R25 (19h)	0011001	Pwr Mgmt (1)	VMIDSEL[1:0]		VREF	AINL	AINR	ADCL	ADCR	0	DIGENB	00000000	43
R26 (1Ah)	0011010	Pwr Mgmt (2)	DACL	DACR	LOUT1	ROUT1	LOUT2	ROUT2	0	0	0	00000000	43
R27 (1Bh)	0011011	Additional Control (3)	00		VROI	HPFLREN	0	0	0	0	0	00000000	35
R31 (1Fh)	0011111	ADC input mode	DS	MONOMIX[1:0]		RDCM	LDCM	0	0	0	0	00000000	17
R32 (20h)	0100000	ADCL signal path	0	LINSEL[1:0]		LMICBOOST[1:0]		0	0	0	0	00000000	17
R33 (21h)	0100001	ADCR signal path	0	RINSEL[1:0]		RMICBOOST[1:0]		0	0	0	0	00000000	17
R34 (22h)	0100010	Left out Mix (1)	LD2LO	LI2LO	LI2LOVOL[2:0]			0	LMIXSEL[2:0]			01010000	29
R35 (23h)	0100011	Left out Mix (2)	RD2LO	RI2LO	RI2LOVOL[2:0]			0	0	0	0	01010000	29
R36 (24h)	0100100	Right out Mix (1)	LD2RO	LI2RO	LI2ROVOL[2:0]			0	RMIXSEL[2:0]			01010000	30
R37 (25h)	0100101	Right out Mix (2)	RD2RO	RI2RO	RI2ROVOL[2:0]			0	0	0	0	01010000	30
R38 (26h)	0100110	Reserved	0	0	1	0	1	0	0	0	0	01010000	30
R39 (27h)	0100111	Reserved	0	0	1	0	1	0	0	0	0	01010000	30
R40 (28h)	0101000	LOUT2 volume	LO2VU	LO2ZC	LOUT2VOL[6:0]							01111001	32
R41 (29h)	0101001	ROUT2 volume	RO2VU	RO2ZC	ROUT2VOL[6:0]							01111001	32
R42 (2Ah)	0101010	Reserved	0	0	1	1	1	0	1	0	1	01111001	35
R67 (43h)	1000011	Low Power Playback	0	0	0	0	0	0	DACMIX BIAS	0	0	00000000	50

16. DIGITAL FILTER CHARACTERISTICS

The ADC and DAC employ different digital filters. There are 4 types of digital filter, called Type 0, 1, 2 and 3. The performance of Types 0 and 1 is listed in the table below, the responses of all filters is shown in the proceeding pages.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Filter Type 0 (USB Mode, 250fs operation)					
Passband	**+/- 0.05dB**	**0**		**0.416fs**	
	-6dB		**0.5fs**		
Passband Ripple				**+/- 0.05**	**dB**
Stopband		**0.584fs**			
Stopband Attenuation	**f > 0.584fs**	**-60**			**dB**
ADC Filter Type 1 (USB mode, 272fs or Normal mode operation)					
Passband	**+/- 0.05dB**	**0**		**0.4535fs**	
	-6dB		**0.5fs**		
Passband Ripple				**+/- 0.05**	**dB**
Stopband		**0.5465fs**			
Stopband Attenuation	**f > 0.5465fs**	**-60**			**dB**
High Pass Filter Corner Frequency	**-3dB**		**3.7**		**Hz**
	-0.5dB		**10.4**		
	-0.1dB		**21.6**		
DAC Filter Type 0 (USB mode, 250fs operation)					
Passband	**+/- 0.03dB**	**0**		**0.416fs**	
	-6dB		**0.5fs**		
Passband Ripple				**+/-0.03**	**dB**
Stopband		**0.584fs**			
Stopband Attenuation	**f > 0.584fs**	**-50**			**dB**
DAC Filter Type 1 (USB mode, 272fs or Normal mode operation)					
Passband	**+/- 0.03dB**	**0**		**0.4535fs**	
	-6dB		**0.5fs**		
Passband Ripple				**+/- 0.03**	**dB**
Stopband		**0.5465fs**			
Stopband Attenuation	**f > 0.5465fs**	**-50**			**dB**

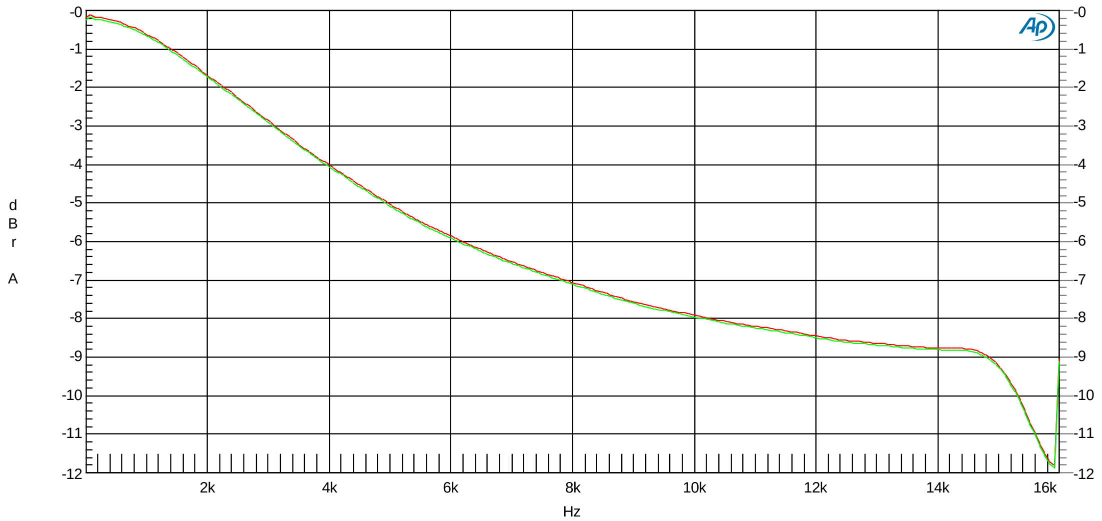
Table 43 Digital Filter Characteristics

DAC FILTERS		ADC FILTERS	
Mode	**Group Delay**	**Mode**	**Group Delay**
0 (250 USB)	**11/FS**	**0 (250 USB)**	**13/FS**
1 (256/272)	**16/FS**	**1 (256/272)**	**23/FS**
2 (250 USB, 96k mode)	**4/FS**	**2 (250 USB, 96k mode)**	**4/FS**
3 (256/272, 88.2/96k mode)	**3/FS**	**3 (256/272, 88.2/96k mode) 3/FS**	**5/FS**

Table 44 ADC/DAC Digital Filters Group Delay

16.1. DAC FILTER RESPONSES
DE-EMPHASIS FILTER RESPONSES

Audio Precision 12/09/11 11:30:04

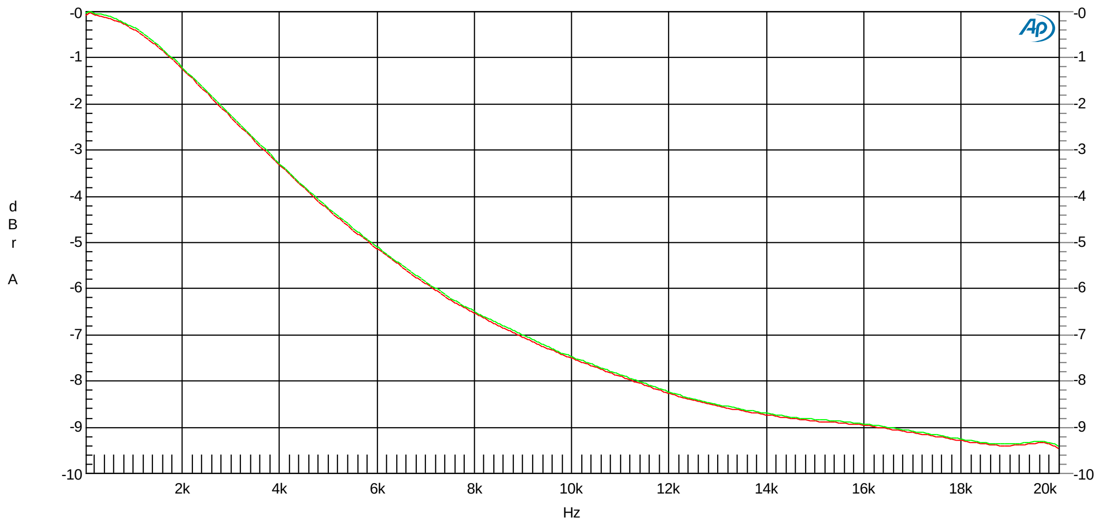


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	1	DSP Anlr.Ampl A	Left	
1	2	Green	Solid	1	DSP Anlr.Ampl B	Right	

dem32k.at27

Figure 21 De-emphasis Frequency Response (32kHz)

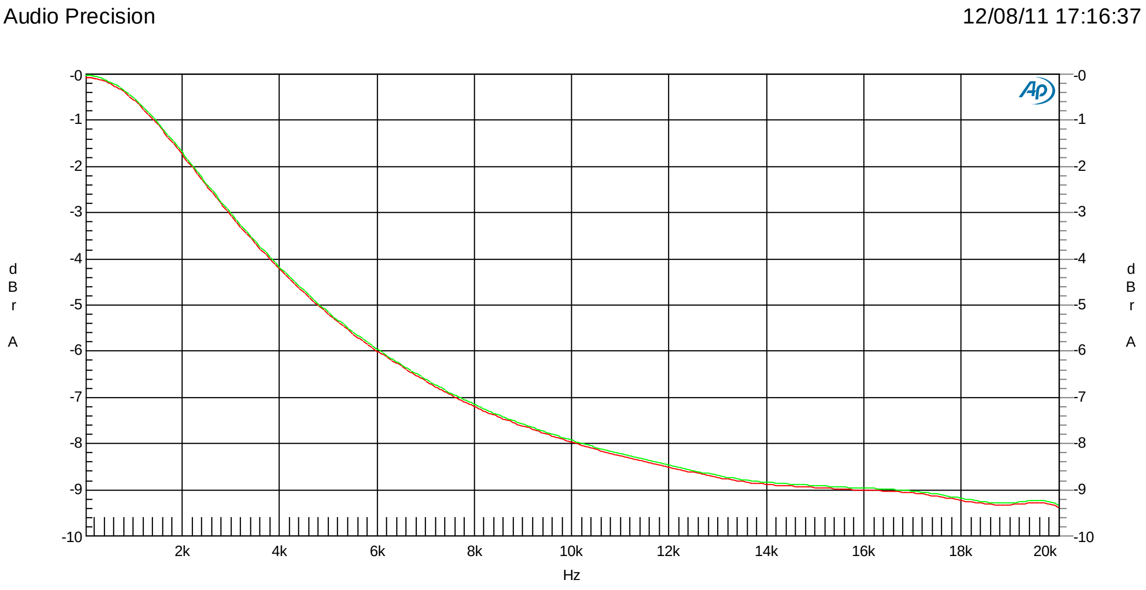
Audio Precision 12/08/11 17:37:04



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	1	DSP Anlr.Ampl A	Left	
1	2	Green	Solid	1	DSP Anlr.Ampl B	Right	

dem44.1k.at27

Figure 22 De-emphasis Frequency Response (44.1kHz)



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	1	DSP Anlr.Ampl A	Left	
1	2	Green	Solid	1	DSP Anlr.Ampl B	Right	

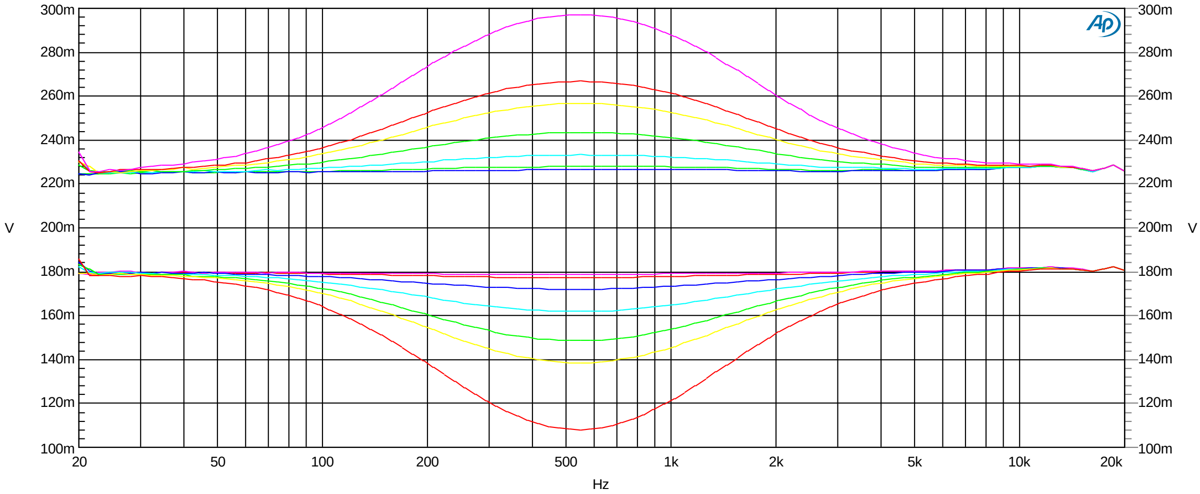
dem48k.at27

Figure 23 De-emphasis Frequency Response (48kHz)

16.2. 3D STEREO ENHANCEMENT

ADC 3D function

Audio Precision 12/05/11 18:02:59

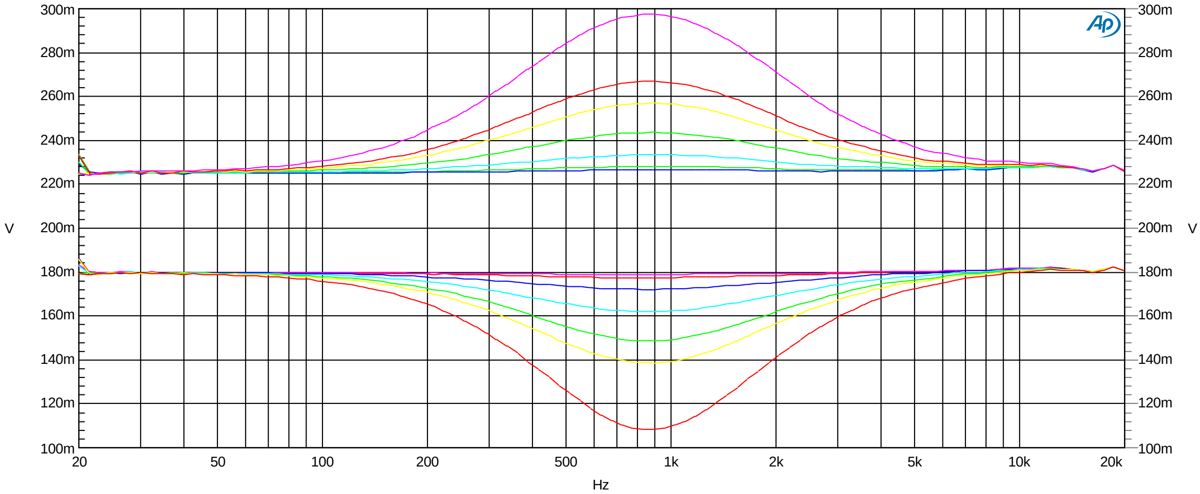


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	1	DSP Anlr.Ampl A	Left	
1	2	Green	Solid	1	DSP Anlr.Ampl B	Right	
2	1	Magenta	Solid	1	DSP Anlr.Ampl A	Left	

3d_1.5k_200.at27

Figure 24 ADC 3D 1.5KHz_200Hz

Audio Precision 12/05/11 18:07:51

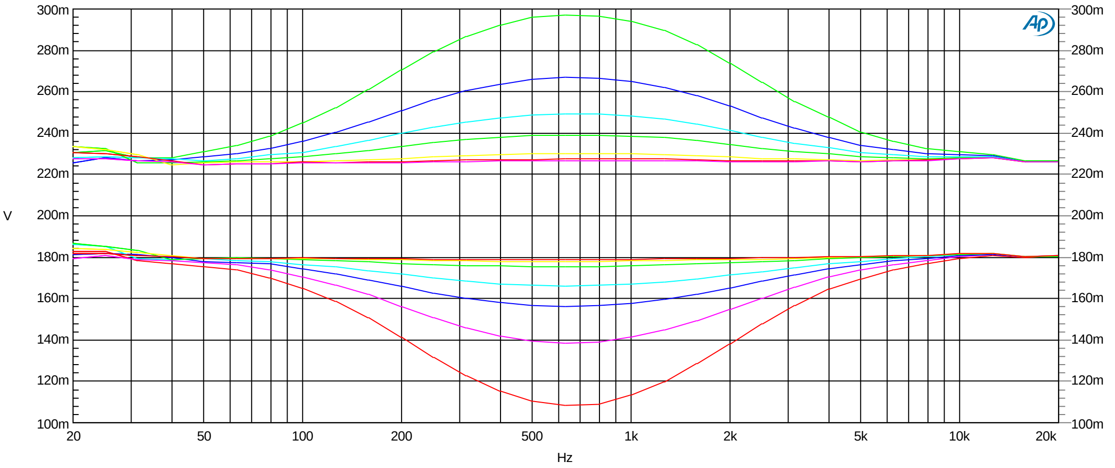


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	1	DSP Anlr.Ampl A	Left	
1	2	Green	Solid	1	DSP Anlr.Ampl B	Right	
2	1	Magenta	Solid	1	DSP Anlr.Ampl A	Left	

3d_1.5k_500.at27

Figure 25 ADC 3D 1.5KHz_500Hz

Audio Precision 12/05/11 17:59:38

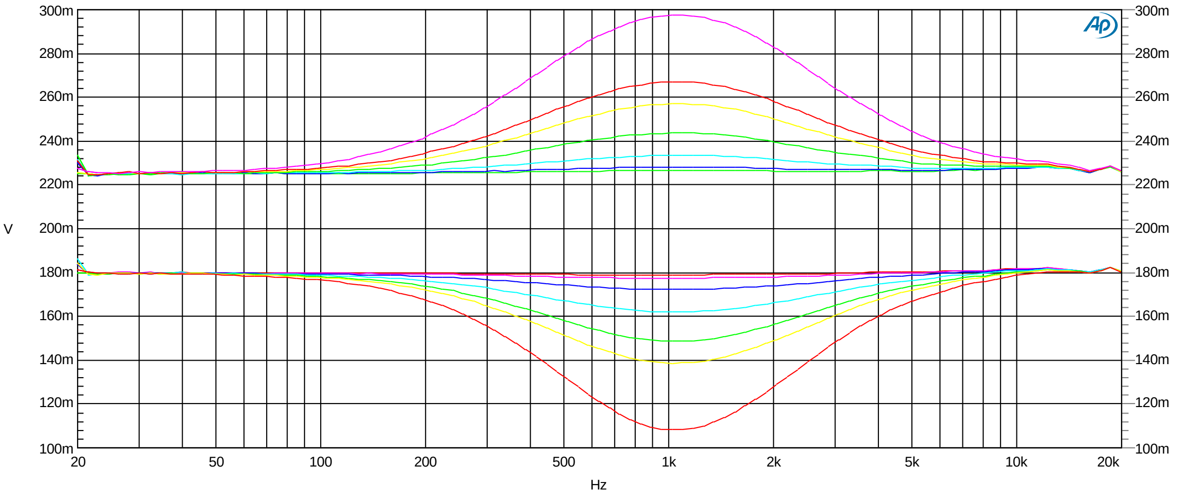


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	1	DSP Anlr.Ampl A	Left	
1	2	Green	Solid	1	DSP Anlr.Ampl B	Right	
2	1	Magenta	Solid	1	DSP Anlr.Ampl A	Left	

3d_2.2k_200.at27

Figure 26 ADC 3D 2.2KHz_200Hz

Audio Precision 12/05/11 18:05:34



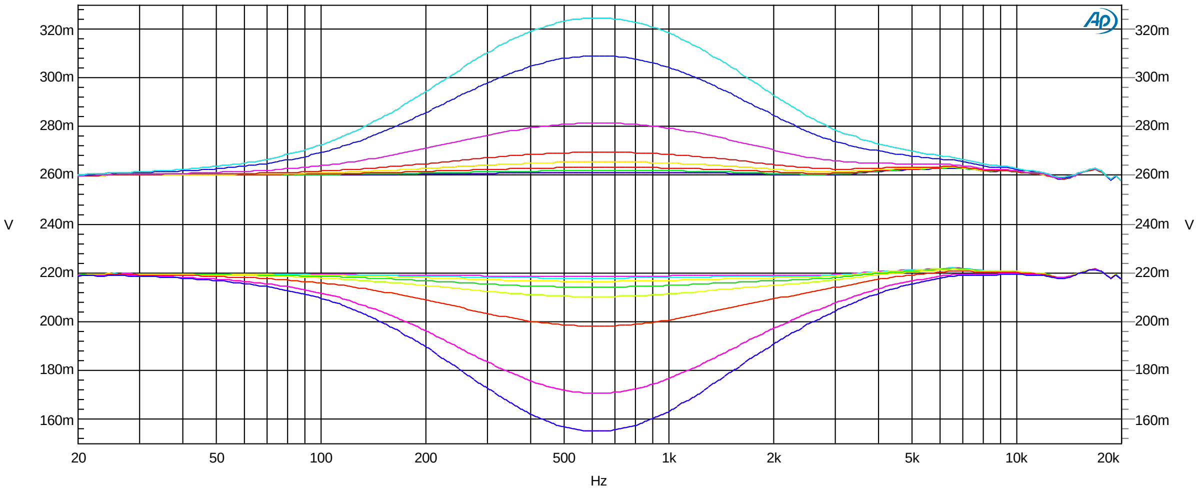
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	1	DSP Anlr.Ampl A	Left	
1	2	Green	Solid	1	DSP Anlr.Ampl B	Right	
2	1	Magenta	Solid	1	DSP Anlr.Ampl A	Left	

3d_2.2k_500.at27

Figure 27 ADC 3D 2.2KHz_500Hz

DAC 3D function

Audio Precision 12/05/11 16:54:09

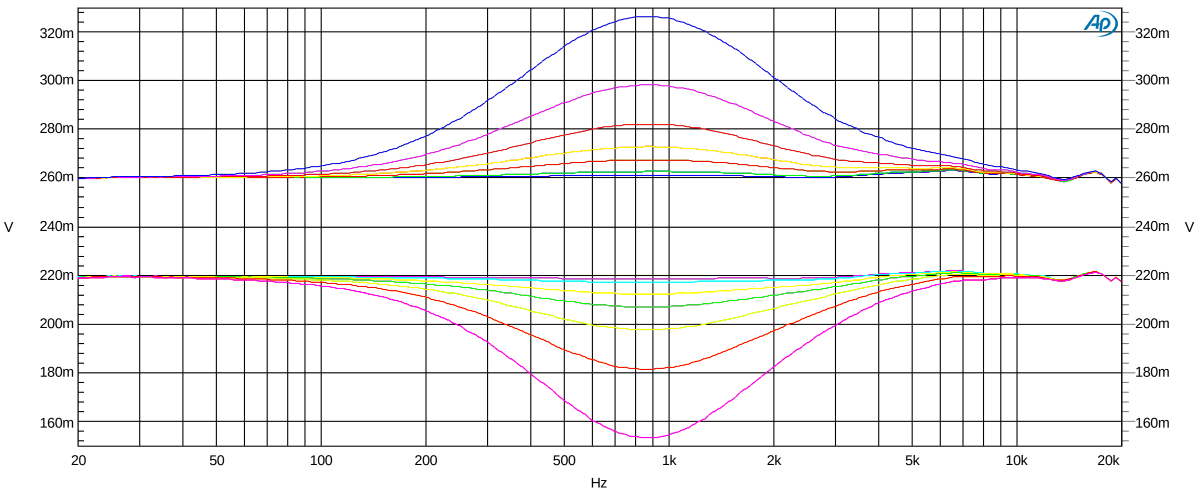


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	1	DSP Anlr.Ampl A	Left	
1	2	Green	Solid	1	DSP Anlr.Ampl B	Right	
1	3	Magenta	Solid	1	DSP Anlr.Ampl B	Left	

3d_1.5k_200.at27

Figure 28 DAC 3D 1.5KHz_200Hz

Audio Precision 12/05/11 17:02:22

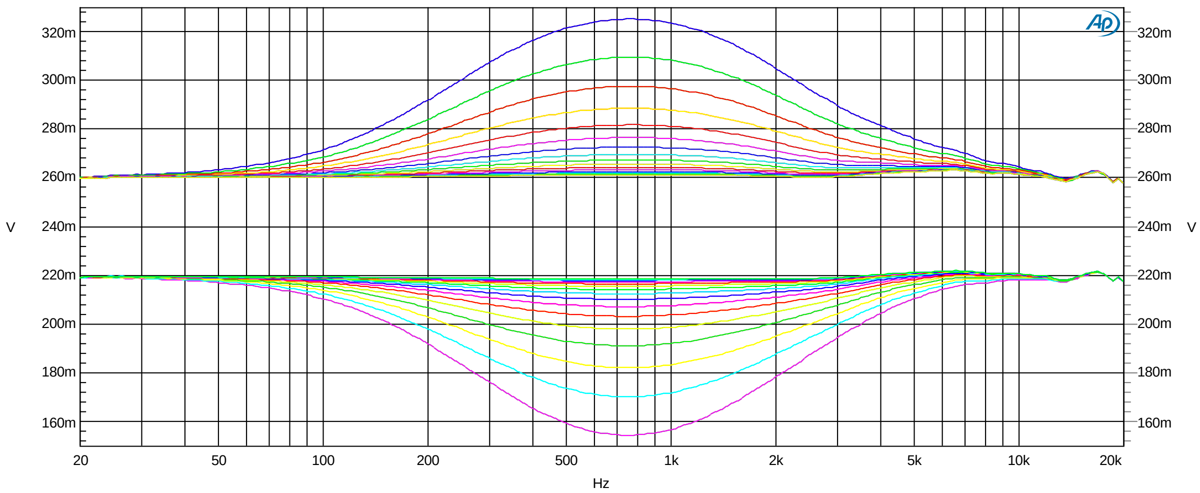


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	1	DSP Anlr.Ampl A	Left	
1	2	Green	Solid	1	DSP Anlr.Ampl B	Right	
1	3	Magenta	Solid	1	DSP Anlr.Ampl B	Left	

3d_1.5k_500.at27

Figure 29 DAC 3D 1.5KHz_500Hz

Audio Precision 12/05/11 16:47:32

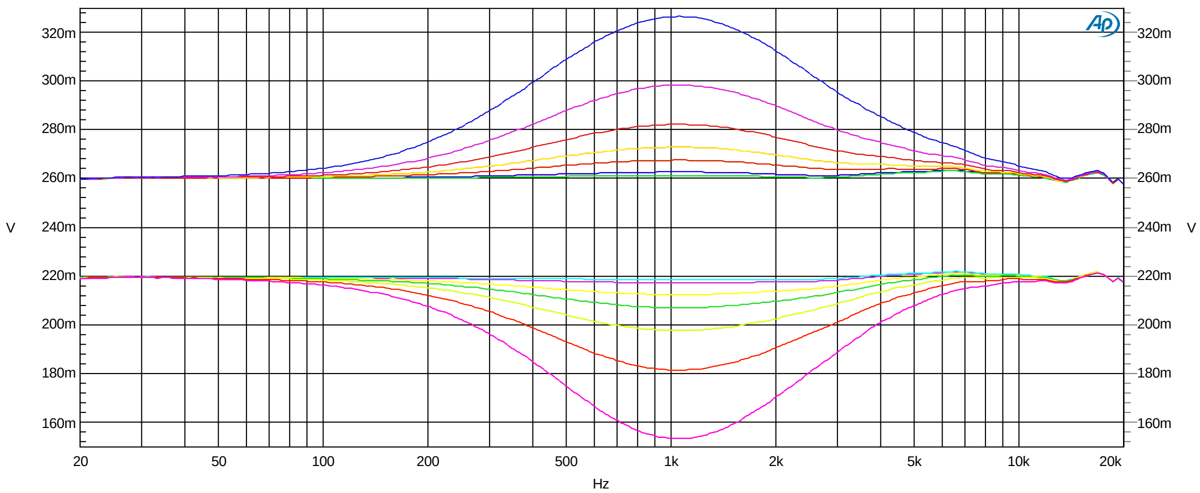


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	1	DSP Anlr.Ampl A	Left	
1	2	Green	Solid	1	DSP Anlr.Ampl B	Right	
1	3	Magenta	Solid	1	DSP Anlr.Ampl B	Left	

3d_2_2k_200.at27

Figure 30 DAC 3D 2.2KHz_200Hz

Audio Precision 12/05/11 16:58:28



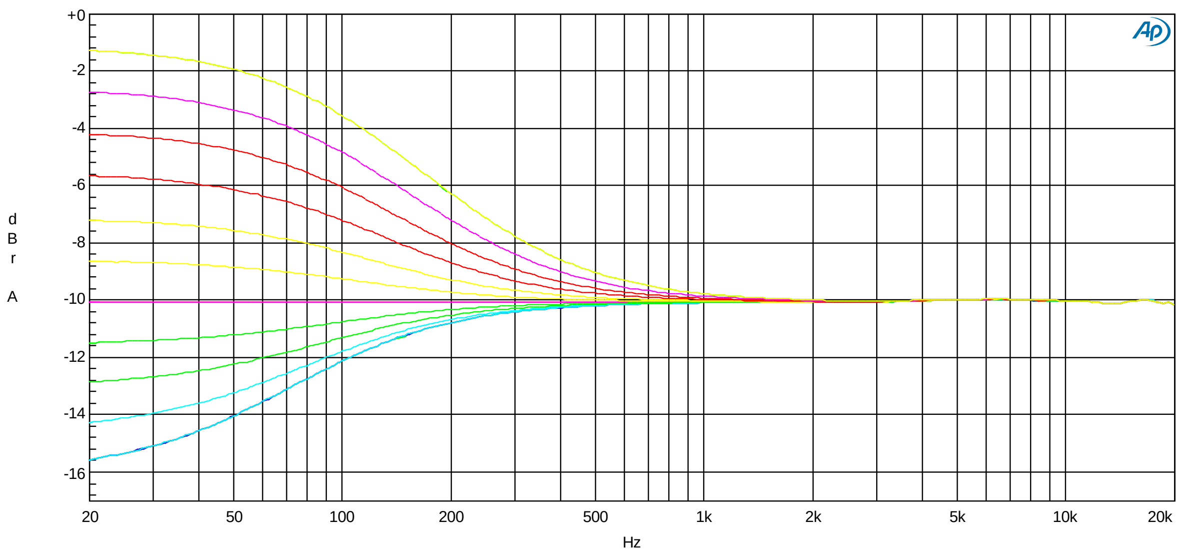
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	1	DSP Anlr.Ampl A	Left	
1	2	Green	Solid	1	DSP Anlr.Ampl B	Right	
1	3	Magenta	Solid	1	DSP Anlr.Ampl B	Left	

3d_2.2k_500.at27

Figure 31 DAC 3D 2.2KHz_500Hz

16.3. BASS BOOST FUNCTION

Audio Precision 12/05/11 15:34:04

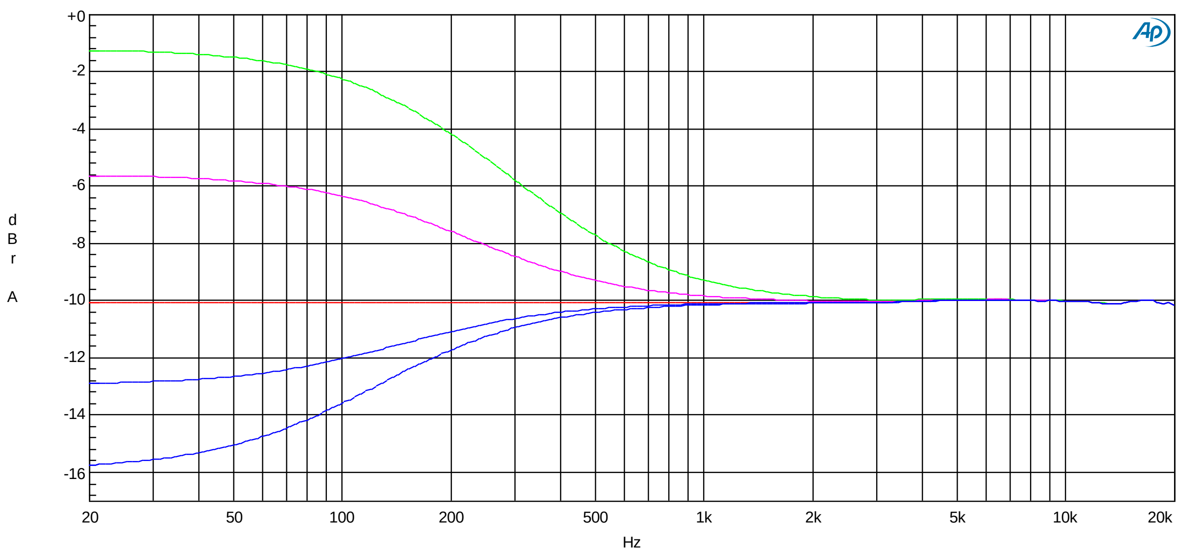


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	1	DSP Anlr.Ampl A	Left	
2	1	Green	Solid	1	DSP Anlr.Ampl A	Left	
3	1	Magenta	Solid	1	DSP Anlr.Ampl A	Left	

FREQUENCY RESPONSE，DIN=-10db BASS_BB=0 BC=0 m.at27

Figure 32 FREQUENCY RESPONSE，DIN=-10db BASS_BB=0 BC=0

Audio Precision 12/05/11 15:42:29

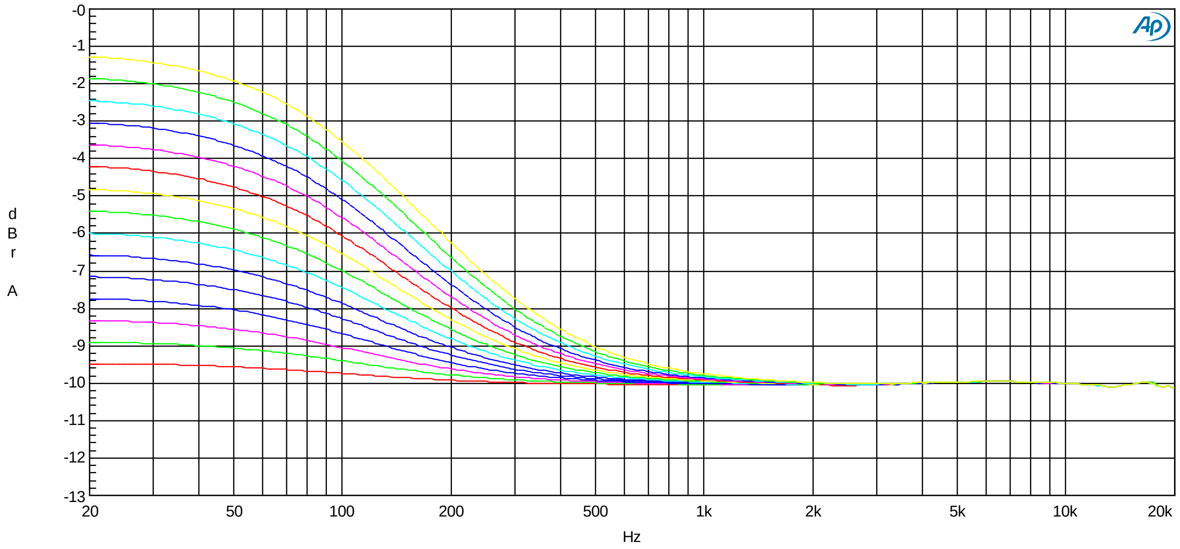


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	1	DSP Anlr.Ampl A	Left	
2	1	Green	Solid	1	DSP Anlr.Ampl A	Left	
3	1	Magenta	Solid	1	DSP Anlr.Ampl A	Left	

FREQUENCY RESPONSE，DIN=-10db BASS_BB=0 BC=1 m.at27

Figure 33 FREQUENCY RESPONSE，DIN=-10db BASS_BB=0 BC=1

Audio Precision 12/05/11 15:58:13

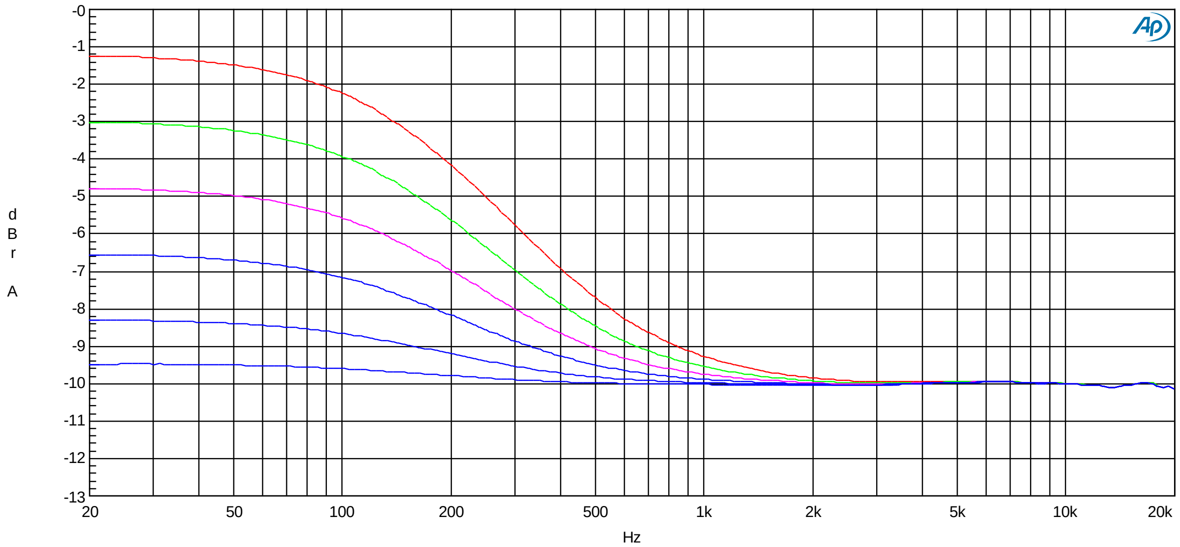


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	1	DSP Anlr.Ampl A	Left	
2	1	Green	Solid	1	DSP Anlr.Ampl A	Left	
3	1	Magenta	Solid	1	DSP Anlr.Ampl A	Left	

FREQUENCY RESPONSE，DIN=-10db BASS_BB=1 BC=0 m.at27

Figure 34 FREQUENCY RESPONSE，DIN=-10db BASS_BB=1 BC=0

Audio Precision 12/05/11 16:07:16

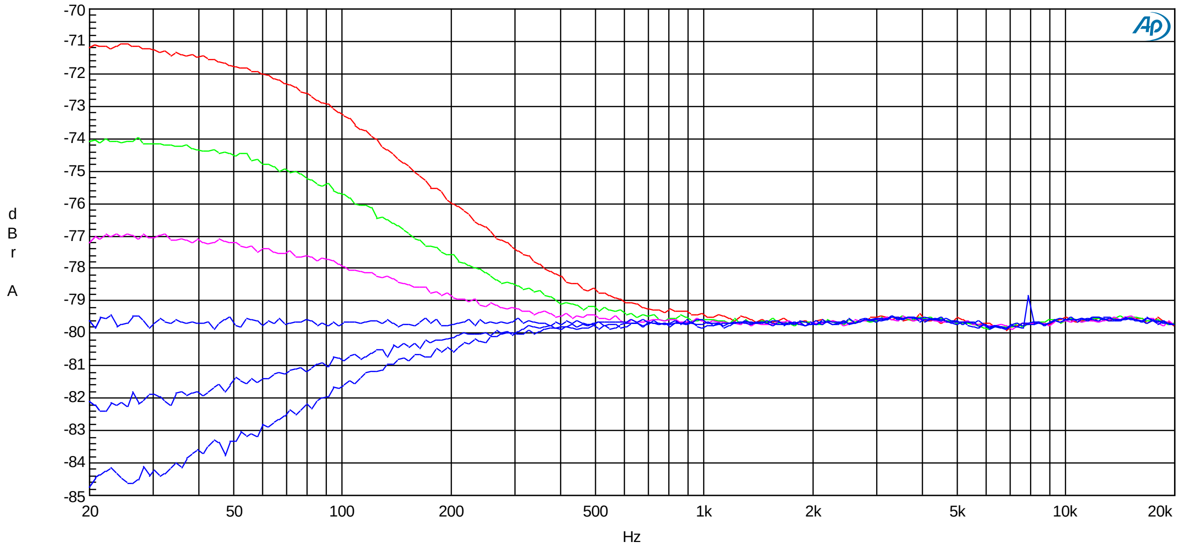


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	1	DSP Anlr.Ampl A	Left	
2	1	Green	Solid	1	DSP Anlr.Ampl A	Left	
3	1	Magenta	Solid	1	DSP Anlr.Ampl A	Left	

FREQUENCY RESPONSE，DIN=-10db BASS_BB=1 BC=1 m.at27

Figure 35 FREQUENCY RESPONSE，DIN=-10db BASS_BB=1 BC=1

Audio Precision 12/05/11 15:38:12

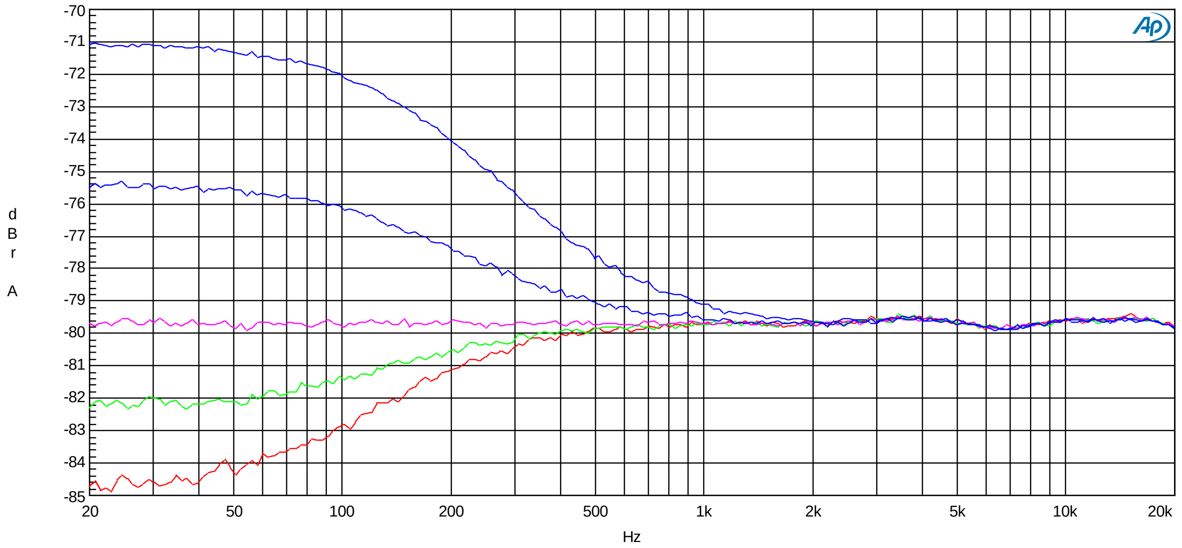


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	1	DSP Anlr.Ampl A	Left	
2	1	Green	Solid	1	DSP Anlr.Ampl A	Left	
3	1	Magenta	Solid	1	DSP Anlr.Ampl A	Left	

FREQUENCY RESPONSE，DIN=-80db BASS_BB=0 BC=0 m.at27

Figure 36 FREQUENCY RESPONSE，DIN=-80db BASS_BB=0 BC=0

Audio Precision 12/05/11 15:45:24



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	1	DSP Anlr.Ampl A	Left	
2	1	Green	Solid	1	DSP Anlr.Ampl A	Left	
3	1	Magenta	Solid	1	DSP Anlr.Ampl A	Left	

FREQUENCY RESPONSE，DIN=-80db BASS_BB=0 BC=1 m.at27

Figure 37 FREQUENCY RESPONSE，DIN=-80db BASS_BB=0 BC=1

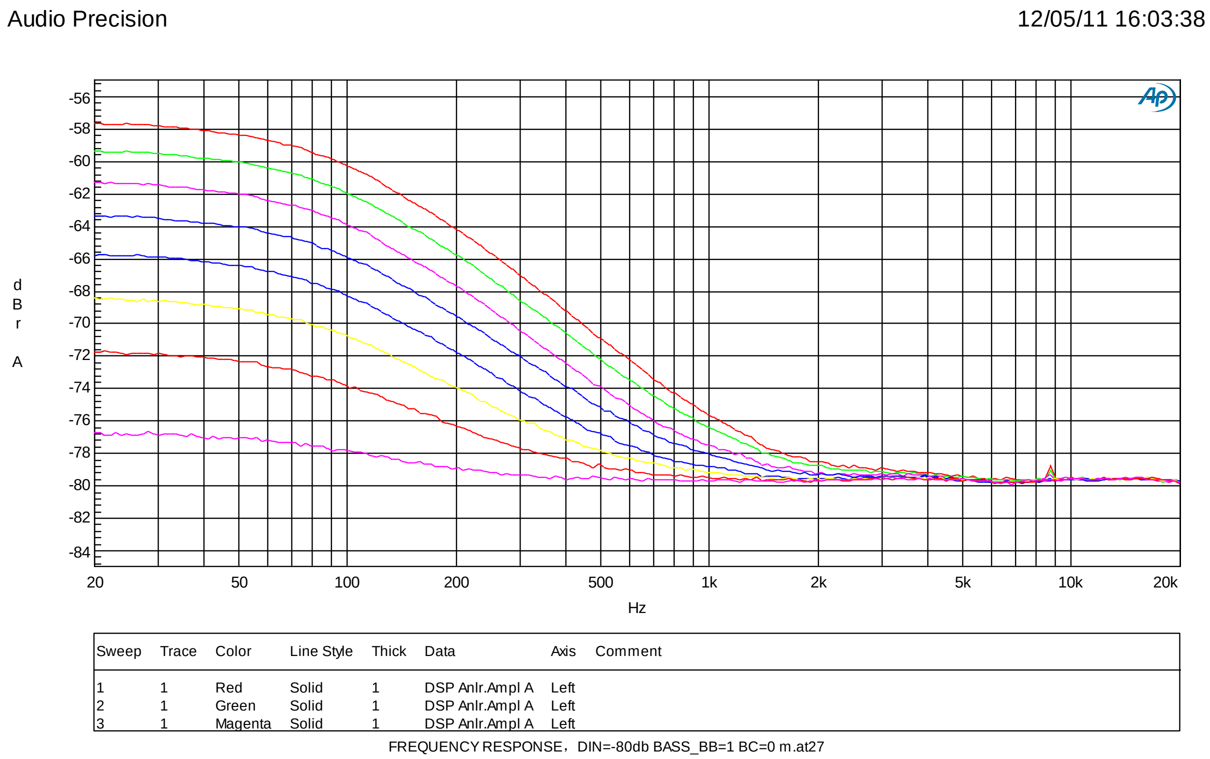


Figure 38 FREQUENCY RESPONSE，DIN=-10db BASS_BB=1 BC=0

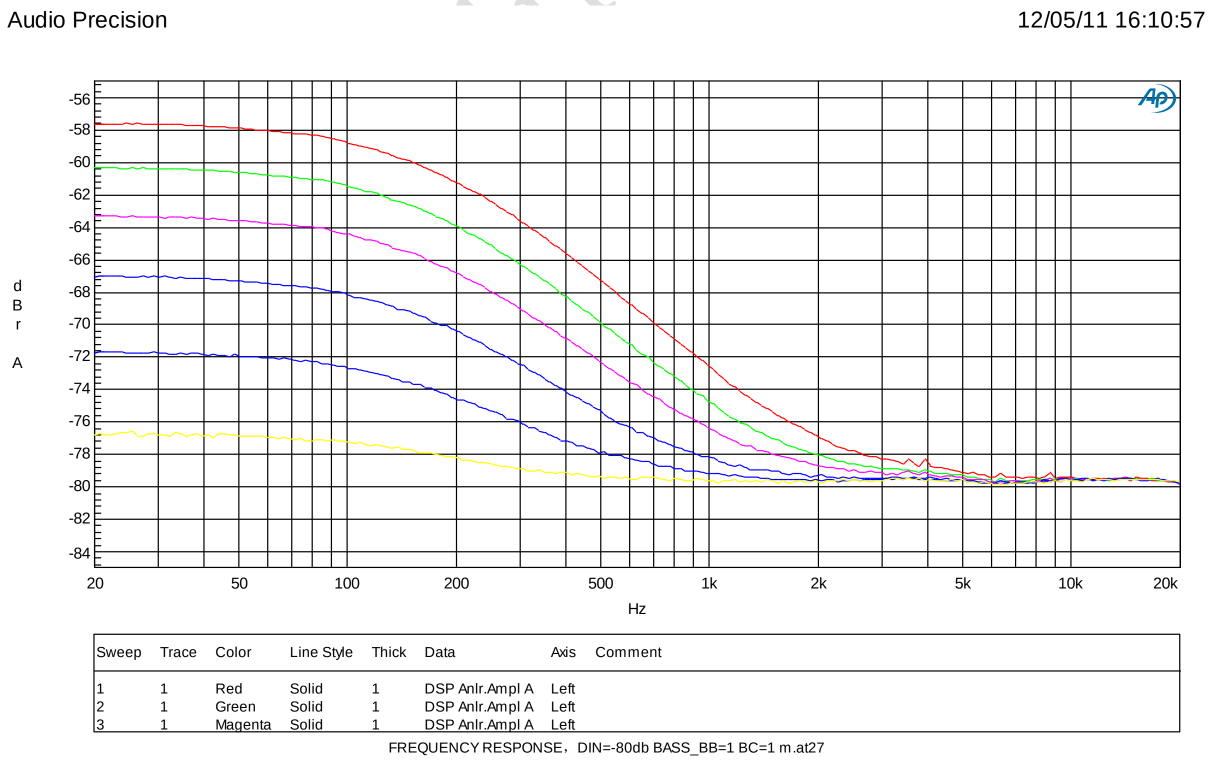
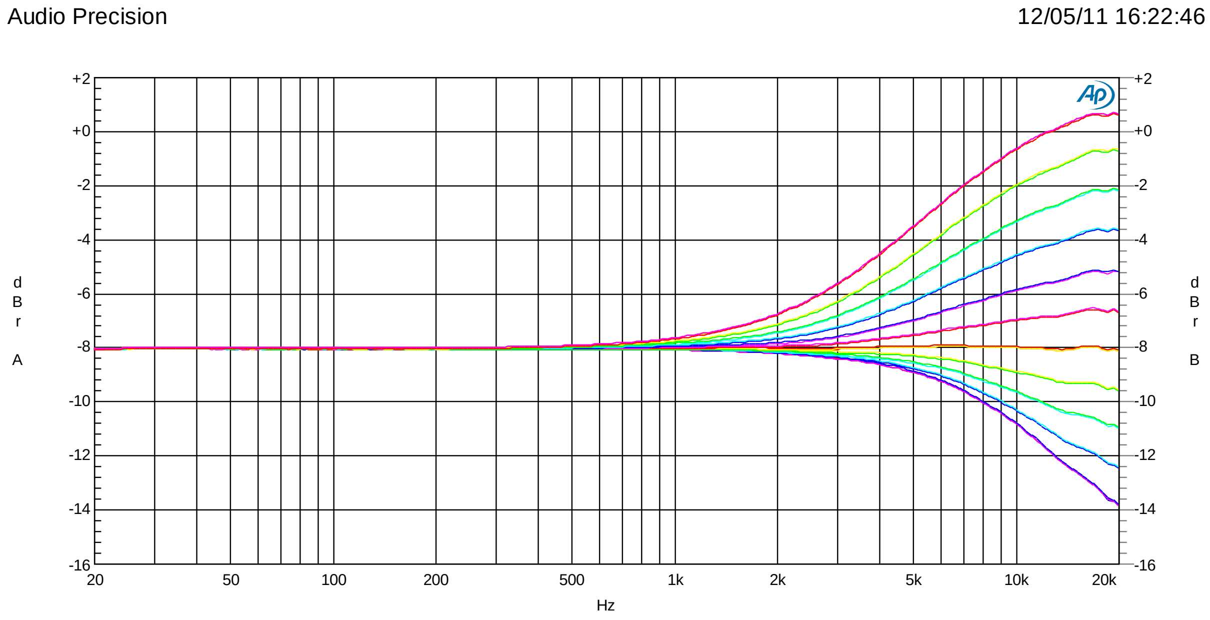


Figure 39 FREQUENCY RESPONSE，DIN=-10db BASS_BB=1 BC=1

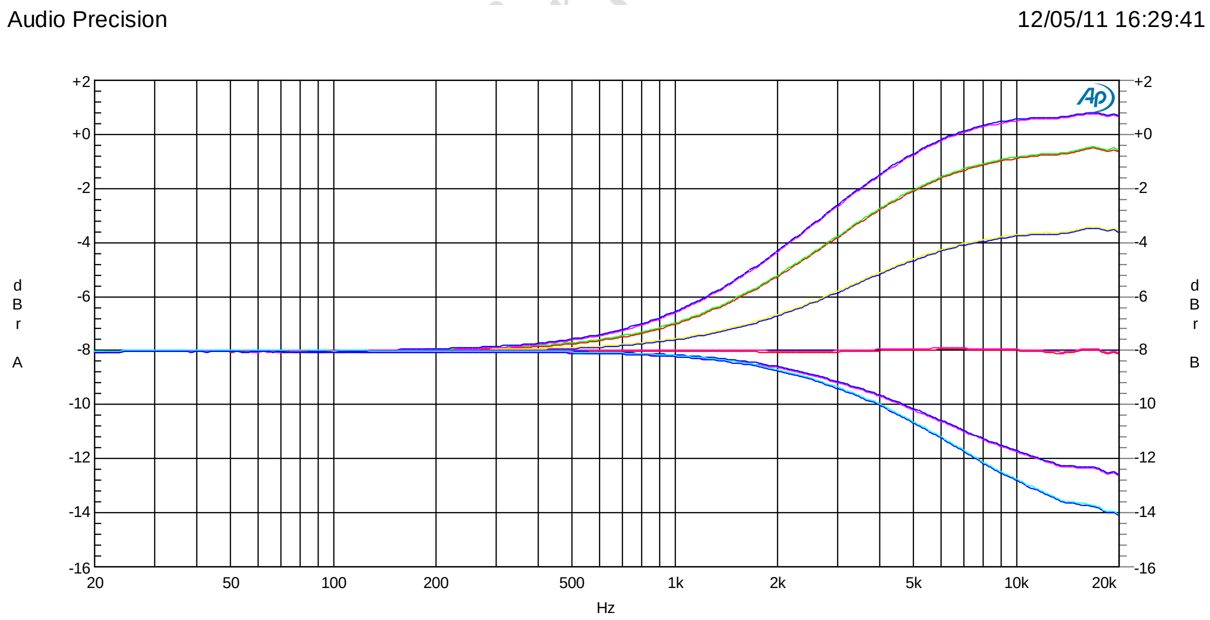
16.4. Treble Filter Characteristic



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	1	DSP Anlr.Ampl A	Left	
1	2	Green	Solid	1	DSP Anlr.Ampl B	Right	
2	1	Magenta	Solid	1	DSP Anlr.Ampl A	Left	

treble，DIN=-8dbFS TC=0.at27

Figure 40 treble，DIN=-8dbFS TC=0



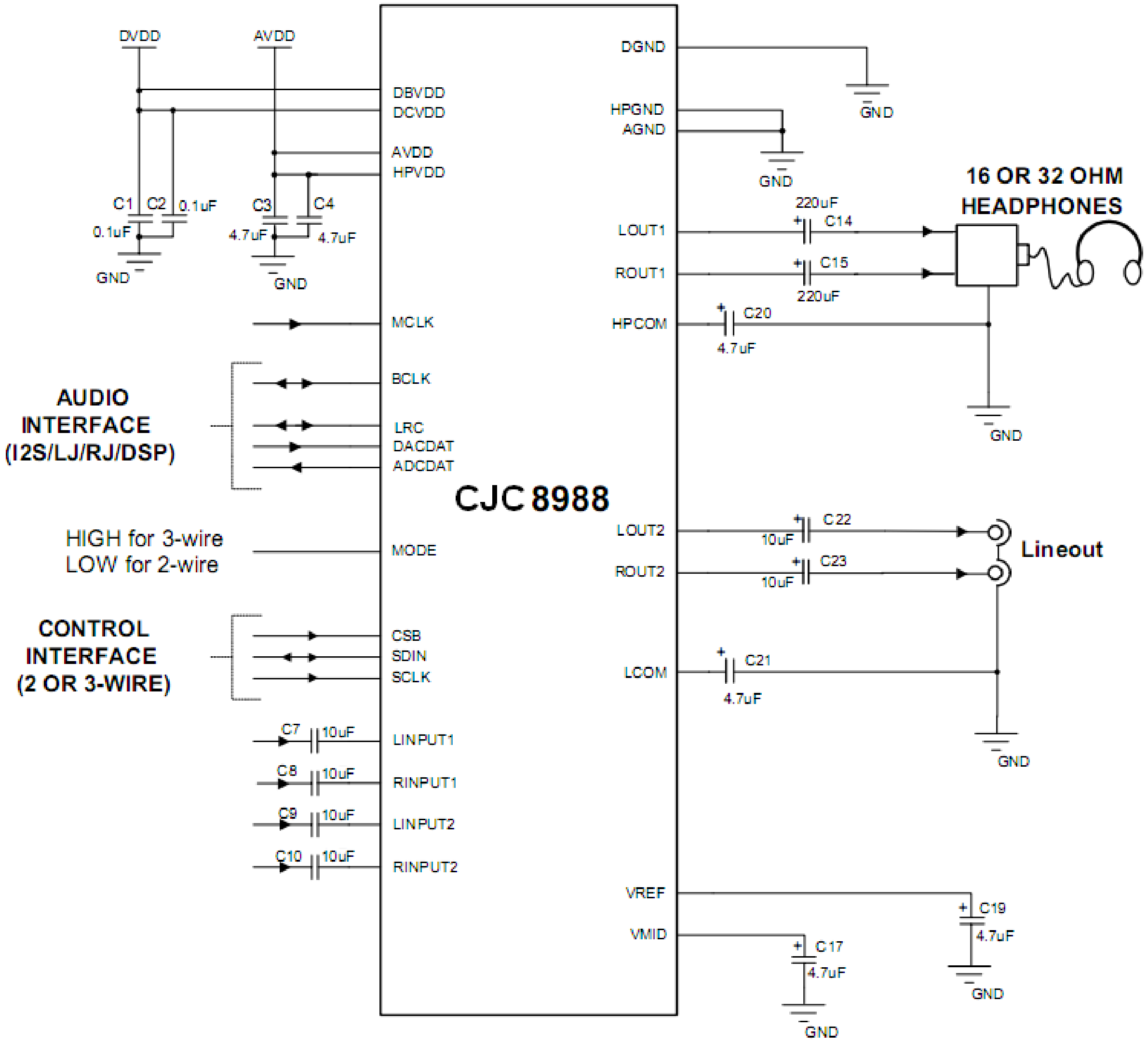
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	1	DSP Anlr.Ampl A	Left	
1	2	Green	Solid	1	DSP Anlr.Ampl B	Right	
2	1	Magenta	Solid	1	DSP Anlr.Ampl A	Left	

treble，DIN=-8dbFS TC=1.at27

Figure 41 treble，DIN=-8dbFS TC=1

17. APPLICATIONS INFORMATION

17.1. RECOMMENDED EXTERNAL COMPONENTS



Layout Notes:

1. C1 to C4, C17, C19, C20 and C21 should be as close to the relative CJC8988 connecting pin as possible.
2. For capacitors C7 to C10, C14, C15, C22 and C23 it is recommended that low ESR components are used.
3. HPCOM and LCOM should be connected to GND at the connector.

Figure 42 Recommended External Components Diagram

17.2. LINE INPUT CONFIGURATION

When LINPUT1/RINPUT1 or LINPUT2/RINPUT2 are used as line inputs, the microphone boost should normally be disabled. In order to avoid clipping, the user must ensure that the input signal does not exceed AVDD. This may require a potential divider circuit in some applications. It is also recommended to remove RF interference picked up on any cables using a simple first-order RC filter, as high-frequency components in the input signal may otherwise cause aliasing distortion in the audio band. AC signals with no DC bias should be fed to the CJC8988 through a DC blocking capacitor, e.g. 10µF.

17.3. HEADPHONE OUTPUT CONFIGURATION

Analogue outputs LOUT1/ROUT1 and LOUT2/ROUT2, can drive a 16Ω or 32Ω headphone load, as shown in Figure 43.

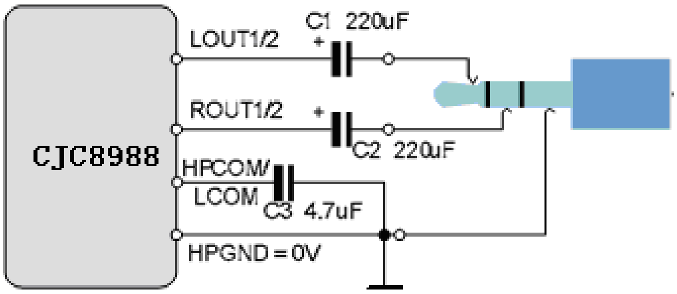


Figure 43 Recommended Headphone Output Configurations

The DC blocking capacitors C1 and C2 and the load resistance together determine the lower cut-off frequency, fc. Increasing the capacitance lowers fc, improving the bass response. Smaller capacitance values will diminish the bass response. Assuming a 16 Ohm load and C1, C2 = 220µF:

fc = 1 / 2π RLC1 = 1 / (2π x 16Ω x 220µF) = 45 Hz

17.4. LINE OUTPUT CONFIGURATION

The analogue outputs, LOUT1/ROUT1 and LOUT2/ROUT2, can be used as line outputs. Recommended external components are shown below.

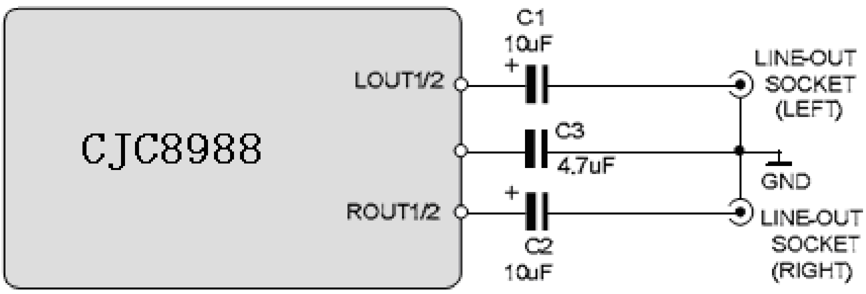


Figure 44 Recommended Circuit for Line Output

The DC blocking capacitors and the load resistance together determine the lower cut-off frequency, fc. Assuming a 10 kΩ load and C1, C2 = 1µF:

fc = 1 / 2π (RL+R1) C1 = 1 / (2π x 10.1kΩ x 1µF) = 16 Hz

Increasing the capacitance lowers fc, improving the bass response. Smaller values of C1 and C2 will diminish the bass response. The function of R1 and R2 is to protect the line outputs from damage when used improperly.

17.5. MINIMISING POP NOISE AT THE ANALOGUE OUTPUTS

To minimize any pop or click noise when the system is powered up or down, the following procedures are recommended.

POWER UP

- Switch on power supplies. By default the CJC8988 is in Standby Mode, the DAC is digitally muted and the Audio Interface, Line outputs and Headphone outputs are all OFF (DACMU = 1 Power Management registers 1 and 2 are all zeros).
- Enable Vmid and VREF.
- Enable DACs as required
- Enable line and / or headphone output buffers as required.
- Set DACMU = 0 to soft-un-mute the audio DACs.

POWER DOWN

- Set DACMU = 1 to soft-mute the audio DACs.
- Disable all output buffers.
- Switch off the power supplies.

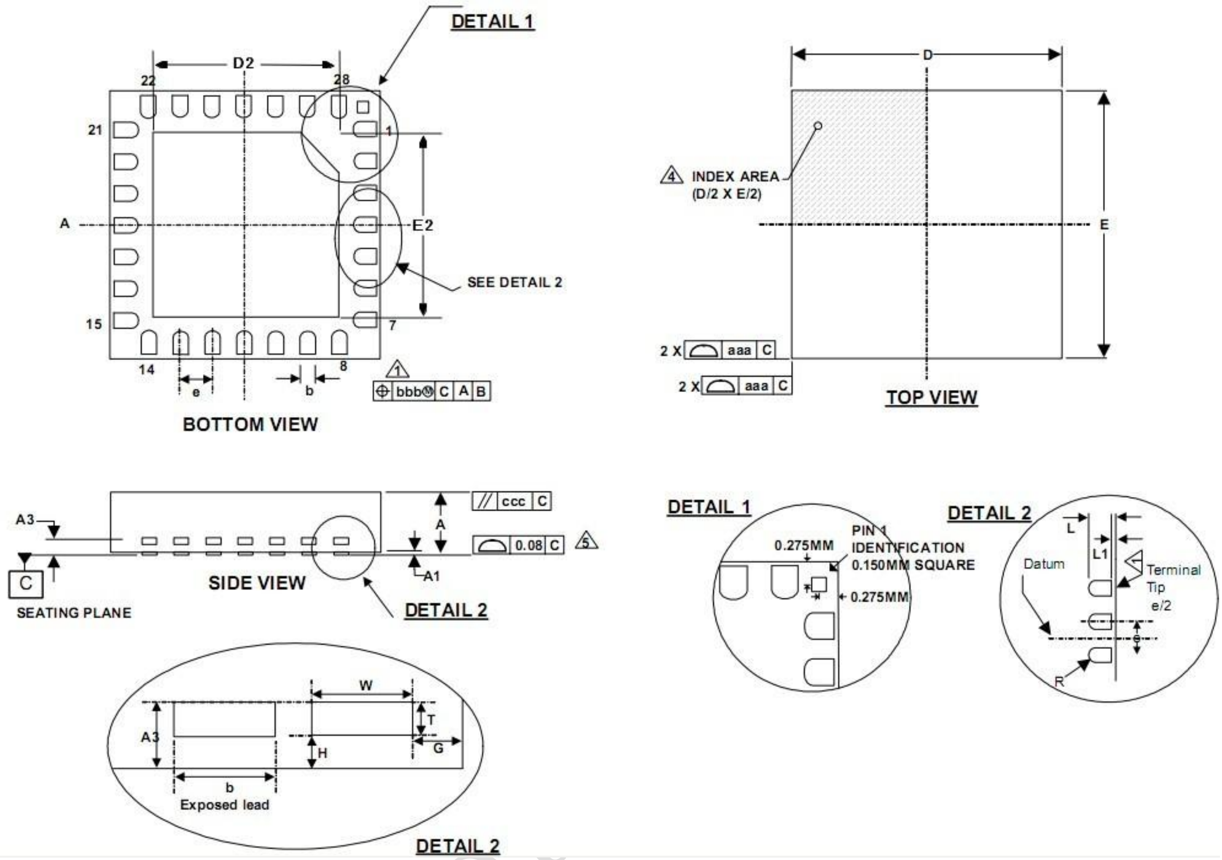
17.6. POWER MANAGEMENT EXAMPLES

OPERATION MODE	POWER MANAGEMENT (1)							POWER MANAGEMENT (2)					
	VREF	AINL/R	PGAs		ADCs		MBI	DACs		Output Buffers			
			PGL	PGR	ADL	ADR		DAL	DAR	LO1	RO1	LO2	RO2
Stereo Headphone Playback	1	0	0	0	0	0	0	1	1	1	1	0	0
Stereo Line-in Record	1	1	1	1	1	1	0	0	0	0	0	0	0
Stereo Microphone Record	1	1	1	1	1	1	1	0	0	0	0	0	0
Mono Microphone Record	1	1	1	0	1	0	1	0	0	0	0	0	0
Stereo Line-in to Headphone Out	1	1	0	0	0	0	0	0	0	1	1	0	0

Table 45 Register Settings for Power Management

18. PACKAGE DIMENSIONS

FL: 28 PIN COL QFN PLASTIC PACKAGE 4 x 4 x 0.55 mm BODY, 0.45 mm LEAD PITCH **DM050.E**



Symbols		Dimensions (mm)		
	MIN	NOM	MAX	NOTE
A	0.500	0.550	0.600	
A1	0	0.025	0.05	
A3		0.152 REF		
b	0.18	0.23	0.28	1
D	3.95	4.00	4.05	
D2	2.45	2.5	2.55	
E	3.95	4.00	4.05	
E2	2.45	2.5	2.55	
e		0.45 BSC		
G		0.535 REF		
H		0.076 REF		
L		0.40 REF		
L1		0.05 REF		5
T		0.076 REF		
W		0.230 REF		
Tolerances of Form and Position				
aaa	0.15			
bbb	0.10			
ccc	0.10			
REF:	JEDEC, MO-220			

Notes:

1. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 mm AND 0.30 mm FROM TERMINAL TIP.
2. ALL DIMENSIONS ARE IN MILLIMETRES.
3. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
4. REFER TOAPPLICATIONS NOTE WAN_0118 FOR FURTHER INFORMATION REGARDING PCB FOOTPRINTS AND QFN PACKAGE SOLDERING.
5. DEPENDING ON THE METHOD OF LEAD TERMINATION AT THE EDGE OF THE PACKAGE, PULL BACK (L1) MAY BE PRESENT.
6. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.