CJC8911

Mono CODEC for Portable Audio Applications

Edition	Author	Date	Description
V1.0	TF	2018.10	Mono CODEC for Portable Audio Applications
V2.0	TF	2022.11	Revise page

DESCRIPTION

The CJC8911 is a low power, high quality Mono CODEC designed for portable digital audio applications.

The device integrates complete interfaces to ONE line out ports. Advanced on-chip digital signal processing performs graphic equalizer, 3-D sound enhancement and automatic level control for the microphone or line input.

The CJC8911 can operate as a master or a slave, with various master clock frequencies including 12 or 24MHz for USB devices, or standard 256fs rates like 12.288MHz and 24.576MHz. Different audio sample rates such as 96kHz, 48kHz, 44.1kHz are generated directly from the master clock without the need for an external PLL.

The CJC8911 operates at supply voltages down to 1.8V, although the digital core can operate at voltages down to 1.5V to save power, and the maximum for all supplies is 3.3Volts. Different sections of the chip can also be powered down under software control. The CJC8911 is supplied in a very small and thin 4x4mm COL package, ideal for use in hand-held and portable systems.

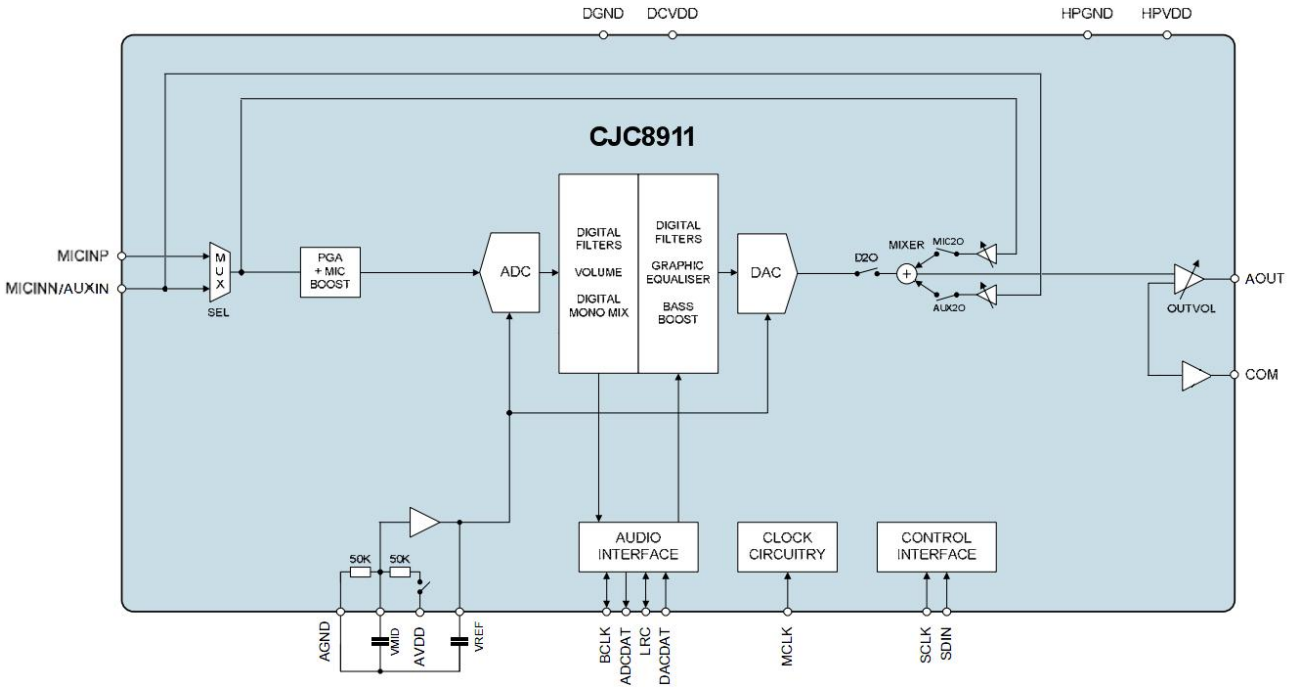
FEATURES

- DAC SNR 91dB ('A' weighted), THD –81.2dB at 48kHz, 1.8V
- ADC SNR 92.7dB ('A' weighted), THD -82dB at 48kHz, 1.8V
- Programmable ALC / Noise Gate
- Digital Graphic Equaliser
- Low Power
  -7mW playback (1.8V supplies)
  -13mW record and playback (1.8V supplies)
- Low Supply Voltages
  -Analogue 1.8V to 3.3V
  -Digital core: 1.5V to 3.3V
  -Digital I/O: 1.8V to 3.3V
- 256fs / 384fs or USB master clock rates: 12MHz, 24MHz
- Audio sample rates: 8, 11.025, 16, 22.05, 24, 32, 44.1, 48,
- 88.2, 96kHz generated internally from master clock
- 4x4mm COL package

APPLICATIONS

- Portable Multimedia players
- Multimedia handsets
- Handheld gaming

BLOCK DIAGRAM



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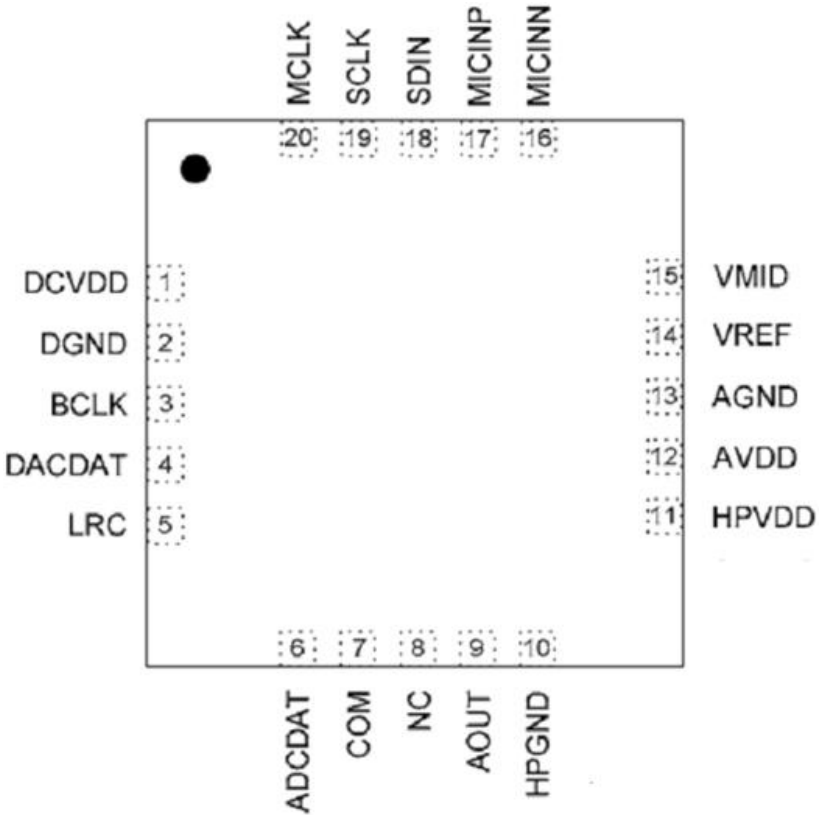
PIN CONFIGURATION AND DEVICE MARKING



PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
1	DCVDD	Supply	Digital Core Supply AND I/O Supply
2	DGND	Supply	Digital Ground (return path for both DCVDD and DBVDD)
3	BCLK	Digital Input / Output	Audio Interface Bit Clock
4	DACDAT	Digital Input	DAC Digital Audio Data
5	LRC	Digital Input / Output	Audio Interface Left / Right Clock
6	ADCDAT	Digital Output	ADC Digital Audio Data
7	COM	Analogue Input	AOUT common mode output
8	NC	--	--
9	AOUT	Analogue Output	Analogue Audio Output
10	HPGND	Supply	Supply for Analogue Output Drivers (AOUT)
11	HPVDD	Supply	Supply for Analogue Output Drivers (AOUT)
12	AVDD	Supply	Analogue Supply
13	AGND	Supply	Analogue Ground (return path for AVDD)
14	VREF	Analogue Output	Reference Voltage Decoupling Capacitor
15	VMID	Analogue Output	Midrail Voltage Decoupling Capacitor
16	MICINN	Analogue Input	MIC INPUT N
17	MICINP	Analogue Input	MIC INPUT P
18	SDIN	Digital Input / Output	Control Interface Data Input / 2-wire Acknowledge output
19	SCLK	Digital Input	Control Interface Clock Input
20	MCLK	Digital Input	Master Clock

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuous operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically to damage from excessive static voltages. Proper ESD precautions must be taken during handling of this device.

Chinaic Semiconductor tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltages	**-0.3V**	**+3.6V**
Voltage range digital inputs	**DGND -0.3V**	**DCVDD +0.3V**
Voltage range analogue inputs	**AGND -0.3V**	**AVDD +0.3V**
Operating temperature range, TA	**-25°C**	**+85°C**
Storage temperature after soldering	**-65°C**	**+150°C**

Notes:
1. Analogue and digital grounds must always be within 0.3V of each other.
2. All digital and analogue supplies are completely independent from each other.
3. DCVDD was equal to DBVDD.

RECOMMENDED OPERATION CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital supply range	**DCVDD**	**1.8**		**3.6**	**V**

(Core/Buffer)					
Analogue supplies range	AVDD, HPVDD	1.8		3.6	V
Ground	DGND,AGND, HPGND		0		V

ELECTRICAL CHARACTERISTICS

NORMAL MODE

Test Conditions

DCVDD = AVDD = HPVDD =1.8V , TA = +25℃, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Inputs (MICINP) to ADC out						
Full Scale Input Signal Level (for ADC 0dB Input at 0dB Gain)	VINFS	AVDD = 2.4V	0.690	0.727	0.763	Vrms
		AVDD = 1.8V	0.480	0.545	0.610	
Input Resistance	MIC	MIC to ADC, PGA gain = 0dB	16	22		kΩ
		MIC to ADC, PGA gain = +30dB	1.5	2.8		
Input Capacitance				10		pF
Signal to Noise Ratio (A-weighted)	SNR	AVDD = 2.4V		94		dB
		AVDD = 1.8V		92		
Total Harmonic Distortion + Noise	THD+N	-6dBr input, AVDD = 2.4V		-86		dB
		-2dBr input, AVDD = 1.8V		-82		
Analogue Outputs (AOUT)						
0dB Full scale output voltage	VOUTFS	AVDD = 2.4V	0.690	0.727	0.763	Vrms
		AVDD = 1.8V	0.507	0.545	0.583	
Signal to Noise Ratio (A-weighted)	SNR	AVDD = 2.4V		96		dB
		AVDD = 1.8V		93		
Total Harmonic Distortion + Noise	THD+N	-0dBr input, AVDD = 2.4V		80		dB
		-4dBr input, AVDD = 2.4V		87		
		-0dBr input, AVDD = 1.8V		80		
		-6dBr input, AVDD = 1.8V		84		

Test Conditions

DCVDD = AVDD = HPVDD =1.8V , TA = +25 ℃, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Reference Levels						
Midrail Reference Voltage	VMID		–3%	AVDD/2	+3%	V
Buffered Reference Voltage	VREF		–3%	AVDD/2	+3%	V
Digital Input / Output						
Input HIGH Level	VIH		0.7×DBVDD			V
Input LOW Level	VIL				0.3×DCVDD	V
Output HIGH Level	VOH	IOH = +1mA	0.9×DBVDD			V
Output LOW Level	VOL	IOL = -1mA			0.1×DCVDD	V

Test Conditions

DCVDD = AVDD = HPVDD =1.8V , TA = +25°C , 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to Line-Out (AOUT with 10kΩ load)						
Signal to Noise Ratio (A-weighted)	SNR	AVDD = 2.4V COM=1		93		dB
		AVDD=1.8V COM=0		91		
Total Harmonic Distortion + Noise	THD+N	AVDD = 2.4V COM=1		76		dB
		AVDD=1.8V COM=0		81		
Channel Separation		min		101		dB
		1kHz signal		111		

COM MODE

Test Conditions

DCVDD = AVDD = HPVDD =1.8V , TA = +25℃, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Inputs (MICINP) to ADC out						
Full Scale Input Signal Level (for ADC 0dB Input at 0dB Gain)	VINFS	AVDD = 2.4V	0.690	0.727	0.763	Vrms
		AVDD = 1.8V	0.480	0.545	0.610	
Input Resistance	MIC	MIC to ADC, PGA gain = 0dB	16	22		kΩ
		MIC to ADC, PGA gain = +30dB	1.5	2.8		
Input Capacitance				10		pF
Signal to Noise Ratio (A-weighted)	SNR	AVDD = 2.4V		97		dB
		AVDD = 1.8V		94		
Total Harmonic Distortion + Noise	THD+N	-6dBr input, AVDD = 2.4V		-86		dB
		-2dBr input, AVDD = 1.8V		-82		
Analogue Outputs (AOUT)						
0dB Full scale output voltage	VOUTFS	AVDD = 2.4V	0.690	0.727	0.763	Vrms
		AVDD = 1.8V	0.507	0.545	0.583	
Signal to Noise Ratio (A-weighted)	SNR	AVDD = 2.4V COM=1		92		dB
		AVDD = 1.8V COM=1		91		
Total Harmonic Distortion + Noise	THD+N	-1dBr input, AVDD = 2.4V COM=1		76		dB
		-2dBr input, AVDD = 1.8V COM=1		72		

POWER CONSUMPTION

The power consumption of the CJC8911 depends on the following factors.

- Supply voltages: Reducing the supply voltages also reduces supply currents, and therefore results in significant power savings, especially in the digital sections of the CJC8911.
- Operating mode: Significant power savings can be achieved by always disabling parts of the CJC8911 that are not used (e.g. mic pre-amps, unused outputs, DAC, ADC, etc.)

AVDD=HPVDD=DCVDD =1.8V AIN=NONE DIN=NONE						
MODE		DCVDD	AVDD	HPVDD	SUM	UNIT
NORMAL	ADC	0.713	2.65	0	3.36	mA
	DAC LINEOUT	1.447	2.34	0.197	3.98	
	BYPASS	0.294	1.92	0.328	2.54	
	POWER DOWN	0.9	0.1	0.1	1.1	uA
COM	ADC	0.73	2.66	0.036	3.43	mA
	POWER DOWN	0.9	0.1	0.1	1.1	uA

Notes:

1. All figures are at TA = +25 ℃, Slave Mode, fs = 48kHz, MCLK = 12.288 MHz (256fs),

SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCK TIMING

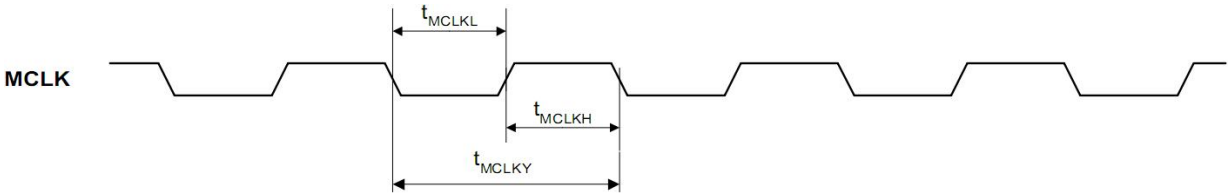


Figure 1 System Clock Timing Requirements

Test Conditions

CLKDIV2=0, DCVDD = 1.8V, DGND = 0V, TA = +25℃, Slave Mode fs = 48kHz, MCLK = 384fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
System Clock Timing Information					
MCLK System clock pulse width high	TMCLKL	21			ns
MCLK System clock pulse width low	TMCLKH	21			ns
MCLK System clock cycle time	TMCLKY	54			ns
MCLK duty cycle	TMCLKDS	60:40		40:60	ns

Test Conditions

CLKDIV2=1, DCVDD = 1.8V, DGND = 0V, TA = +25 C, Slave Mode fs = 48kHz, MCLK = 384fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
System Clock Timing Information					
MCLK System clock pulse width high	TMCLKL	10			ns
MCLK System clock pulse width low	TMCLKH	10			ns
MCLK System clock cycle time	TMCLKY	27			ns

AUDIO INTERFACE TIMING – MASTER MODE

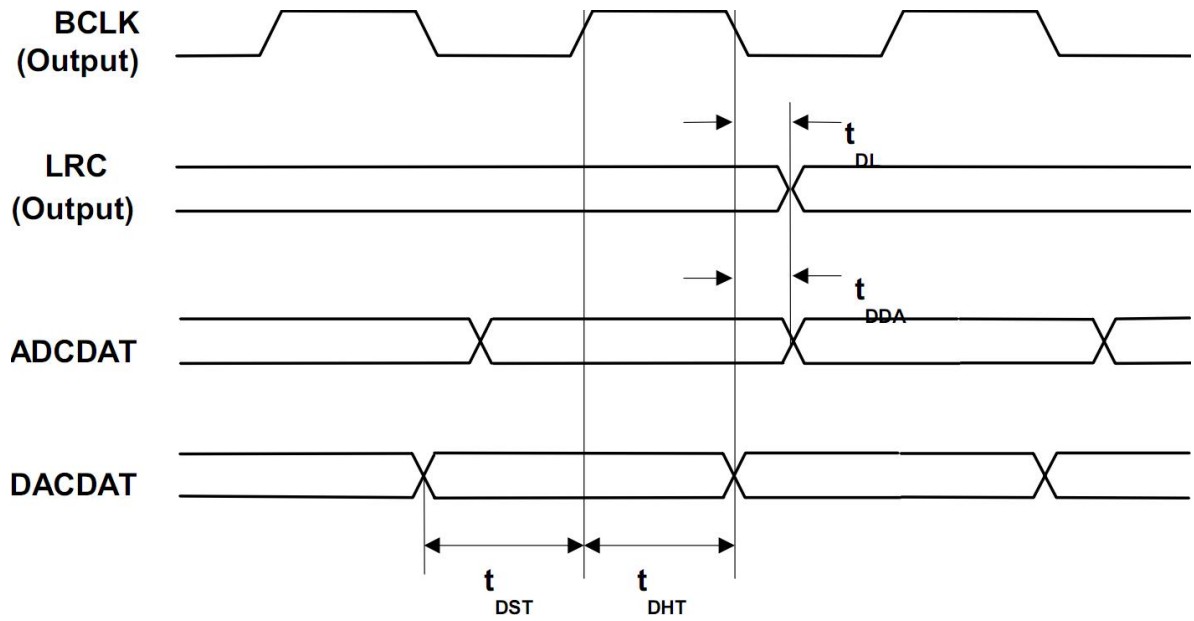


Figure 2 Digital Audio Data Timing – Master Mode

Test Conditions

DCVDD = 1.8V, DGND = 0V, TA = +25 C, Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Bit Clock Timing Information					
BCLK rise time (10pF load)	tBCLKR			3	ns
BCLK fall time (10pF load)	tBCLKF			3	ns
BCLK duty cycle (normal mode, BCLK = MCLK/n)	tBCLKDS		50:50		
BCLK duty cycle (USB mode, BCLK = MCLK)	tBCLKDS		Tmclkds		
Audio Data Input Timing Information					
DACLRC propagation delay from BCLK falling edge	tDL			10	ns
ADCDAT propagation delay from BCLK falling edge	tDDA			10	ns
DACDAT setup time to BCLK rising edge	tDST	10			ns
DACDAT hold time from BCLK rising edge	tDHT	10			ns

AUDIO INTERFACE TIMING – SLAVE MODE

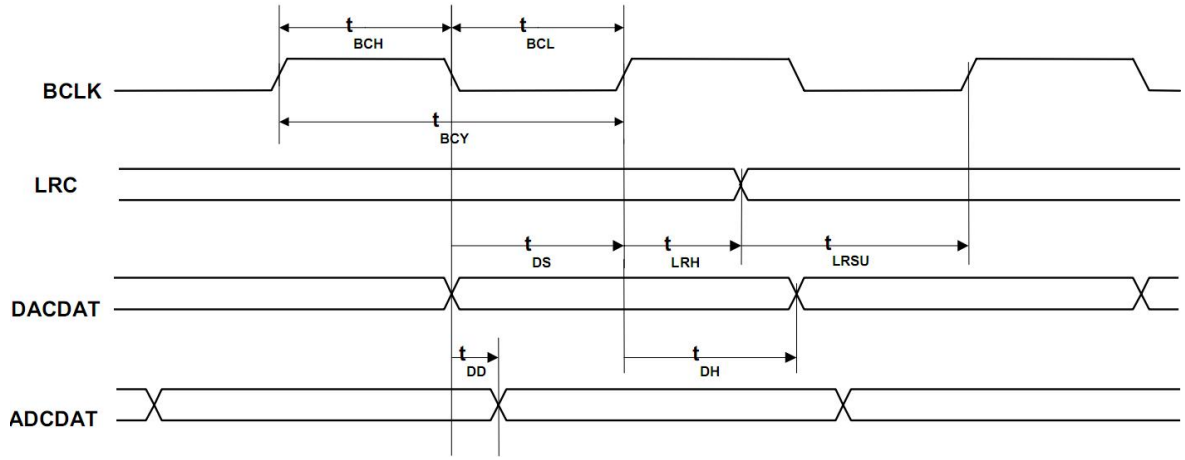


Figure 3 Digital Audio Data Timing – Slave Mode

Test Conditions

DCVDD = 1.8V, DGND = 0V, TA = +25 C, Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
BCLK cycle time	tBCY	50			ns
BCLK pulse width high	tBCH	20			ns
BCLK pulse width low	tBCL	20			ns
DACLRC set-up time to BCLK rising edge	tLRSU	10			ns
DACLRC hold time from BCLK rising edge	tLRH	10			ns
DACDAT hold time from BCLK rising edge	tDH	10			ns
ADCDAT propagation delay from BCLK falling edge	tDD			10	ns

Note:

BCLK period should always be greater than or equal to MCLK period.

CONTROL INTERFACE TIMING – 2-WIRE MODE

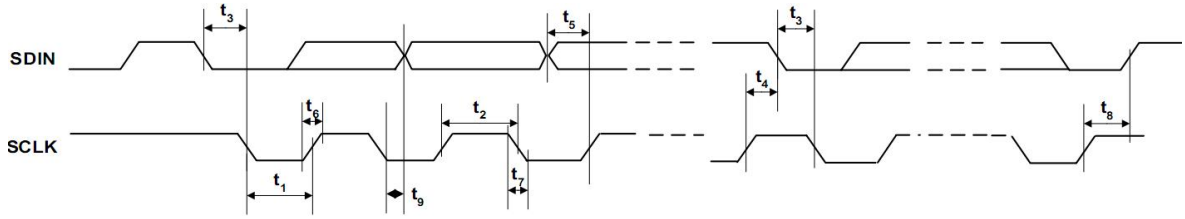


Figure 4 Control Interface Timing – 2-Wire Serial Control Mode

Test Conditions

DCVDD = 1.8V,DGND = 0V, TA = +25 C, Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK Frequency		0		526	kHz
SCLK Low Pulse-Width	t1	1.3			us
SCLK High Pulse-Width	t2	600			ns
Hold Time (Start Condition)	t3	600			ns
Setup Time (Start Condition)	t4	600			ns
Data Setup Time	t5	100			ns
SDIN, SCLK Rise Time	t6			300	ns
SDIN, SCLK Fall Time	t7			300	ns
Setup Time (Stop Condition)	t8	600			ns
Data Hold Time	t9			900	ns
Pulse width of spikes that will be suppressed	tps	0		5	ns

INTERNAL POWER ON RESET CIRCUIT

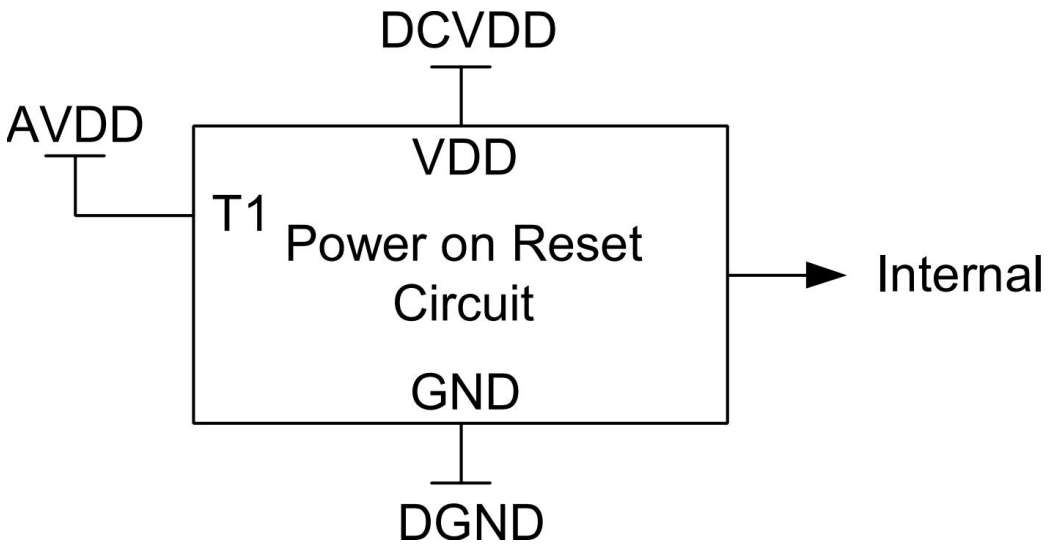


Figure 5 Internal Power on Reset Circuit Schematic

The CJC8911 includes an internal Power-On-Reset Circuit, as shown in Figure 5, which is used to reset the digital logic into a default state after power up. The power on reset circuit is powered from DCVDD and monitors DCVDD and AVDD. It asserts PORB low if DCVDD or AVDD are below a minimum threshold.

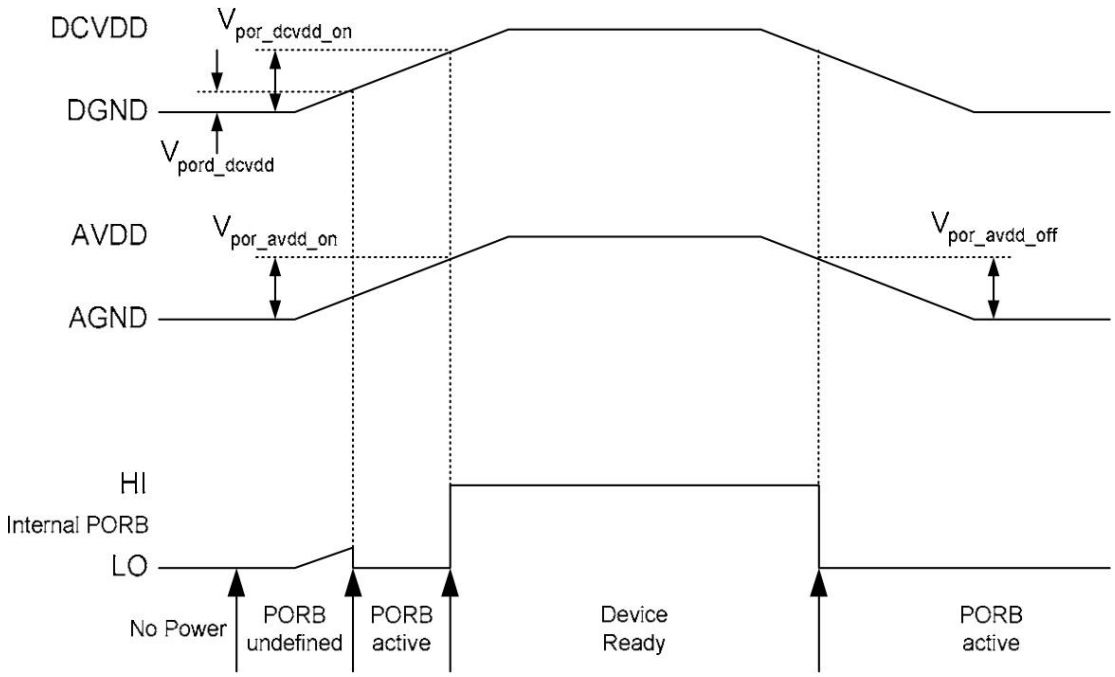


Figure 6 Typical Power-Up Sequence

Figure 6 shows a typical power-up sequence. When DCVDD and AVDD rise above the minimum thresholds, Vpord_dcvdd and Vpord_avdd, there is enough voltage for the circuit to guarantee the Power on Reset is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. When DCVDD rises to Vpor_dcvdd_on and AVDD rises to Vpor_avdd_on, PORB is released high and all registers are in their default state and writes to the control interface may take place. If DCVDD and AVDD rise at different rates then PORB will only be released when DCVDD and AVDD have both exceeded the Vpor_dcvdd_on and Vpor_avdd_on thresholds.

On power down, PORB is asserted low whenever DCVDD drops below the minimum threshold Vpor_dcvdd_off or AVDD drops below the minimum threshold Vpor_avdd_off.

SYMBOL	MIN	TYP	MAX	UNIT
Vpord_dcvdd	0.4	0.6	0.8	V
Vpor_dcvdd_on	0.9	1.26	1.6	V
Vpor_avdd_on	0.5	0.7	0.9	V
Vpor_avdd_off	0.4	0.6	0.8	V

Table 1 Typical POR Operation (typical values, not tested)

DEVICE DESCRIPTION

INTRODUCTION

The CJC8911 is a low power audio codec offering a combination of high quality audio, advanced features, low power and small size. These characteristics make it ideal for portable digital audio applications such as MP3 and minidisk player / recorders.Mono 24-bit multi-bit delta sigma ADCs and DACs are used with oversampling digital interpolation and decimation filters.

The device includes TWO analogue inputs that as MIC input, that is MICINP and MICINN . As the MIC phone is single end mode we can use MICINP as input PIN. If the MIC phone is differential then MICINP and MICINN should be use. A programmable gain amplifier with automatic level control (ALC) keeps the recording volume constant. The on-chip Mono ADC and DAC are of a high quality using a multi-bit, low-order oversampling architecture to deliver optimum performance with low power consumption.

The DAC output signal first enters an analogue mixer where an analogue input and/or the post-ALC signal can be added to it. This mix is available on line outputs.

The CJC8911 has a configurable digital audio interface where ADC data can be read and digital audio playback data fed to the DAC. It supports a number of audio data formats including I2 S, DSP Mode (a burst mode in which frame sync plus 2 data packed words are transmitted), MSB-First, left justified and and can operate in master or slave modes.

The CJC8911 uses a unique clocking scheme that can generate many commonly used audio sample rates from either a 12.00MHz USB clock or an industry standard 256/384 fs clock. This feature eliminates the common requirement for an external phase-locked loop (PLL) in applications where the master clock is not an integer multiple of the sample rate. Sample rates of 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz, 88.2kHz and 96kHz can be generated.

The digital filters used for recording and playback are optimised for each sampling rate used.

The design of the CJC8911 has given much attention to power consumption without compromising performance. It operates at very low voltages, and includes the ability to power off parts of the circuitry under software control, including standby and power off modes.

INPUT SIGNAL PATH

The input signal path consists of a MIC inputs, followed by a PGA (programmable gain amplifier) and an optional microphone gain boost. The gain of the PGA can be controlled either by the user or by the on-chip ALC function (see Automatic Level Control).

The signal then enters an ADC where it is digitized.

SIGNAL INPUTS

The CJC8911 has two high impedance, low capacitance AC coupled analogue inputs, MICINP / MICINN. Inputs can be configured as microphone or line level by enabling or disabling the microphone gain boost.

MIC_DIF_EN control bits (see Table 2) are used to select independently between single-ended input and internally generated differential products (MICINP-MICINN). The choice of differential signal OR single-ended input, MICINP-MICINN or MICINP, which is chosen using MIC_DIF_EN (refer to Table 2).

The CJC8911 can be set up to convert differential or one single ended mono signal by applying the differential signal to MICINP/MICINN or the single ended signal MICINP. For example ,by setting MIC_DIF_EN to high, the differential signal (MICINP-MICINN) go to PGA path.

The signal inputs are biased internally to the reference voltage VREF. Whenever the line inputs are muted or the device placed into standby mode, the inputs are kept biased to VREF using special anti-thump circuitry. This reduces any audible clicks that may otherwise be heard when changing inputs.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R32 (20h) ADC Signal Path Control	8	MIC_DIF_EN	0	0: MICINP single-ended input into ADC 1: MICINP and MICINN differential input into ADC
	5:4	MIC BOOST	00	Microphone Gain Boost 00 = Boost off (bypassed) 01 = 13dB boost 10 = 20dB boost 11 = 29dB boost

Table 2 MIC input control and gain adjust

PGA CONTROL

The PGA matches the input signal level to the ADC input range. The PGA gain is logarithmically adjustable from +30dB to –17.25dB in 0.75dB steps. Each PGA can be controlled either by the user or by the ALC function (see Automatic Level Control). When ALC is enabled for one or both channels, then writing to the corresponding PGA control register has no effect.

The gain is independently adjustable on both MICINP Line Inputs. Additionally, by controlling the register bits IVU, the gain settings can be simultaneously updated. Setting the ZCEN bits enables a zero-cross detector which ensures that PGA gain changes only occur when the signal is at zero, eliminating any zipper noise.If zero cross is enabled a timeout is also available to update the gain if a zero cross does not occur. This function may be enabled by setting TOEN in register R23 (17h).

The inputs can also be muted in the analogue domain under software control. The software control registers are shown in Table 3.If zero crossing is enabled, it is necessary to enable zero cross timeout to un-mute the input PGAs.This is because their outputs will not cross zero when muted. Alternatively, zero cross can be disabled before sending the un-mute command.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 (00h) Channel PGA	8	IVU	0	Volume Update 0 = Store INVOL in intermediate latch (no gain change) 1 = Update gains
	7	INMUTE	1	Channel Input Analogue Mute 1 = Enable Mute 0 = Disable Mute Note: LIVU must be set to un-mute.
	6	ZCEN	0	Channel Zero Cross Detector 1 = Change gain on zero cross only 0 = Change gain immediately
	5:0	INVOL [5:0]	010111 (0dB)	Channel Input Volume Control 111111 = +30dB 111110 = +29.25dB . . 0.75dB steps down to 000000 = -17.25dB
R23 (17h) Additional Control (1)	0	TOEN	0	Timeout Enable 0 : Timeout Disabled 1 : Timeout Enabled

Table 3 Input PGA Software Control

ANALOGUE TO DIGITAL CONVERTER (ADC)

The CJC8911 uses a multi-bit, oversampled sigma-delta ADC for each channel. The use of multi-bit feedback and high oversampling rates reduces the effects of jitter and high frequency noise. The ADC Full Scale input level is proportional to AVDD. With a 1.8V supply voltage, the full-scale level is 1.0 Volts r.m.s. Any voltage greater than full scale may overload the ADC and cause distortion.

ADC DIGITAL FILTER

The ADC filters perform true 24 bit signal processing to convert the raw multi-bit oversampled data from the ADC to the correct sampling frequency to be output on the digital audio interface. The digital filter path is illustrated in Figure 7.

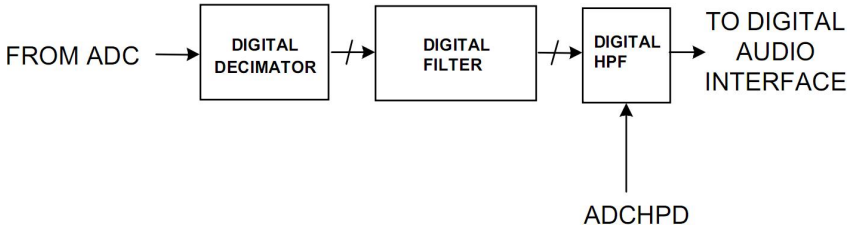


Figure 7 ADC Digital Filter

The ADC digital filters contain a digital high-pass filter, selectable via software control.The high-pass filter response is detailed in the Digital Filter Characteristics section.When the high-pass filter is enabled the DC offset is continuously calculated and subtracted from the input signal.By setting HPOR, the last calculated DC offset value is stored when the high-pass filter is disabled and will continue to be subtracted from the input signal.If the DC offset is changed,the stored and subtracted value will not change unless the high-pass filter is enabled.This feature can be used for calibration purposes.In addition the high-pass filter may be enabled separately on the channels (see Table 4).

The output data format can be programmed by the user to accommodate Mono or monophonic recording on both inputs. The polarity of the output signal can also be changed under software control. The software control is shown in Table 4.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) ADC and DAC Control	5	ADCPOL	00	0 = Polarity not inverted 1 = Polarity invert
	4	HPOR	0	Store dc offset when high-pass filter disabled 1 = store offset 0 = clear offset
	0	ADCHPD	0	ADCHPD determine high-pass filter

				behaviour 1 = HPF on 0 = HPF off

Table 4 ADC Signal Path Control

DIGITAL ADC VOLUME CONTROL

The output of the ADCs can be digitally amplified or attenuated over a range from –97dB to +30dB in 0.5dB steps. The volume of each channel can be controlled separately. The gain for a given eight-bit code X is given by:

0.5 × (X-195) dB for 1 ≤ X ≤ 255; MUTE for X = 0

The AVU control bits control the loading of digital volume control data. When AVU are set to 0, the ADCVOL control data will be loaded into the respective control register, but will not actually change the digital gain setting. Both gain settings are updated when either AVU are set to 1. This makes it possible to update the gain of both channels simultaneously.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R21 (15h) ADC Digital Volume	7:0	ADCVOL [7:0]	11000011 (0dB)	ADC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -97dB 0000 0010 = -96.5dB ... 0.5dB steps up to 1111 1111 = +30dB
	8	AVU	0	ADC Volume Update 0 = Store ADCVOL in intermediate latch (no gain change) 1 = Update gains

Table 5 ADC Digital Volume Control

AUTOMATIC LEVEL CONTROL (ALC)

The CJC8911 has an automatic level control that aims to keep a constant recording volume irrespective of the input signal level. This is achieved by continuously adjusting the PGA gain so that the signal level at the ADC input remains constant. A digital peak detector monitors the ADC output and changes the PGA gain if necessary. Note that when the ALC function is enabled, the settings of registers 0 and 1 (INVOL, IVU, IZC, INMUTE) are ignored.

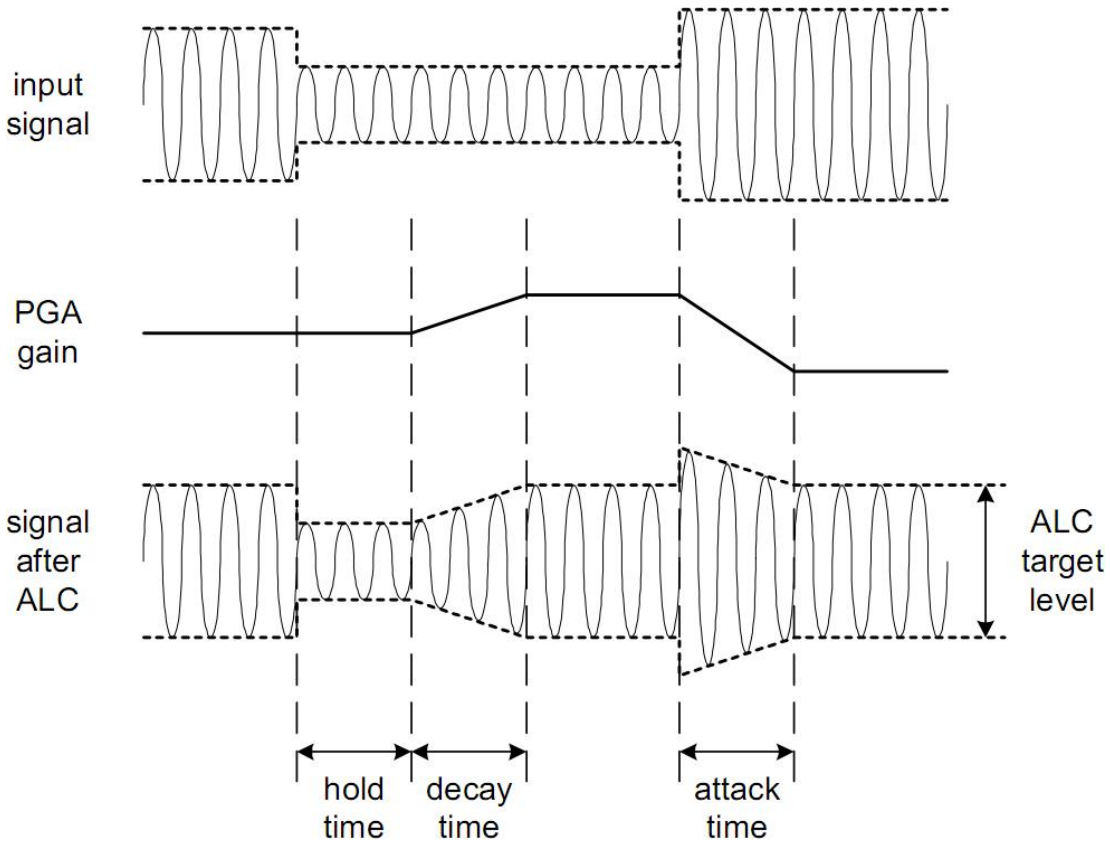


Figure 8 ALC Operation

The ALC function is enabled using the ALCSEL control bits. When enabled, the recording volume can be programmed between –6dB and –28.5dB (relative to ADC full scale) using the ALC register bits. An upper limit for the PGA gain can be imposed by setting the MAXGAIN control bits.

HLD, DCY and ATK control the hold, decay and attack times, respectively:

Hold time is the time delay between the peak level detected being below target and the PGA gain beginning to ramp up. It can be programmed in power-of-two (2n) steps, e.g. 2.67ms, 5.33ms, 10.67ms etc. up to 43.7s. Alternatively, the hold time can also be set to zero. The hold time only applies to gain ramp-up, there is no delay before ramping the gain down when the signal level is above target.

Decay (Gain Ramp-Up) Time is the time that it takes for the PGA gain to ramp up across 90% of its range (e.g. from –15B up to 27.75dB). The time it takes for the recording level to return to its target value therefore depends on both the decay time and on the gain adjustment required. If the gain adjustment is small, it will be shorter than the decay time. The decay time can be programmed in power-of-two (2) steps, from 24ms, 48ms, 96ms, etc. to 24.58s.

Attack (Gain Ramp-Down) Time is the time that it takes for the PGA gain to ramp down across 90% of its range (e.g. from 27.75dB down to -15B gain). The time it takes for the recording level to return to its target value therefore depends on both the attack time and on the gain adjustment required. If the gain adjustment is small, it will be shorter than the attack time. The attack time can be programmed in power-of-two (2) steps, from 6ms, 12ms, 24ms, etc. to 6.14s.

When operating in Mono, the peak detector takes the maximum of channel peak values, and any new gain setting is applied to both PGAs, so that the Mono image is preserved. However, the ALC function can also be enabled on one channel only. In this case, only one PGA is controlled by the ALC mechanism, while the other channel runs independently with its PGA gain set through the control register.

When one ADC channel is unused or used for DC measurement, the peak detector disregards that channel. The ALC function can also operate when the two ADC outputs are mixed to mono in the digital domain, but not if they are mixed to mono in the analogue domain, before entering the ADCs.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R17 (11h) ALC Control 1	8	ALCSE	0 (OFF)	ALC function select 0 = ALC off (PGA gain set by register) 1 = channel only Note: ensure that INVOL settings (reg. 0) is the same before entering this mode.
	6:4	MAXGAIN [2:0]	111 (+30dB)	Set Maximum Gain of PGA 111 : +30dB 110 : +24dB ….(-6dB steps) 001 : -6dB 000 : -12dB
	3:0	ALC [3:0]	1011 (-12dB)	ALC target – sets signal level at ADC Input 0000 = -28.5dB FS 0001 = -27.0dB FS … (1.5dB steps) 1110 = -7.5dB FS 1111 = -6dB FS
R18 (12h) ALC Control 2	7	ALCZC	0 (zero cross off)	ALC uses zero cross detection circuit.
	3:0	HLD [3:0]	0000 (0ms)	ALC hold time before gain is increased. 0000 = 0ms 0001 = 2.67ms 0010 = 5.33ms … (time doubles with every step) 1111 = 43.7s
R19 (13h) ALC Control 3	7:4	DCY [3:0]	0011 (192ms)	ALC decay (gain ramp-up) time 0000 = 24ms 0001 = 48ms 0010 = 96ms … (time doubles with every step) 1010 or higher = 24.58s
	3:0	ATK [3:0]	0010 (24ms)	ALC attack (gain ramp-down) time 0000 = 6ms 0001 = 12ms 0010 = 24ms … (time doubles with every step) 1010 or higher = 6.14s

Table 6 ALC Control

PEAK LIMITER

To prevent clipping when a large signal occurs just after a period of quiet, the ALC circuit includes a limiter function. If the ADC input signal exceeds 87.5% of full scale (–1.16dB), the PGA gain is ramped down at the maximum attack rate (as when ATK = 0000), until the signal level falls below 87.5% of full scale. This function is automatically enabled whenever the ALC is enabled.

Note:

If ATK = 0000, then the limiter makes no difference to the operation of the ALC. It is designed to prevent clipping when long attack times are used.

NOISE GATE

When the signal is very quiet and consists mainly of noise, the ALC function may cause “noise pumping”, i.e. loud hissing noise during silence periods. The CJC8911 has a noise gate function that prevents noise pumping by comparing the signal level at the MICINP and MICINN pins against a noise gate threshold, NGTH. The noise gate cuts in when:

- Signal level at ADC [dB] < NGTH [dB] + PGA gain [dB] + Mic Boost gain [dB]

This is equivalent to:

- Signal level at input pin [dB] < NGTH [dB]

The ADC output can then either be muted or alternatively, the PGA gain can be held constant (preventing it from ramping up as it normally would when the signal is quiet).

The table below summarises the noise gate control register. The NGTH control bits set the noise gate threshold with respect to the ADC full-scale range. The threshold is adjusted in 1.5dB steps. Levels at the extremes of the range may cause inappropriate operation, so care should be taken with set–up of the function. Note that the noise gate only works in conjunction with the ALC function, and always operates on the same channel(s) as the ALC (both, or none).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R20 (14h) Noise Gate Control	7:3	NGTH [4:0]	00000	Noise gate threshold 13 -76.5dBfs 13 -75dBfs … 1.5 dB steps 11110 -31.5dBfs 11111 -30dBfs
	2:1	NGG [1:0]	00	Noise gate type X0 = PGA gain held constant 01 = mute ADC output 11 = reserved (do not use this setting)
	0	NGAT	0	Noise gate function enable 1 = enable 0 = disable

Table 7 Noise Gate Control

Note:

The performance of the ADC may degrade at high input signal levels if the monitor bypass mux is selected with MIC boost and ALC enabled.

3D Mono ENHANCEMENT

The CJC8911 has a digital 3D enhancement option to artificially increase the separation between the channels. This effect can be used for recording or playback, but not for both simultaneously. Selection of 3D for record or playback is controlled by register bit MODE3D.

Important:

Switching the 3D filter from record to playback or from playback to record may only be done when ADC and DAC are disabled. The CJC8911 control interface will only allow MODE3D to be changed when ADC and DAC are disabled.

The 3D enhancement function is activated by the 3DEN bit, and has two programmable parameters. The 3DDEPTH setting controls the degree of mono expansion. Additionally, one of four filter characteristics can be selected for the 3D processing, using the 3DVC and 3DLC control bits.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16 (10h) 3D enhance	6	3DUC	0	Upper Cut-off frequency 0 = High (2.2kHz at 48kHz sampling) 1 = Low (1.5kHz at 48kHz sampling)
	5	3DLC	0	Lower Cut-off frequency 0 = Low (200Hz at 48kHz sampling) 1 = High (500Hz at 48kHz sampling)
	4:1	3DDEPTH [3:0]	0000	Mono depth 0000: 0% (minimum 3D effect) 0001: 6.67% .... 1110: 93.3% 1111: 100% (maximum 3D effect)
	0	3DEN	0	3D function enable 1: enabled 0: disabled

Table 8 3D Mono Enhancement Function

When 3D enhancement is enabled (and/or the graphic equaliser for playback) it may be necessary to attenuate the signal by 6dB to avoid limiting. This is a user selectable function, enabled by setting ADCDIV2 for the record path and DACDIV2 for the playback path.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) ADC and DAC control	8	ADCDIV2	0	ADC 6dB attenuate enable 0 = disabled (0dB) 1 = -6dB enabled
	7	DACDIV2	0	DAC 6dB attenuate enable 0 = disabled (0dB) 1 = -6dB enabled

Table 9 ADC and DAC 6dB Attenuation Select

OUTPUT SIGNAL PATH

The CJC8911 output signal paths consist of digital filters, DACs, analogue mixers and output drivers. The digital filters and DACs are enabled when the CJC8911 is in 'playback only' or 'record and playback' mode. The mixers and output drivers can be separately enabled by individual control bits (see Analogue Outputs). Thus it is possible to utilise the analogue mixing and amplification provided by the CJC8911, irrespective of whether the DACs are running or not.
The CJC8911 receives digital input data on the DACDAT pin. The digital filter block processes the data to provide the following functions:

- Digital volume control
- Graphic equaliser and Dynamic Bass Boost
- Sigma-Delta Modulation

Two high performance sigma-delta audio DACs convert the digital data into one analogue signals . These can then be mixed with analogue signals from the MICINP and MICINN pins, and the mix is fed to the output drivers, AOUT.

DIGITAL DAC VOLUME CONTROL

The signal volume from each DAC can be controlled digitally, in the same way as the ADC volume (see Digital ADC Volume Control). The gain and attenuation range is –127dB to 0dB in 0.5dB steps. The level of attenuation for an eight-bit code X is given by:

0.5 × (X-255) dB for 1 ≤ X ≤ 255; MUTE for X = 0

The DVU control bits control the loading of digital volume control data. When DVU are set to 0, the DACVOL control data is loaded into an intermediate register, but the actual gain does not change. Both gain settings are updated simultaneously when either DVU are set to 1.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R10 (0Ah) Digital Volume	8	DVU	0	DAC Volume Update 0 = Store DACVOL in intermediate latch (no gain change) 1 = Update gains
	7:0	DACVOL [7:0]	11111111 (0dB)	DAC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -127dB 0000 0010 = -126.5dB ... 0.5dB steps up to 1111 1111 = 0dB

Table 10 Digital Volume Control

GRAPHIC EQUALISER

The CJC8911 has a digital graphic equaliser and adaptive bass boost function. This function operates on digital audio data before it is passed to the audio DACs. Bass enhancement can take two different forms:

- Linear bass control: bass signals are amplified or attenuated by a user programmable gain. This is independent of signal volume, and very high bass gains on loud signals may lead to signal clipping.

- Adaptive bass boost: The bass volume is amplified by a variable gain. When the bass volume is low, it is boosted more than when the bass volume is high. This method is recommended because it prevents clipping, and usually sounds more pleasant to the human ear.
  Treble control applies a user programmable gain, without any adaptive boost function. Bass and treble control are completely independent with separately programmable gains and filter characteristics.

<table>
<tr><th>REGISTER ADDRESS</th><th>BIT</th><th>LABEL</th><th>DEFAULT</th><th colspan="3">DESCRIPTION</th></tr>
<tr><td rowspan="20">R12 (0Ch)
Bass Control</td><td>7</td><td>BB</td><td>0</td><td colspan="3">Bass Boost
0 = Linear bass control
1 = Adaptive bass boost</td></tr>
<tr><td>6</td><td>BC</td><td>0</td><td colspan="3">Bass Filter Characteristic
0 = Low Cutoff (130Hz at 48kHz sampling)
1 = High Cutoff (200Hz at 48kHz sampling)</td></tr>
<tr><td rowspan="18">3:0</td><td rowspan="18">BASS
[3:0]</td><td rowspan="18">1111
(Disabled)</td><td colspan="3">Bass Intensity</td></tr>
<tr><td>Code</td><td>BB=0</td><td>BB=1</td></tr>
<tr><td>0000</td><td>+9dB</td><td>15</td></tr>
<tr><td>0001</td><td>+9dB</td><td>14</td></tr>
<tr><td>0010</td><td>+7.5dB</td><td>13</td></tr>
<tr><td>0011</td><td>+6dB</td><td>12</td></tr>
<tr><td>0100</td><td>+4.5dB</td><td>11</td></tr>
<tr><td>0101</td><td>+3dB</td><td>10</td></tr>
<tr><td>0110</td><td>+1.5dB</td><td>9</td></tr>
<tr><td>0111</td><td>0dB</td><td>8</td></tr>
<tr><td>1000</td><td>-1.5dB</td><td>7</td></tr>
<tr><td>1001</td><td>-3dB</td><td>6</td></tr>
<tr><td>1010</td><td>-4.5dB</td><td>5</td></tr>
<tr><td>1011</td><td>-6dB</td><td>4</td></tr>
<tr><td>1100</td><td>-6dB</td><td>3</td></tr>
<tr><td>1101</td><td>-6dB</td><td>2</td></tr>
<tr><td>1110</td><td>-6dB</td><td>1</td></tr>
<tr><td>1111</td><td colspan="2">Bypass (OFF)</td></tr>
<tr><td rowspan="2">R13 (0Dh)
Treble Control</td><td>6</td><td>TC</td><td>0</td><td colspan="3">Treble Filter Characteristic
0 = High Cutoff (8kHz at 48kHz sampling)
1 = Low Cutoff (4kHz at 48kHz sampling)</td></tr>
<tr><td>3:0</td><td>TRBL
[3:0]</td><td>1111
(Disabled)</td><td colspan="3">Treble Intensity
0000 or 0001 = +9dB
0010 = +7.5dB
… (1.5dB steps)
1011 to 1110 = -6dB
1111 = Disable</td></tr>
</table>

Table 11 Graphic Equaliser

DIGITAL TO ANALOGUE CONVERTER (DAC)

After passing through the graphic equaliser filters, digital 'de-emphasis' can be applied to the audio data if necessary (e.g. when the data comes from a CD with pre-emphasis used in the recording). De-emphasis filtering is available for sample rates of 48kHz, 44.1kHz and 32kHz.

The CJC8911 also has a Soft Mute function, which gradually attenuates the volume of the digital signal to zero. When removed, the gain will return to the original setting. This function is enabled by default. To play back an audio signal, it must first be disabled by setting the DACMU bit to zero.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) ADC and DAC control	2:1	DEEMP [1:0]	00	De-emphasis Control 11 = 48kHz sample rate 10 = 44.1kHz sample rate 01 = 32kHz sample rate 00 = No De-emphasis
	3	DACMU	1	Digital Soft Mute 1 = mute 0 = no mute (signal active)

Table 12 DAC Control

The digital audio data is converted to oversampled bit streams in the on-chip, true 24-bit digital interpolation filters.

The bitstream data enters two multi-bit, sigma-delta DACs, which convert them to high quality analogue audio signals.

The multi-bit DAC architecture reduces high frequency noise and sensitivity to clock jitter. It also uses a Dynamic Element Matching technique for high linearity and low distortion. In normal operation, the channel digital audio data is converted to analogue in two separate DACs.

However, it is also possible to disable one channel, so that the same signal appears on both analogue output channels.

Additionally, there is a mono-mix mode where the two audio channels are mixed together digitally and then converted to analogue using only one DAC, while the other DAC is switched off.

The mono-mix signal can be selected to appear on both analogue output channels.

The DAC output defaults to non-inverted. Setting DACINV will invert the DAC output phase on both channels.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R23 (17h) Additional Control (1)	5:4	DMONOMIX [1:0]	00	DAC mono mix 00: Disable 01: mono ((L+R)/2) into DACL, '0' into DACR 10: mono ((L+R)/2) into DACR, '0' into DACL 11: mono ((L+R)/2) into DACL and DACR
	1	DACINV	0	DAC phase invert 0 : non-inverted 1 : inverted

Table 13 DAC Mono Mix and Phase Invert Select

OUTPUT MIXERS

The CJC8911 provides the option to mix the DAC output signal with analogue MIC-in signals from the MIC pins through the PGAs. The level of the mixed-in signals can be controlled with PGAs (Programmable Gain Amplifiers).

The mono mixer is designed to allow a number of signal combinations to be mixed, including the possibility of mixing both the channels together to produce a mono output. To prevent overloading of the mixer when full-scale DAC signals are input, the mixer inputs from the DAC outputs each have a fixed gain of -6dB. The path inputs to the mono mixer have variable gain as determined by R36 bits [2:0].

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R33 (21h) MIC	4	MIC2O	0	Micphone signal after INSEL to Mixer 0 = Disable (Mute) 1 = Enable Path
	3:0	MIC2OVOL	1010 (-9dB)	MIC Signal from INSEL to Mixer Volume 000 0= +6dB … (1.5dB steps) 111 1= -16.5dB
R34 (22h) AUX	4	AUX2O	0	Micphone signal after PGA to Mixer 0 = Disable (Mute) 1 = Enable Path
	3:0	AUX2OVOL	1010 (-9dB)	MIC Signal after PGA to Mixer Volume 000 = +6dB … (1.5dB steps) 111 = -16.5dB

Table 14 Output Mixer Signal Selection

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R35 (23h) Mixer Control (1)	8	D2O	0	DAC to Mixer (DIGITAL) 0 = Disable (Mute) 1 = Enable Path

Table 15 Output Mixer Control

ANALOGUE OUTPUTS

AOUT OUTPUTS

The AOUT pins can drive a line output (see Line Output sections, respectively). The signal volume on AOUT can be independently adjusted under software control by writing to OUTVOL, respectively. Note that gains over 0dB may cause clipping if the signal is large. Any gain setting below 0101111 (minimum) mutes the output driver. The corresponding output pin remains at the same DC level (the reference voltage on the VREF pin), so that no click noise is produced when muting or un-muting.

A zero cross detect on the analogue output may also be enabled when changing the gain setting to minimize audible clicks and zipper noise as the gain updates. If zero cross is enabled a timeout is also available to update the gain if a zero cross does not occur. This function may be enabled by setting TOEN in register R23 (17h).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h) AOUT Volume	8	OVU	0	Volume Update 0 = Store OUTVOL in intermediate latch (no gain change) 1 = Update channel gains
	7	OZC	0	zero cross enable 1 = Change gain on zero cross only 0 = Change gain immediately
	6:0	OUTVOL [6:0]	1111001 (0dB)	AOUT Volume 1111111 = +6dB … (80 steps) 0110000 = -67dB 0111111 to 0000000 = Analogue MUTE

Table 16 AOUT Volume Control

AOUT COMMON GROUND Enable (COM)

The AOUT outputs also have the option of incorporating common ground via a connection to the COM which can act as a ground for then we need not the big capacitor between AOUT pin. The COM is driven by an opamp in chip and should be AC-coupled via a 4.7uF capacitor for the aout loads. If we used as LINE outputs requires we should connect the AOUT and real GND to instrument , not COM. Because COM voltage is equal to VREF pin.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24 (18h) COM Control	7	COMEN	1	Enables COM on then AOUT 0: Disable COM drive 1: Enable COM drive

Table 17 COM Control

ENABLING THE OUTPUTS

Each analogue output of the CJC8911 can be separately enabled or disabled. The analogue mixer associated with each output is powered on or off along with the output pin. All outputs are disabled by default. To save power, unused outputs should remain disabled.

Outputs can be enabled at any time, except when VREF is disabled (VR=0), as this may cause pop noise (see “Power Management” and “Applications Information” sections)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R26 (1Ah) Power Management(2)	6	AOUT	0	AOUT Enable
Note: All “Enable” bits are 1 = Enabled, 0 = Disabled				

Table 18 Analogue Output Control

Whenever an analogue output is disabled, it remains connected to VREF (pin 20) through a resistor. This helps to prevent pop noise when the output is re-enabled. The resistance between VREF and each output can be controlled using the VROI bit in register 27. The default is low (1.5kΩ), so that any capacitors on the outputs can charge up quickly at start-up. If a high impedance is desired for disabled outputs, VROI can then be set to 1, increasing the resistance to about 40Kω

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R27 (1Bh) Additional (1)	6	VROI	0	VREF to analogue output resistance 0: 1.5 kΩ 1: 40 kΩ

Table 19 Disabled Outputs to VREF Resistance

THERMAL SHUTDOWN

The AOUT outputs can drive very large currents. To protect the CJC8911 from overheating a thermal shutdown circuit is included. If the device temperature reaches approximately 150 C and the thermal shutdown circuit is enabled (TSDEN = 1) then the outputs AOUT will be disabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R23 (17h) Additional Control (1)	8	TSDEN	0	Thermal Shutdown Enable 0 : thermal shutdown disabled 1 : thermal shutdown enabled

Table 20 Thermal Shutdown

DIGITAL AUDIO INTERFACE

The digital audio interface is used for inputting DAC data into the CJC8911 and outputting ADC data from it. It uses four pins:

- ADCDAT: ADC data output
- DACDAT: DAC data input
- LRC: DAC and ADC data alignment clock
- BCLK: Bit clock, for synchronisation

The clock signals BCLK and LRC can be an output when the CJC8911 operates as a master, or an input when it is a slave (see Master and Slave Mode Operation, below).
Four different audio data formats are supported:

- Left justified
- I2S
- DSP mode

All four of these modes are MSB first. They are described in Audio Data Formats, below. Refer to the Electrical Characteristic section for timing information.

MASTER AND SLAVE MODE OPERATION

The CJC8911 can be configured as either a master or slave mode device. As a master device the CJC8911 generates BCLK, ADCLRC and DACLRC and thus controls sequencing of the data transfer on ADCDAT and DACDAT. In slave mode, the CJC8911 responds with data to clocks it receives over the digital audio interface. The mode can be selected by writing to the MS bit (see Table 21). Master and slave modes are illustrated below.

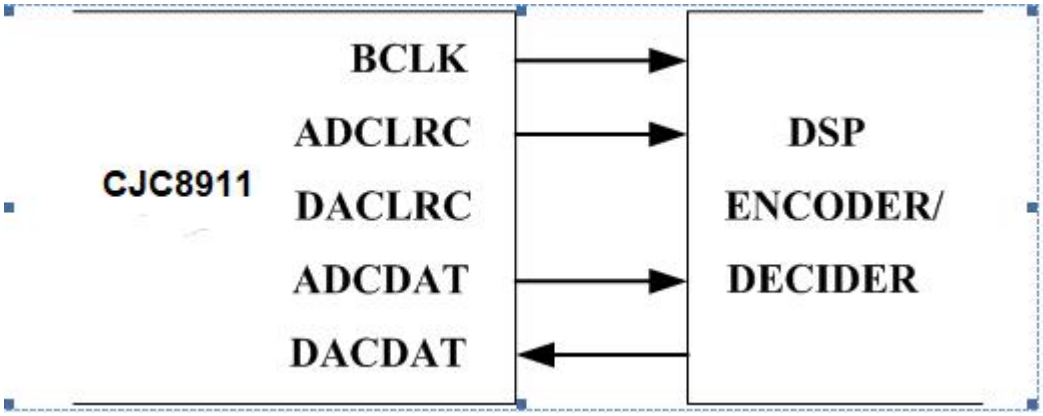


Figure 9 Master Mode

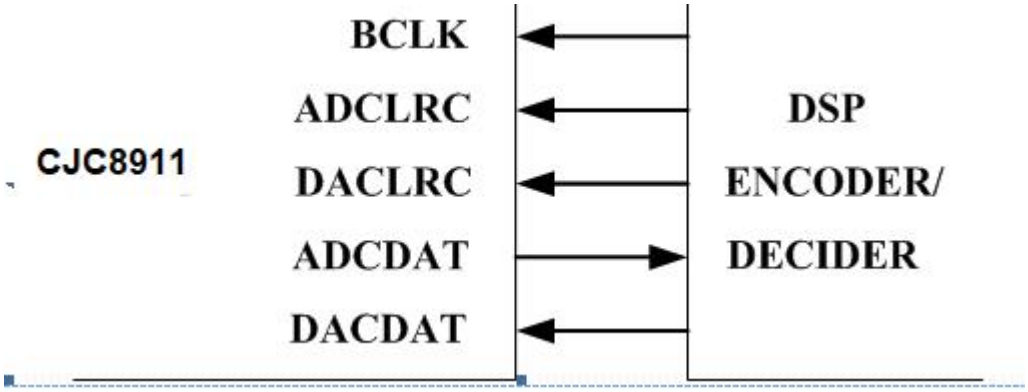


Figure 10 Slave Mode

AUDIO DATA FORMATS

In Left Justified mode, the MSB is available on the first rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRCLK transition.

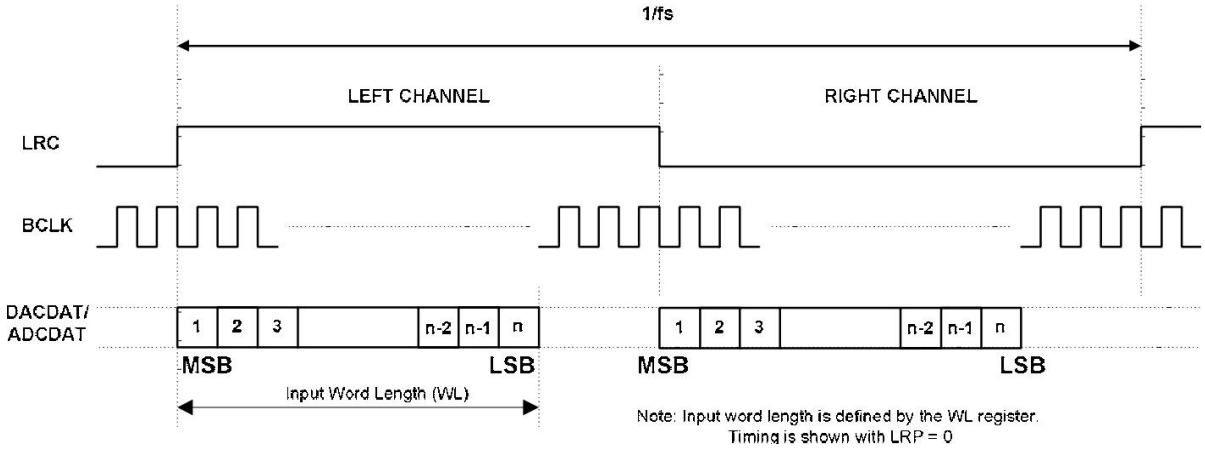


Figure 11 Left Justified Audio Interface (assuming n-bit word length)

In I2S mode, the MSB is available on the second rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

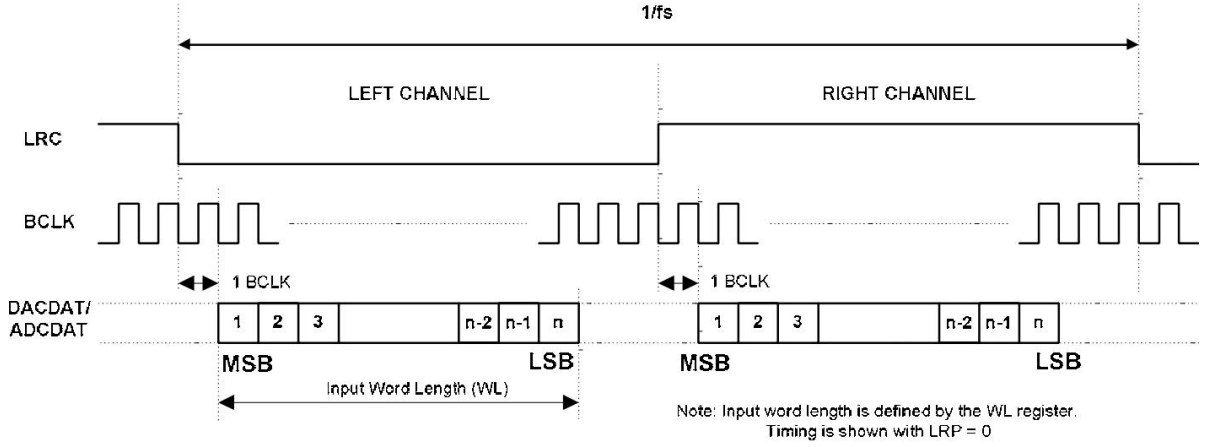


Figure 12 I2S Justified Audio Interface (assuming n-bit word length)

In DSP/PCM mode, the left channel MSB is available on either the 1 (mode B) or 2 (mode A) rising edge of BCLK (selectable by LRP) following a rising edge of LRC. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample. In device master mode, the LRC output will resemble the frame pulse shown in Figure 13 and Figure 14. In device slave mode, Figure 15 and Figure 16, it is possible to use any length of frame pulse

less than 1/fs, providing the falling edge of the frame pulse occurs greater than one BCLK period before the rising edge of the next frame pulse.

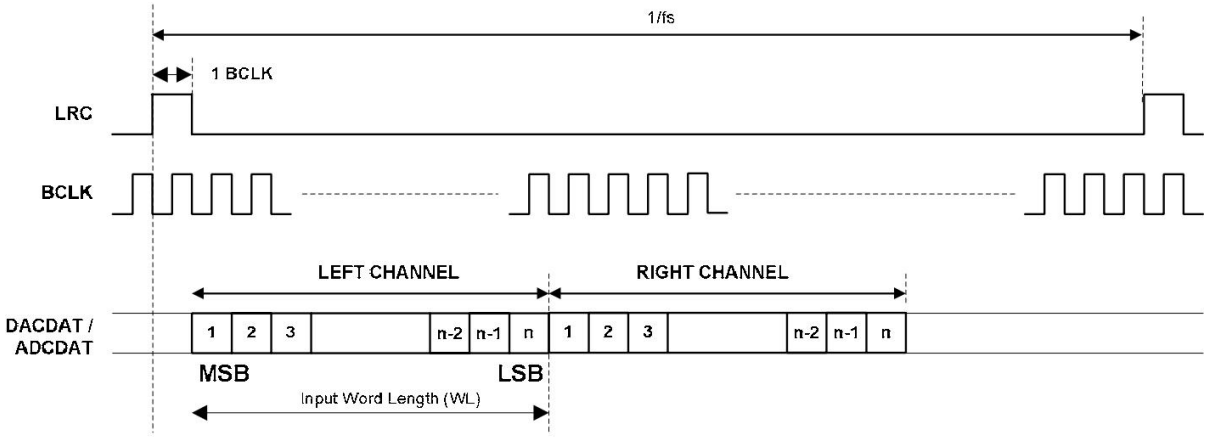


Figure 13 DSP/PCM Mode Audio Interface (mode A, LRP=0, Master)

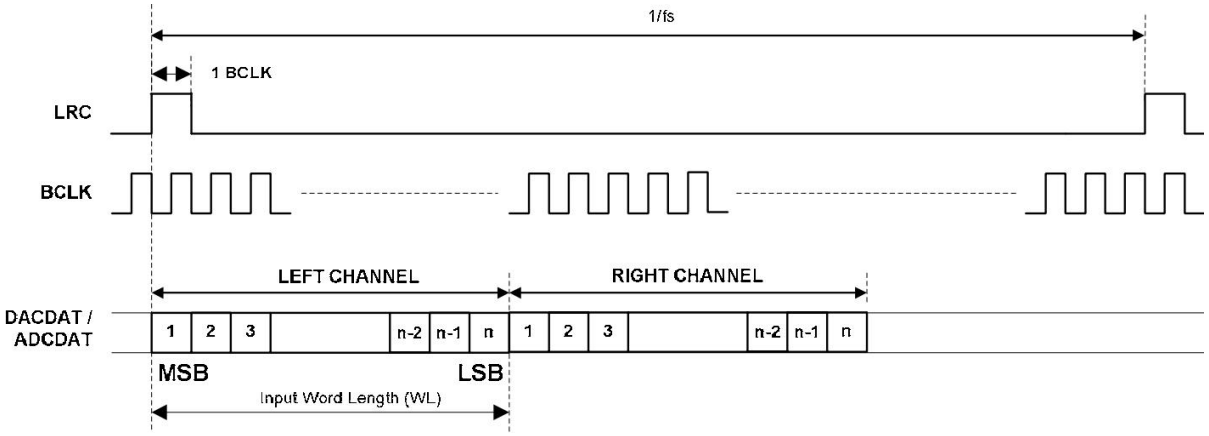


Figure 14 DSP/PCM Mode Audio Interface (mode B, LRP=1, Master)

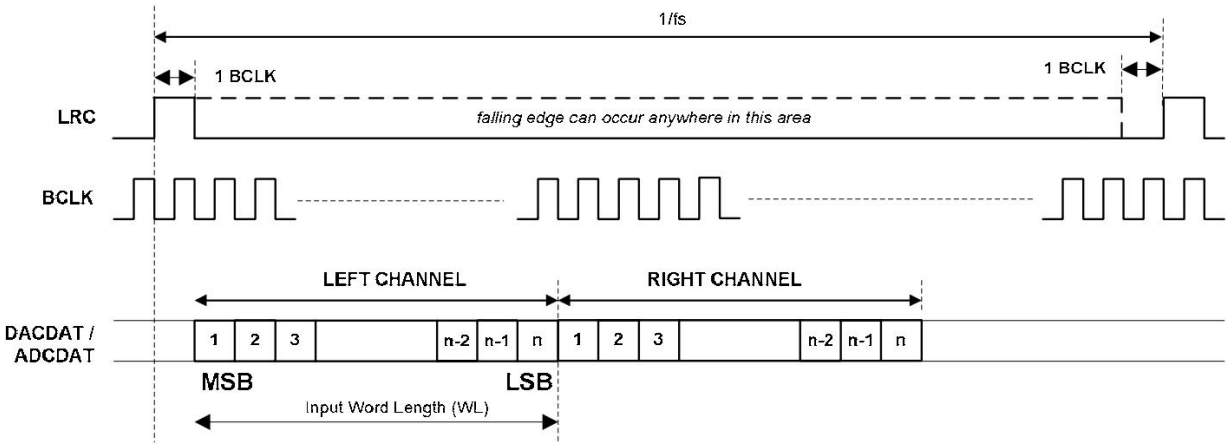


Figure 15 DSP/PCM Mode Audio Interface (mode A, LRP=0, Slave)

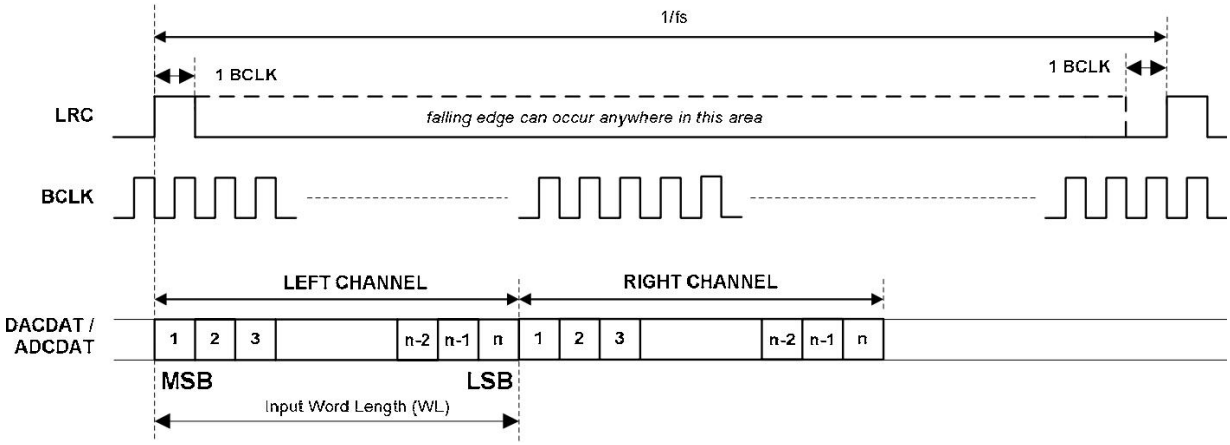


Figure 16 DSP/PCM Mode Audio Interface (mode B, LRP=0, Slave)

AUDIO INTERFACE CONTROL

The register bits controlling audio format, word length and master / slave mode are summarised in Table 21. MS selects audio interface operation in master or slave mode. In Master mode BCLK and LRC are outputs. The frequency of LRC is set by the sample rate control bits SR[4:0] and USB. In Slave mode BCLK and LRC are inputs.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 (07h) Digital Audio Interface Format	7	BCLKINV	0	BCLK invert bit (for master and slave modes) 0 = BCLK not inverted 1 = BCLK inverted
	6	MS	0	Master / Slave Mode Control 1 = Enable Master Mode 0 = Enable Slave Mode
	4	LRP	0	right, left and I^2S modes – LRCLK polarity 1 = invert LRCLK polarity 0 = normal LRCLK polarity NOTE: this register is valid for ADC, DAC don't output when LRP equals to 1.
				DSP Mode – mode A/B select 1 = MSB is available on 1 BCLK rising edge after LRC rising edge (mode B) 0 = MSB is available on 2 BCLK rising edge after LRC rising edge (mode A)
	3:2	WL[1:0]	10	Audio Data Word Length 11 = 32 bits (see Note) 10 = 24 bits 01 = 20 bits 00 = 16 bits
	1:0	FORMAT[1:0]	10	Audio Data Format Select 11 = DSP Mode 10 = I^2S Format 01 = Left justified 00 = reserved (do not use this setting)

Table 21 Audio Data Format Control

AUDIO INTERFACE OUTPUT TRISTATE

Register bit TRI, register 24(18h) bit[3] can be used to tristate the ADCDAT pin and switch ADCLRC, DACLRC and BCLK to inputs. In Slave mode (MASTER=0) LRC and BCLK are by default configured as inputs and only ADCDAT will be tri-stated, (see Table 22).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24(18h) Additional Control (2)	3	TRI	0	Tristates ADCDAT and switches ADCLRC, DACLRC and BCLK to inputs. 0 = ADCDAT is an output, LRC and BCLK are inputs (slave mode) or outputs (master mode) 1 = ADCDAT is tristated, LRC and BCLK are inputs

Table 22 Tri-stating the Audio Interface

MASTER MODE LRC ENABLE

In Master mode the lrclk (LRC) is enabled by default only when the DAC is enabled. If ADC only operation in Master mode is required register bit LRCM must be set in oder to generate an lrclk. For DAC only operation LRCM may be set to '0'.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24(18h) Additional Control (2)	2	LRCM	0	Selects disable mode for LRC 0 = LRC disabled when DAC disabled. 1 = LRC disabled only when ADC and DAC are disabled.

Table 23 LRC Enable

BIT CLOCK MODE

The default master mode bit clock generator produces a bit clock frequency based on the sample rate and input MCLK frequency as shown in Table 24.When enabled by setting the appropriate BCM[1:0] bits, the bit clock mode (BCM) function overrides the default master mode bit clock generator to produce the bit clock frequency shown in the table below:

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 (08h) Clocking and Sample Rate Control	8:7	BCM[1:0]	00	BCLK Frequency 00 = BCM function disabled 01 = MCLK/4 10 = MCLK/8 11 = MCLK/16

Table 24 Master Mode BCLK Frequency Control

The BCM mode bit clock generator produces 16 or 24 bit clock cycles per sample. The number of bit clock cycles per sample in this mode is determined by the word length bits (WL[1:0]) in the Digital Audio Interface Format register (R7). When these bits are set to 00, there will be 16 bit clock cycles per sample. When these bits are set to 01, 10 or 11, there will be 24 bit clock cycles per sample. Please refer to Figure 17.

In order to use BCM either the ADC must be enabled or, if the ADC is disabled, the LRCM bit must be set and the DAC enabled.

When the BCM function is enabled, the following restrictions apply:

1. The bit clock invert (BCLKINV) function is not available.
2. DSP late digital audio interface mode is not available and must not be enabled.

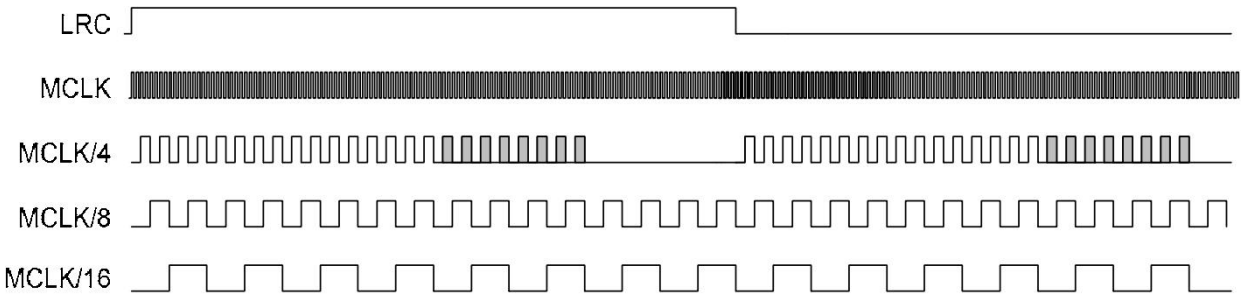


Figure 17 Bit Clock Mode

Note:

The shaded bit clock cycles are present only when 24-bit mode is selected. Please refer to the “Bit Clock Mode” description for details.

CLOCKING AND SAMPLE RATES

The CJC8911 supports a wide range of master clock frequencies on the MCLK pin, and can generate many commonly used audio sample rates directly from the master clock. The ADC and DAC must always run at the same sample rate.

There are two clocking modes:

- 'Normal' mode supports master clocks of 128fs, 192fs, 256fs, 384fs, and their multiples (Note: fs refers to the ADC or DAC sample rate, whichever is faster)
- USB mode supports 12MHz or 24MHz master clocks. This mode is intended for use in systems with a USB interface, and eliminates the need for an external PLL to generate another clock frequency for the audio codec.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 (08h) Clocking and Sample Rate Control	6	CLKDIV2	0	Master Clock Divide by 2 1 = MCLK is divided by 2 0 = MCLK is not divided
	5:1	SR [4:0]	00000	Sample Rate Control
	0	USB	0	Clocking Mode Select 1 = USB Mode 0 = 'Normal' Mode

Table 25 Clocking and Sample Rate Control

The clocking of the CJC8911 is controlled using the CLKDIV2, USB, and SR control bits. Setting the CLKDIV2 bit divides MCLK by two internally. The USB bit selects between 'Normal' and USB mode. Each value of SR[4:0] selects one combination of MCLK division ratios and hence one combination of sample rates (see next page). Since all sample rates are generated by dividing MCLK, their accuracy depends on the accuracy of MCLK. If MCLK changes, the sample rates change proportionately.

Note that some sample rates (e.g. 44.1kHz in USB mode) are approximated, i.e. they differ from their target value by a very small amount. This is not audible, as the maximum deviation is only 0.27% (8.0214kHz instead of 8kHz in USB mode). By comparison, a half-tone step corresponds to a 5.9% change in pitch.

The SR[4:0] bits must be set to configure the appropriate ADC and DAC sample rates in both master and slave mode.

MCLK CLKDIV2=0	MCLK CLKDIV2=1	ADC SAMPLE RATE (ADCLRC)	DAC SAMPLE RATE (DACLRC)	USB	SR [4:0]	FILTER TYPE	BCLK (MS=1)
'Normal' Clock Mode ('*' indicates backward compatibility with CJC8731)							
12.288 MHz	24.576 MHz	8 kHz (MCLK/1536)	8 kHz (MCLK/1536)	0	00110*	1	MCLK/4
		12 kHz (MCLK/1024)	12 kHz (MCLK/1024)	0	01000	1	MCLK/4
		16 kHz (MCLK/768)	16 kHz (MCLK/768)	0	01010	1	MCLK/4
		24 kHz (MCLK/512)	24 kHz (MCLK/512)	0	11100	1	MCLK/4
		32 kHz (MCLK/384)	32 kHz (MCLK/384)	0	01100*	1	MCLK/4
		48 kHz (MCLK/256)	48 kHz (MCLK/256)	0	00000*	1	MCLK/4
		96 kHz (MCLK/128)	96 kHz (MCLK/128)	0	01110*	3	MCLK/2
11.2896MHz	22.5792MHz	8.0182 kHz (MCLK/1408)	8.0182 kHz (MCLK/1408)	0	10110*	1	MCLK/4
		11.025 kHz (MCLK/1024)	11.025 kHz (MCLK/1024)	0	11000	1	MCLK/4
		22.05 kHz (MCLK/512)	22.05 kHz (MCLK/512)	0	11010	1	MCLK/4
		44.1 kHz (MCLK/256)	44.1 kHz (MCLK/256)	0	10000*	1	MCLK/4
		88.2 kHz (MCLK/128)	88.2 kHz (MCLK/128)	0	11110*	3	MCLK/2
18.432MHz	36.864MHz	8 kHz (MCLK/2304)	8 kHz (MCLK/2304)	0	00111*	1	MCLK/6
		12 kHz (MCLK/1536)	12 kHz (MCLK/1536)	0	01001	1	MCLK/6
		16kHz (MCLK/1152)	16 kHz (MCLK/1152)	0	01011	1	MCLK/6
		24kHz (MCLK/768)	24 kHz (MCLK/768)	0	11101	1	MCLK/6
		32 kHz (MCLK/576)	32 kHz (MCLK/576)	0	01101*	1	MCLK/6
		48 kHz (MCLK/384)	48 kHz (MCLK/384)	0	00001*	1	MCLK/6
		96 kHz (MCLK/192)	96 kHz (MCLK/192)	0	01111*	3	MCLK/3
16.9344MHz	33.8688MHz	8.0182 kHz (MCLK/2112)	8.0182 kHz (MCLK/2112)	0	10111*	1	MCLK/6
		11.025 kHz (MCLK/1536)	11.025 kHz (MCLK/1536)	0	11001	1	MCLK/6
		22.05 kHz (MCLK/768)	22.05 kHz (MCLK/768)	0	11011	1	MCLK/6
		44.1 kHz (MCLK/384)	44.1 kHz (MCLK/384)	0	10001*	1	MCLK/6
		88.2 kHz (MCLK/192)	88.2 kHz (MCLK/192)	0	11111*	3	MCLK/3

Table 26 Master Clock and Sample Rate

MCLK CLKDIV2=0	MCLK CLKDIV2=1	ADC SAMPLE RATE (ADCLRC)	DAC SAMPLE RATE (DACLRC)	USB	SR [4:0]	FILTER TYPE	BCLK (MS=1)
USB Mode ('*' indicates backward compatibility with CJC8731)							
12.000MHz	24.000MHz	8 kHz (MCLK/1500)	8 kHz (MCLK/1500)	1	00110*	0	MCLK
		8.0214 kHz (MCLK/1496)	8.0214kHz (MCLK/1496)	1	10111*	1	MCLK
		11.0259 kHz (MCLK/1088)	11.0259kHz (MCLK/1088)	1	11001	1	MCLK
		12 kHz (MCLK/1000)	12 kHz (MCLK/1000)	1	01000	0	MCLK
		16kHz (MCLK/750)	16kHz (MCLK/750)	1	01010	0	MCLK
		22.0588kHz (MCLK/544)	22.0588kHz (MCLK/544)	1	11011	1	MCLK
		24kHz (MCLK/500)	24kHz (MCLK/500)	1	11100	0	MCLK
		32 kHz (MCLK/375)	32 kHz (MCLK/375)	1	01100*	0	MCLK
		44.118 kHz (MCLK/272)	44.118 kHz (MCLK/272)	1	10001*	1	MCLK
		48 kHz (MCLK/250)	48 kHz (MCLK/250)	1	00000*	0	MCLK
		88.235kHz (MCLK/136)	88.235kHz (MCLK/136)	1	11111*	3	MCLK
		96 kHz (MCLK/125)	96 kHz (MCLK/125)	1	01110*	2	MCLK

Table 27 Master Clock and Sample Rates

CONTROL INTERFACE

CONTROL MODE

The CJC8911 is controlled by writing to registers through a serial control interface. A control word consists of 16 bits. The control interface operate as 2-wire MPU interface.

2-WIRE SERIAL CONTROL MODE

The CJC8911 supports software control via a 2-wire serial bus. Many devices can be controlled by the same bus, and each device has a unique 7-bit address (this is not the same as the 7-bit address of each register in the CJC8911).

The CJC8911 operates as a slave device only. The controller indicates the start of data transfer with a high to low transition on SDIN while SCLK remains high. This indicates that a device address and data will follow. All devices on the 2-wire bus respond to the start condition and shift in the next eight bits on SDIN (7-bit address + Read/Write bit, MSB first). If the device address received matches the address of the CJC8911 and the R/W bit is '0', indicating a write, then the CJC8911 responds by pulling SDIN low on the next clock pulse (ACK). If the address is not recognised or the R/W bit is '1', the CJC8911 returns to the idle condition and wait for a new start condition and valid address.

Once the CJC8911 has acknowledged a correct address, the controller sends the first byte of control data (B15 to B8, i.e. the CJC8911 register address plus the first bit of register data). The CJC8911 then acknowledges the first data byte by pulling SDIN low for one clock pulse. The controller then sends the second byte of control data (B7 to B0, i.e. the remaining 8 bits of register data), and the CJC8911 acknowledges again by pulling SDIN low.
The transfer of data is complete when there is a low to high transition on SDIN while SCLK is high. After receiving a complete address and data sequence the CJC8911 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. SDIN changes while SCLK is high), the device jumps to the idle condition.

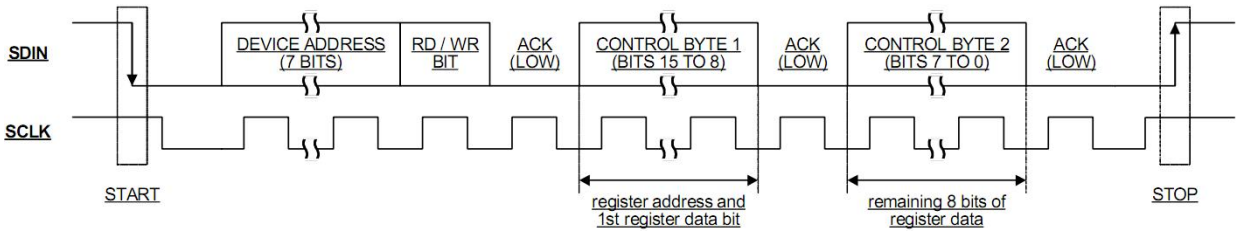


Figure 19 2-Wire Serial Control Interface

The CJC8911 has one device addresses, the CSB pin is high.

CSB STATE	DEVICE ADDRESS
High	0011011 (0 x 36h)

Table 28 2-Wire MPU Interface Address Selection

POWER SUPPLIES

The CJC8911 can use up to four separate power supplies:

- AVDD / AGND: Analogue supply, powers all analogue functions except the AOUT drivers. AVDD can range from 1.8V to 3 V and has the most significant impact on overall power consumption. A large AVDD slightly improves audio quality.

- HPVDD / HPGND: AOUT supply, powers the AOUT drivers. HPVDD is normally tied to AVDD, but it requires separate layout and decoupling capacitors to curb harmonic distortion. If HPVDD is lower than AVDD, the output signal may be clipped.

- DCVDD: Digital core supply, powers all digital functions except the audio and control interfaces. DCVDD can range from 1.5V to 3.3V, and has no effect on audio quality. The return path for DCVDD is DGND, which is shared with DBVDD.

DBVDD: Digital buffer supply, powers the audio and control interface buffers. For saving the PIN number, DBVDD is connect to DCVDD . DBVDD draws much less power than DCVDD, and has no effect on audio quality. For the reason of less PIN, we connect DBVDD and DCVDD, and DBVDD did not effect the digital core and chip performance.

It is possible to use the same supply voltage on all three However, digital and analogue supplies should be outed and decoupled separately to keep digital switching noise out of the analogue signal paths.

POWER MANAGEMENT

The CJC8911 has two control registers that allow users to select which functions are active. For minimum power consumption, unused functions should be disabled. To avoid any pop or click noise, it is important to enable or disable functions in the correct order (see Applications Information). VMIDSEL is the enable for the Vmid reference, which defaults to disabled and can be enabled as a 50kΩ potential divider or, for low power maintenance of Vref when all other blocks are disabled, as a 500kΩ potential divider.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R25 (19h) Power Management (1)	8:7	VMIDSEL	00	Vmid divider enable and select 00 – Vmid disabled (for OFF mode) 01 – 50kΩ divider enabled (for playback/record) 10 – 500kΩ divider enabled (for low-power standby) 11 – 5kΩ divider enabled (for fast start-up)
	6	VREF	0	VREF (necessary for all other functions) 0 = Power down 1 = Power up
	5	AIN	0	Analogue in PGA 0 = Power down 1 = Power up
	3	ADC	0	ADC 0 = Power down 1 = Power up
R26 (1Ah) Power Management (2)	8	DAC	0	DAC 0 = Power down 1 = Power up
	6	AOUT	0	AOUT Output Buffer* 0 = Power down 1 = Power up
* The mixer is enabled when AOUT=1.				

Table 29 Power Management

STOPPING THE MASTER CLOCK

In order to minimise power consumed in the digital core of the CJC8911, the master clock may be stopped in Standby and OFF modes. If this cannot be done externally at the clock source, the DIGENB bit (R25, bit 0) can be set to stop the MCLK signal from propagating into the device core. In Standby mode, setting DIGENB will typically provide an additional power saving on DCVDD of 20uA.

However, since setting DIGENB has no effect on the power consumption of other system components external to the CJC8911, it is preferable to disable the master clock at its source wherever possible.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R25 (19h) Additional Control (1)	0	DIGENB	0	Master clock disable 0: master clock enabled 1: master clock disabled

Table 30 ADC and DAC Oversampling Rate Selection

Note:

Before DIGENB can be set, the control bits ADCL and DAC must be set to zero and a waiting time of 1ms must be observed. Any failure to follow this procedure may prevent DACs and ADCs from re-starting correctly.

SAVING POWER BY REDUCING BIAS CURRENTS

The design of the DAC allows user trade-off between power consumption and performance, using the DACMIXBIAS bit. The default setting (DACMIXBIAS=0) delivers the best audio performance. Setting DACMIXBIAS=1 reduces AVDD current consumption, at the cost of marginally reduced performance (see “Electrical Characteristics” for details).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R67 (43h)	3	DACMIX BIAS	0	DAC biasing 0 = high bias current (results in higher performance and power consumption) 1 = low bias current (results in lower performance and power consumption)

Table 31 DAC Biasing

SAVING POWER BY REDUCING OVERSAMPLING RATE

The default mode of operation of the ADC and DAC digital filters is in 128x oversampling mode. Under the control of ADCOSR and DACOSR the oversampling rate may be halved. This will result in a slight decrease in noise performance but will also reduce the power consumption of the device. In USB mode ADCOSR must be set to 0, i.e. 128x oversampling.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24 (18h) Additional Control (2)	1	ADCOSR	0	ADC oversample rate select 1 = 64x (lowest power) 0 = 128x (best SNR)
	0	DACOSR	0	DAC oversample rate select 1 = 64x (lowest power) 0 = 128x (best SNR)

Table 32 ADC and DAC Oversampling Rate Selection

ADCOSR set to '1', 64x oversample mode, is not supported in USB mode (USB=1).

SAVING POWER AT HIGHER SUPPLY VOLTAGES

The analogue supplies to the CJC8911 can run from 1.8V to 3.3V. By default, all analogue circuitry on the device is optimized to run at 3.3V. This set-up is also good for all other supply voltages down to 1.8V. At lower voltages, performance can be improved by increasing the bias current.If low power operation is preferred the bias current can be left at the default setting. This is controlled as shown below.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R23 (17h) Additional Control (1)	7:6	VSEL [1:0]	11	Analogue Bias optimization 00: Highest bias current, optimized for AVDD=1.8V 01: Bias current optimized for AVDD=2.4V 1X: Lowest bias current, optimized for AVDD=3.3V

Device shutdown mode

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R37 (25h) Additional Control (1)	3	SDB	0	0=shutdown mode 1=operation mode

REGISTER MAP

REGISTER	ADDRESS (Bit 15 – 9)	remarks	Bit[8]	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	default	page ref
R0 (00h)	0000000	Input volume	IVU	INMUTE	IZC	INVOL						10010111	23
R1 (01h)	0000001	Reserved	0	0	0	0	0	0	0	0	0	00000000	-
R2 (02h)	0000010	OUT volume	OVU	OZC	OUTVOL[6:0]							01111001	38
R3 (03h)	0000011	Reserved	0	0	0	0	0	0	0	0	0	00000000	-
R4 (04h)	0000100	Reserved	0	0	0	0	0	0	0	0	0	00000000	-
R5 (05h)	0000101	ADC & DAC Control	ADCDIV2	DACDIV2	0	ADCPOL	HPOR	DACMU	DEEMPH[1:0]		ADCHPD	00001000	24,32,35
R6 (06h)	0000110	Reserved	0	0	0	0	0	0	0	0	0	00000000	-
R7 (07h)	0000111	Audio Interface	0	BCLKINV	MS	LRSWAP	LRP	WL[1:0]		FORMAT[1:0]		00001010	45
R8 (08h)	0001000	Sample rate	BCM[1:0]		CLKDIV2	SR[4:0]					USB	00000000	47,48
R9 (09h)	0001001	Reserved	0	0	0	0	0	0	0	0	0	00000000	-
R10 (0Ah)	0001010	DAC volume	DVU	DACVOL[7:0]								11111111	33
R11 (0Bh)	0001011	Reserved	0	0	0	0	0	0	0	0	0	00000000	-
R12 (0Ch)	0001100	Bass control	0	BB	BC	0	0	BASS[3:0]				00001111	34
R13 (0Dh)	0001101	Treble control	0	0	TC	0	0	TRBL[3:0]				00001111	34
R15 (0Fh)	0001111	Reset	writing to this register resets all registers to their default state									not reset	-
R16 (10h)	0010000	3D control	0	0	3DUC	3DLC	3DDEPTH[3:0]				3DEN	00000000	31
R17 (11h)	0010001	ALC1	ALCSEL	0	MAXGAIN[2:0]			ALC[3:0]				01111011	28
R18 (12h)	0010010	ALC2	0	ALCZC	0	0	0	HLD[3:0]				00000000	28
R19 (13h)	0010011	ALC3	0	DCY[3:0]				ATK[3:0]				00110010	28
R20 (14h)	0010100	Noise Gate	0	NGTH[4:0]					NGG[1:0]		NGAT	00000000	30
R21 (15h)	0010101	ADC volume	AVU	ADCVOL[7:0]								11000011	25

R22 (16h)	0010110	Reserved	0	0	0	0	0	0	0	0	0	00000000	-
R23 (17h)	0010111	Additional control(1)	TSDEN	VSEL[1:0]		DMONOMIX[1:0]		0	0	DACINV	TOEN	11000000	23,36,40,55
R24 (18h)	0011000	Additional control(2)		COMEN	0	0	0	TRI	LRCM	ADCOSR	DACOSR	00000000	39,46,55
R25 (19h)	0011001	Pwr Mgmt (1)	VMIDSEL[1:0]		VREF	AIN	0	ADC	0	0	DIGENB	00000000	53,54
R26 (1Ah)	0011010	Pwr Mgmt (2)	DAC	0	AOUT	0	0	0	0	0	0	00000000	39,53
R27 (1Bh)	0011011	Additional Control (3)	0	0	VROI	0	0	0	0	0	0	00000000	39
R31 (1Fh)	0011111	Reserved	0	0	0	0	0	0	0	0	0	00000000	-
R32 (20h)	0100000	ADC signal path	MIC_DIF_EN	0	0	MICBOOST[1:0]		0	0	0	0	00000000	22
R33 (21h)	0100001	MIC	0	0	0	0	MIC2O	MIC2OVOL[3:0]				00001010	37
R34 (22h)	0100010	AUX	0	0	0	0	AUL2O	AUL2OVOL[3:0]				00001010	37
R35 (23h)	0100011	Out Mix (2)	0	D2O	0	0	0	0	0	0	0	01010000	37
R36 (24h)	0100100	Reserved	0	0	0	0	0	0	0	0	0	00000000	-
R37 (25h)	0100101	Adc_pdn sel	0	0	0	0	0	SDB	0	0	0	00000000	56
R38 (26h)	0100110	Reserved	0	0	0	0	0	0	0	0	0	00000000	-
R39 (27h)	0100111	Reserved	0	0	0	0	0	0	0	0	0	00000000	-
R40 (28h)	0101000	Reserved	0	0	0	0	0	0	0	0	0	00000000	-
R41 (29h)	0101001	Reserved	0	0	0	0	0	0	0	0	0	00000000	-
R42 (2Ah)	0101010	Reserved	0	0	0	0	0	0	0	0	0	00000000	-
R67 (43h)	1000011	Low Power Playback	0	0	0	0	0	0	DACMIX BIAS	0	0	00000000	54

DIGITAL FILTER CHARACTERISTICS

The ADC and DAC employ different digital filters. There are 4 types of digital filter, called Type 0, 1, 2 and 3. The performance of Types 0 and 1 is listed in the table below, the responses of all filters is shown in the proceeding pages.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Filter Type 0 (USB Mode, 250fs operation)					
Passband	+/- 0.05dB	0		0.416fs	
	-6dB		0.5fs		
Passband Ripple				+/- 0.05	dB
Stopband		0.584fs			
Stopband Attenuation	f > 0.584fs	-60			dB
ADC Filter Type 1 (USB mode, 272fs or Normal mode operation)					
Passband	+/- 0.05dB	0		0.4535fs	
	-6dB		0.5fs		
Passband Ripple				+/- 0.05	dB
Stopband		0.5465fs			
Stopband Attenuation	f > 0.5465fs	-60			dB
High Pass Filter Corner Frequency	-3dB		3.7		Hz
	-0.5dB		10.4		
	-0.1dB		21.6		
DAC Filter Type 0 (USB mode, 250fs operation)					
Passband	+/- 0.03dB	0		0.416fs	
	-6dB		0.5fs		
Passband Ripple				+/-0.03	dB
Stopband		0.584fs			
Stopband Attenuation	f > 0.584fs	-50			dB
DAC Filter Type 1 (USB mode, 272fs or Normal mode operation)					
Passband	+/- 0.03dB	0		0.4535fs	
	-6dB		0.5fs		
Passband Ripple				+/- 0.03	dB
Stopband		0.5465fs			
Stopband Attenuation	f > 0.5465fs	-50			dB

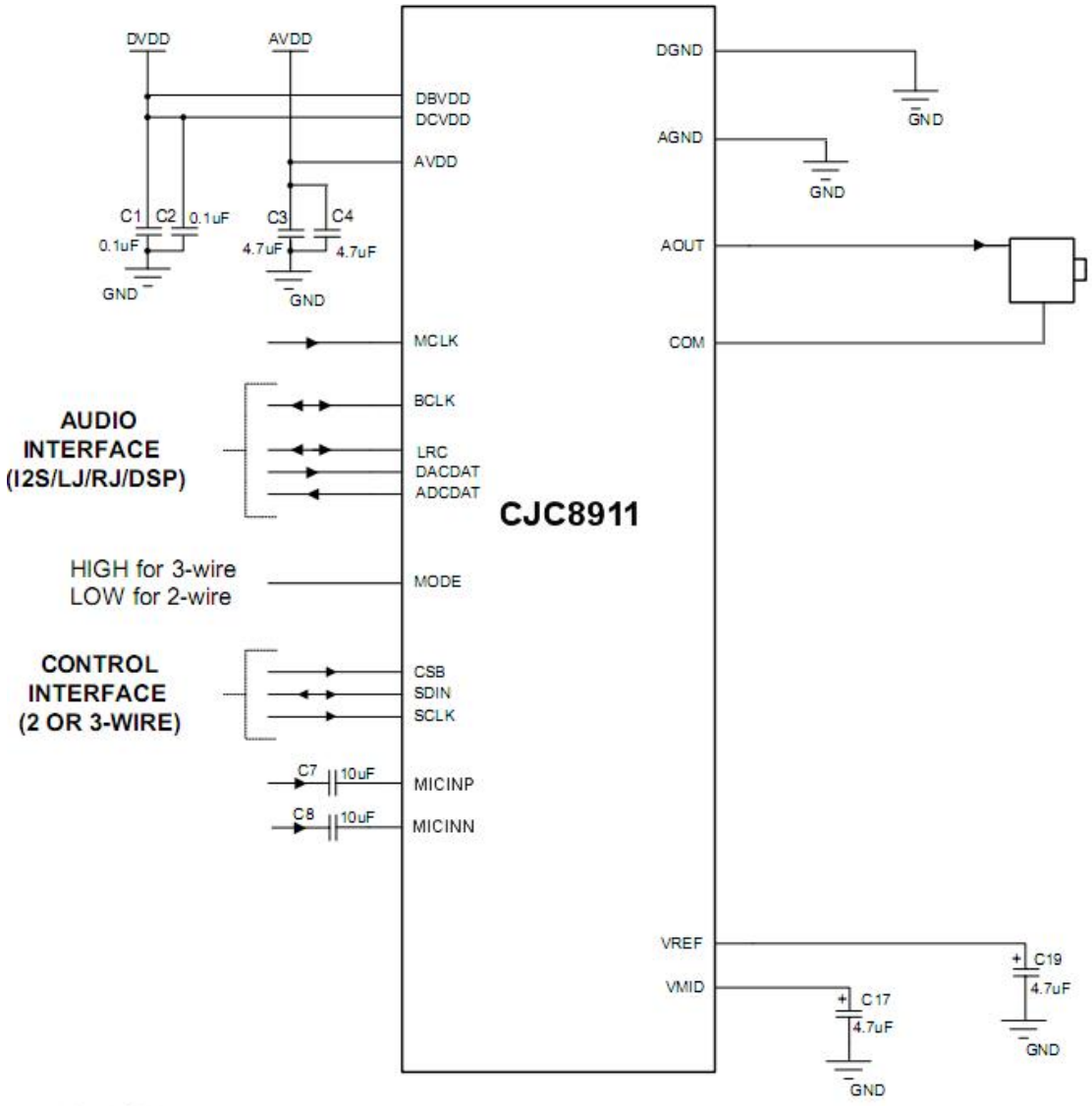
Table 33 Digital Filter Characteristics

DAC FILTERS		ADC FILTERS	
Mode	Group Delay	Mode	Group Delay
0 (250 USB)	11/FS	0 (250 USB)	13/FS
1 (256/272)	16/FS	1 (256/272)	23/FS
2 (250 USB, 96k mode)	4/FS	2 (250 USB, 96k mode)	4/FS
3 (256/272, 88.2/96k mode)	3/FS	3 (256/272, 88.2/96k mode) 3/FS	5/FS

Table 34 ADC/DAC Digital Filters Group Delay

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS



Layout Notes:

1. C1 to C4, C17, C19, C20 should be as close to the relative CJC8911 connecting pin as possible.
2. For capacitors C7 to C8 , C14, it is recommended that low ESR components are used.
3. COM should be connected to GND at the connector.

Figure 20 Recommended External Components Diagram

LINE INPUT CONFIGURATION

When MICINP/MICINN are used as line inputs, the microphone boost and ALC functions should normally be disabled. In order to avoid clipping, the user must ensure that the input signal does not exceed AVDD. This may require a potential divider circuit in some applications. It is also recommended to remove RF interference picked up on any cables using a simple first-order RC filter, as high-frequency components in the input signal may otherwise cause aliasing distortion in the audio band. AC signals with no DC bias should be fed to the CJC8911 through a DC blocking capacitor, e.g. 10μF.

LINE OUTPUT CONFIGURATION

The analogue outputs, AOUT , can be used as line outputs. Recommended external components are shown below.

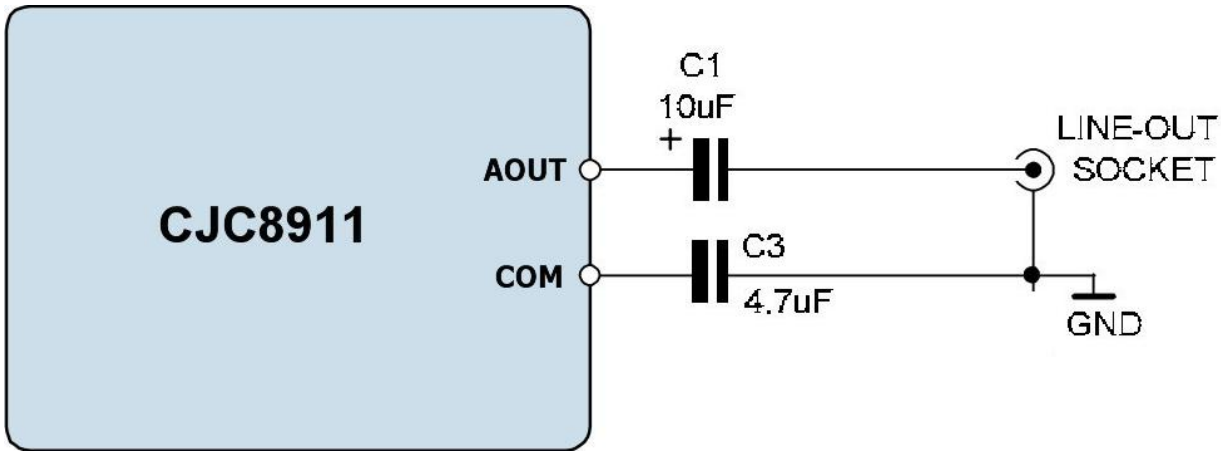


Figure 21 Recommended Circuit for Line Output

The DC blocking capacitors and the load resistance together determine the lower cut-off frequency, fc. Assuming a 10 kΩ load and C1, C2 = 1μF:

$$fc = 1 / 2\pi (RL+R1) C1 = 1 / (2\pi \times 10.1k\Omega \times 1\mu F) = 16 Hz$$

Increasing the capacitance lowers fc, improving the bass response. Smaller values of C1 and C2 will diminish the bass response. The function of R1 and R2 is to protect the line outputs from damage when used improperly.

MINIMISING POP NOISE AT THE ANALOGUE OUTPUTS

To minimize any pop or click noise when the system is powered up or down, the following procedures are recommended.

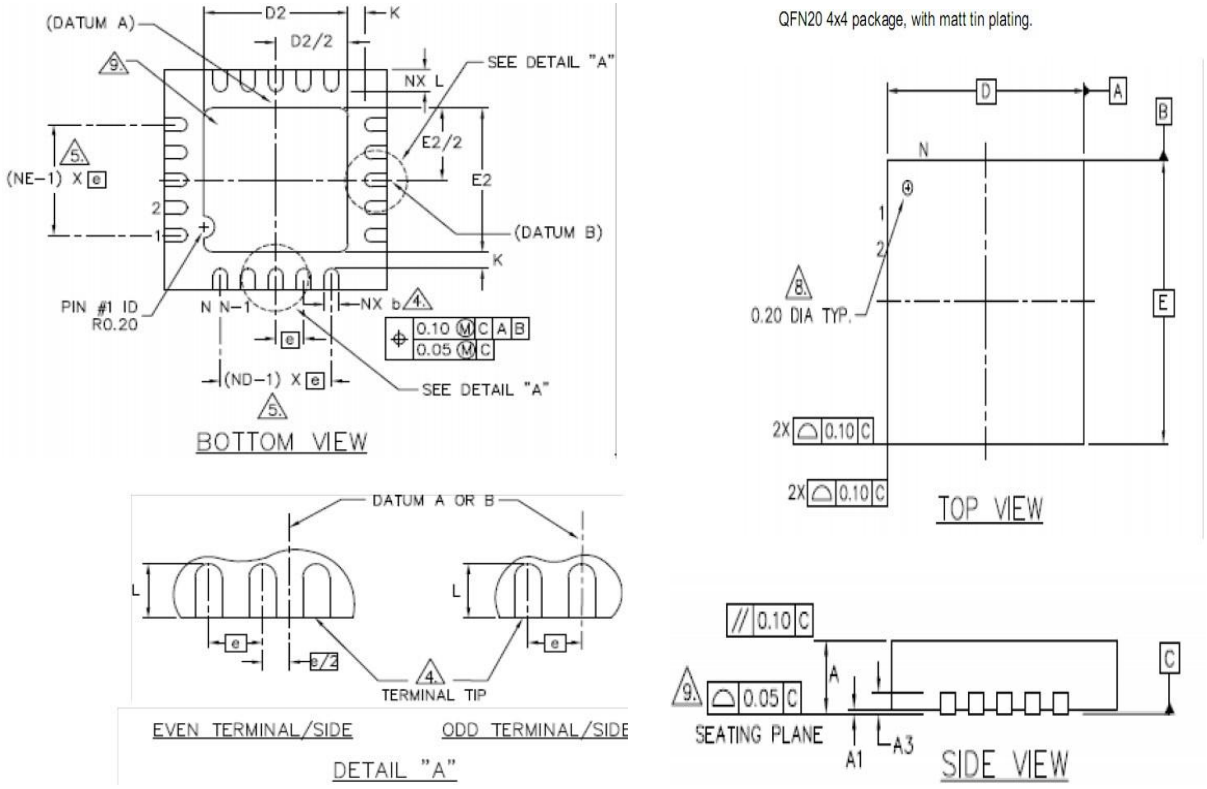
POWER UP

- Switch on power supplies. By default the CJC8911 is in Standby Mode, the DAC is digitally muted and the Audio Interface, Line outputs are all OFF (DACMU = 1 Power Management registers 1 and 2 are all zeros).
- Enable Vmid and VREF.
- Enable DACs as required
- Enable line output buffers as required.
- Set DACMU = 0 to soft-un-mute the audio DACs.

POWER DOWN

- Set DACMU = 1 to soft-mute the audio DACs.
- Disable all output buffers.
- Switch off the power supplies.

PACKAGE DIMENSIONS



Package Type		A	A1	A3	K	D/E	e	D2/E2	L	L1	b
Saw QFN20 (4x4 mm)	**Min.**	0.80	0.00					2.50	0.35		0.18
	Typ.	0.85	0.02	0.20	0.20	4.0	0.5 BSC	2.60	0.40	0.15	0.25
	Max	0.95	0.05	REF.	min.	BSC[a]		2.70	0.45	max	0.30

a. BSC: Basic Spacing between Centers, ref. JEDEC standard 95, page 4.17-11/A

Notes:

1. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 mm AND 0.30 mm FROM TERMINAL TIP.
2. ALL DIMENSIONS ARE IN MILLIMETRES.
3. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
4. REFER TOAPPLICATIONS NOTE WAN_0118 FOR FURTHER INFORMATION REGARDING PCB FOOTPRINTS AND QFN PACKAGE SOLDERING.
5. DEPENDING ON THE METHOD OF LEAD TERMINATION AT THE EDGE OF THE PACKAGE, PULL BACK (L1) MAY BE PRESENT.
6. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.