多通道CODEC

(6channel-ADC/2channel-DAC)

Edition	Author	Date	Description
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DESCRIPTION

The CJC6808 are low power multi route direct sound gathering CODECs. The CJC6808 is also ideal for MD, CD-RW machines and DAT recorders.

The CJC6808 include 6 ADCs and 2 DACs, along with a mute function, programmable line level volume control and a bias voltage output suitable for an electronic microphone. Stereo 24-bit multi-bit sigma delta ADCs and DACs are used with oversampling digital interpolation and decimation filters. Digital audio input word lengths from 16-32 bits and sampling rates from 8kHz to 96kHz are supported. Line level outputs are also provided along with anti-thump mute and power up/down circuitry.

The CJC6808 also include a PLL which can produce 11.2896MHZ clock. Then only 12.288MHZ crystal is needed and we need not change crystal . A sar adc is also put into to wake up the chip when the music coming in .

The device is controlled via a 2 or 3 wire serial interface. The interface provides access to all features including volume controls, mutes, de-emphasis and extensive power management facilities. The smaller 48 lead quad flat leadless package (QFN).

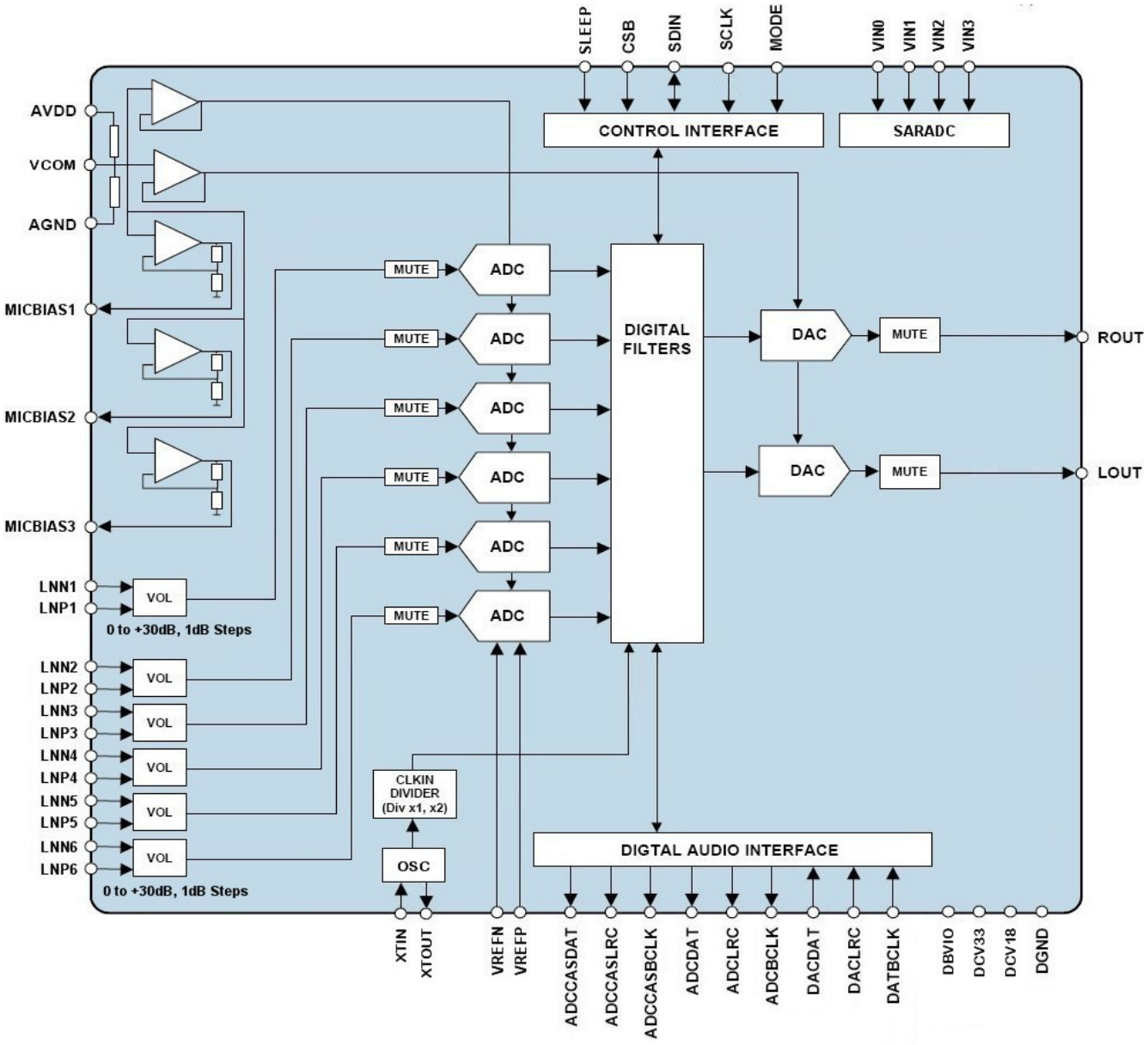
FEATURES

- Audio Performance
  - ADC SNR 95dB (‘A’ weighted) at 3.3V
  - DAC SNR 98dB (‘A’ weighted) at 3.3V
- ADC and DAC Sampling Frequency: 8kHz – 96kHz
  ADC : 16K 32K
  DAC : 8K 32K 44.1K 48K 88.2K 96K
- Selectable ADC High Pass Filter
- Programmable ALC / Noise Gate
- 2 or 3-Wire MPU Serial Control Interface
- Programmable Audio Data Interface Modes
  - I2S, Left, Right Justified
  - 16/20/24/32 bit Word Lengths of DAC
  - Master or Slave Clocking Mode
  -Cascade TDM interface of ADC
- Microphone differential input
- Available in 48-lead QFN package

APPLICATIONS

- Recorders
- PDAs / smartphones

BLOCK DIAGRAM



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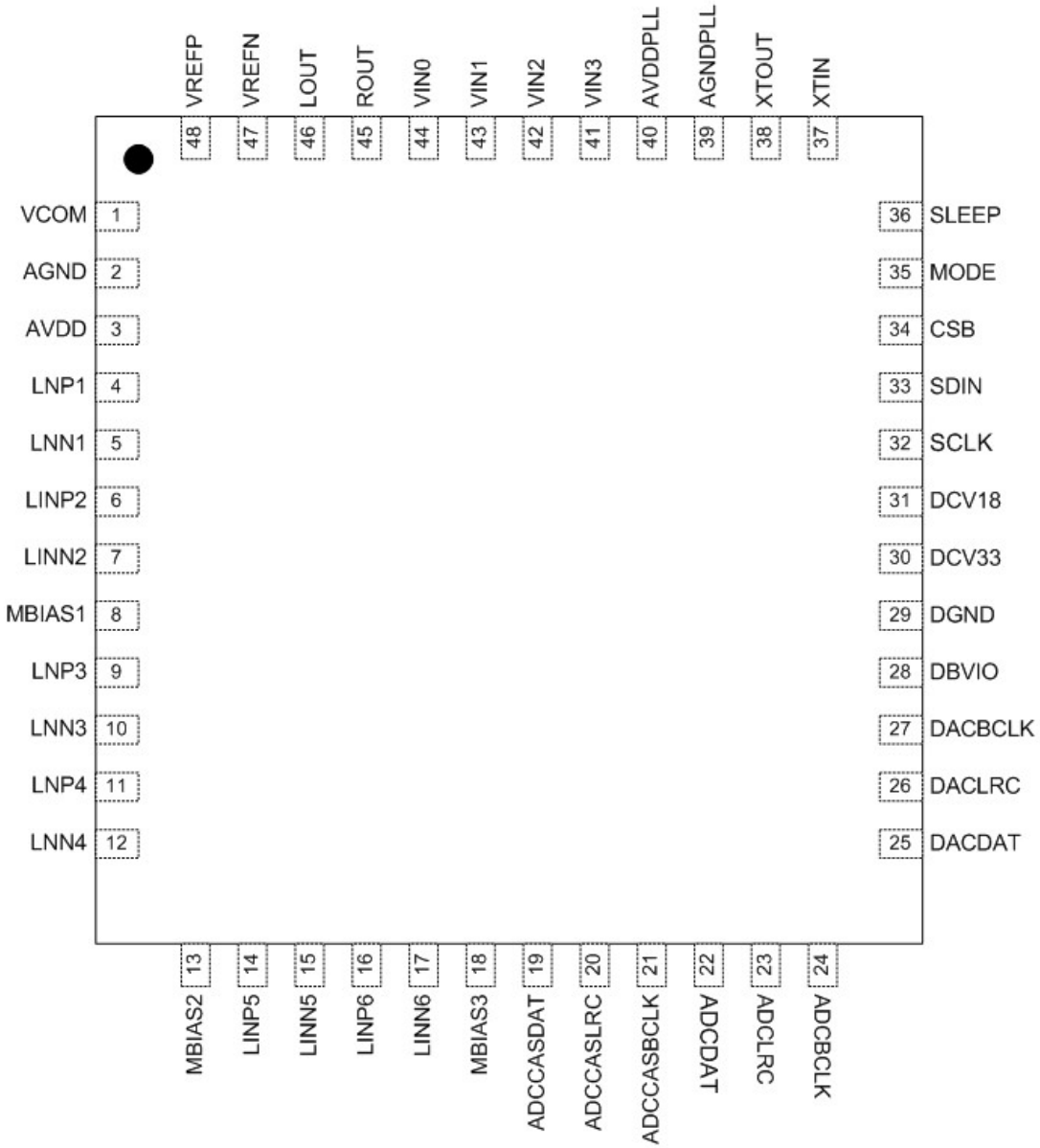
PIN CONFIGURATION – 48 PIN QFN



PIN DESCRIPTION

28PIN QFN	NAME	TYPE	DESCRIPTION
1	VCOM	O	Midrail Voltage Decoupling Capacitor
2	AGND	Ground	Analogue GND
3	AVDD	Supply	Analogue VDD
4	LINP1	I	Channel Line Input P 1 (AC coupled)
5	LINN1	I	Channel Line Input N 1 (AC coupled)
6	LINP2	I	Channel Line Input P 2 (AC coupled)
7	LINN2	I	Channel Line Input N 2 (AC coupled)
8	MICBIAS1	O	Electret Microphone Bias1
9	LINP3	I	Channel Line Input P 3 (AC coupled)
10	LINN3	I	Channel Line Input N 3 (AC coupled)
11	LINP4	I	Channel Line Input P 4 (AC coupled)
12	LINN4	I	Channel Line Input N 4 (AC coupled)
13	MICBIAS2	O	Electret Microphone Bias2
14	LINP5	I	Channel Line Input P 5 (AC coupled)
15	LINN5	I	Channel Line Input N 5 (AC coupled)
16	LINP6	I	Channel Line Input P 6 (AC coupled)
17	LINN6	I	Channel Line Input N 6 (AC coupled)
18	MICBIAS3	O	Electret Microphone Bias3
19	ADCCASDAT	IO	ADC cascade data transmit or receive data port
20	ADCCASLRC	IO	ADC cascade data transmit or receive channel clock port
21	ADCCASBCLK	IO	ADC cascade data transmit or receive bit clock port
22	ADCDAT	O	ADC Digital Audio Data Output
23	ADCLRC	IO	ADC Sample Rate Left/Right Clock, Pull Down (see Note 1)
24	ADCBCLK	IO	ADC data output bit clock(see Note 1)
25	DACDAT	I	DAC Digital Audio Data Input
26	DACLRC	I/O	DAC Sample Rate Left/Right Clock, Pull Down (see Note 1)
27	DACBCLK	IO	DAC Bit Clock, Pull Down, (see Note 1)
28	DBVIO	Supply	Digital IO Power
29	DGND	Ground	Digital GND
30	DCV33	Supply	Ldo Power 3.3v
31	DCV18	O	Digital Core Power 1.8v
32	SCLK	I	3-Wire MPU Clock Input / 2-Wire MPU Clock Input
33	SDIN	I/O	3-Wire MPU Data Input / 2-Wire MPU Data Input
34	CSB	I	3-Wire MPU Chip Select/ 2-Wire MPU interface address selection, active low, Pull up (see Note 1)
35	MODE	I	Control Interface Selection, Pull Up (see Note 1)
36	SLEEP	I	Halt Mode Contral

37	XTIN	I	12.288M Oscillator input
38	XTOUT	O	12.288M Oscillator output
39	AGNDPLL	Ground	Pll GND
40	AVDDPLL	Supply	Pll VDD
41	VIN3	I	SARADC INPUT3
42	VIN2	I	SARADC INPUT2
43	VIN1	I	SARADC INPUT1
44	VIN0	I	SARADC INPUT0
45	ROUT	O	Right Channel Line Output
46	LOUT	O	Left Channel Line Output
47	VREFN	O	DAC Negative input Range (GND)
48	VREFP	O	DAC Positive input Range (VDD)

Note:

1. Pull Up/Down only present when Control Register Interface ACTIVE=0 to conserve power.
2. It is recommended that the QFN ground paddle is connected to analogue ground on the application PCB.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Chinaic semiconductor tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30° C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30° C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30° C / 60% Relative Humidity. Supplied in moisture barrier bag.

CONDITION	MIN	MAX
Digital supply voltage	-0.3V	+3.6V
Analogue supply voltage	-0.3V	+3.6V
Voltage range digital inputs	DGND -0.3V	DVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Operating temperature range, T_A	-25° C	+85° C
Storage temperature after soldering	-65° C	+150° C

Notes:

1. Analogue and digital grounds must always be within 0.3V of each other.

2. The digital supply core voltage (DCVDD) must always be less than or equal to the analogue supply voltage (AVDD)

RECOMMENDED OPERATING CONDITIONS – CJC6808

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range (Core)	DCVDD		2.4	3.3	3.6	V
Digital supply range (Buffer)	DBVDD		2.4	3.3	3.6	V
Analogue supply range	AVDD		2.7	3.3	3.6	V
Ground	DGND,AGND			0		V

TERMINOLOGY

1. Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).

2. Dynamic range (dB) - DR is a measure of the difference between the highest and lowest portions of a signal. ormally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= -31dB, DR= 91dB).

3. THD+N (dB) - THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.

4. Channel Separation (dB) - Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.

ELECTRICAL CHARACTERISTICS – CJC6808

Test Conditions

AVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 3.3V, DGND = 0V, TA = +25oC, Slave Mode, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Logic Levels (CMOS Levels)						
Input LOW level	V_{IL}				0.3 x DBVDD	V
Input HIGH level	V_{IH}		0.7 x DBVDD		0.10 x DBVDD	V
Output LOW	V_{OL}					V
Output HIGH	V_{OH}		0.9 x DBVDD			V
Power On Reset Threshold (DCVDD)						
DCVDD Threshold On -> Off	V_{th}		0.9			V
Hysteresis	V_{IH}		0.3			V
DCVDD Threshold Off -> On	V_{OL}		0.6			V
Analogue Reference Levels						
Reference voltage (VMID)	V_{VMID}			AVDD/2		V
Potential divider resistance	R_{VMID}			50k		Ω

Test Conditions

AVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 3.3V, DGND = 0V, TA = +25oC, Slave Mode, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Line Input to ADC						
Input Signal Level (0dB)	V_{INLINE}			0.9 AVDD		VPP
Signal to Noise Ratio (Note 1,3)	SNR	A-weighted, 0dB gain @ fs = 48kHz		95		dB
		A-weighted, 0dB gain @ fs = 96kHz		94		
Dynamic Range (Note 3)	DR	A-weighted, -60dB full scale input		95		dB
Total Harmonic Distortion	THD	-1dBv input, 0dB gain		-85		dB
Power Supply Rejection Ratio	PSRR	1kHz, 50mVpp		65		dB
ADC channel separation				-120		dB
Input Resistance	R_{INLINE}	0dB gain	20k	30k		Ω
		12dB gain	10k	15k		
Input Capacitance	C_{INLINE}			10		pF

Test Conditions

AVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 3.3V, DGND = 0V, TA = +25oC, Slave Mode, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Microphone Bias						
Bias Voltage	VMICBIAS		0.75*AVDD – 100mV	0.75*AVDD	0.75*AVDD + 100mV	V
Bias Current Source	IMICBIAS				3	mA

Output Noise Voltage	**Vn**	**1K to 20kHz**		**25**		**nV/√Hz**
Line Output for DAC Playback Only (Load = 10kΩ. 50pF)						
Signal to Noise Ratio (Note 1,3)	**SNR**	**A-weighted, @ fs = 48kHz**		**98**		**dB**
		A-weighted @ fs = 96kHz		**94**		
Dynamic Range (Note 3)	**DR**	**A-weighted, -60dB full scale input**		**98**		**dB**
Total Harmonic Distortion	**THD+N**	**1kHz, 0dBfs**		**-85**		**dB**
		1kHz, -3dBfs		**-**		
Power Supply Rejection Ratio	**PSRR**	**1kHz 50mVpp**		**65**		**dB**
DAC channel separation				**-120**		**dB**

Test Conditions

AVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 3.3V, DGND = 0V, TA = +25oC, Slave Mode, fs = 48kHz, MCLK = 256fs unless otherwise stated.

Notes:

1. Ratio of output level with 1kHz full scale input, to the output level with the input short circuited, measured 'A' weighted over a 20Hz to 20kHz bandwidth using an Audio analyser.
2. Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured 'A' weighted over a 20Hz to 20kHz bandwidth.
3. All performance measurements done with 20kHz low pass filter, and where noted an A-weight filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
4. VMID decoupled with 10uF and 0.1uF capacitors (smaller values may result in reduced performance).

POWER CONSUMPTION – CJC6808

MODE DESCRIPTION	POWEROFF	CLKOUTP	OSCPD	OUTPD	DACPD	ADCPD	MICPD	LINEINPD	CURRENT CONSUMPTION TYPICAL				
									AVDD (3.3V)		DCVDD (1.5V)	DBVDD (3.3V)	UNIT
Oscillator enabled	0	0	0	0	0	0	0	0	3		2.61	1.03	mA
Playback Only													
OSC enabled	0	0	0	0	0	1	1	1	5.8		1.5	1.09	mA
Record Only													
Line Record, OSC enabled	0	0	0	1	1	0	1	0	4		2.04	1.13	mA
Analogue Bypass (Line-in to Line-out)													
External clock still running	0	0	1	0	1	1	1	0	0.4		0.9	1.09	mA
Standby													
External clock still running	0	1	1	1	1	1	1	1	0.4		0.48	0.18	mA
Power Down													
External clock still running	1	1	1	1	1	1	1	1	0.4		0.46	0.03	mA

Table 1 Powerdown Mode Current Consumption Examples

Notes:

1. TA = +25oC. fs = 48kHz, MCLK = 256fs (12.288MHz).
2. The data presented here was measured with the audio interface in master mode whenever the internal clock oscillator as used, and in slave mode whenever an external clock was used. owever, it is also possible.
3. All figures are quiescent, with no signal..
4. The power dissipation in the headphone itself not included in the above tab

MASTER CLOCK TIMING

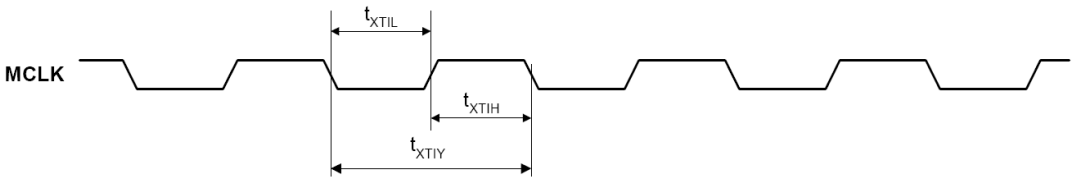


Figure 1 System Clock Timing Requirements

Test Conditions

AVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 3.3V, DGND = 0V, TA = +25oC, Slave Mode fs = 48kHz, MCLK =256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
MIN TYP MAX UNIT						
MCLK System clock pulse width high	**tXTIH**		**18**			**ns**
MCLK System clock pulse width low	**tXTIL**		**18**			**ns**
MCLK System clock cycle time	**tXTIY**		**54**			**ns**
MCLK Duty cycle			**40:60**		**60:40**	

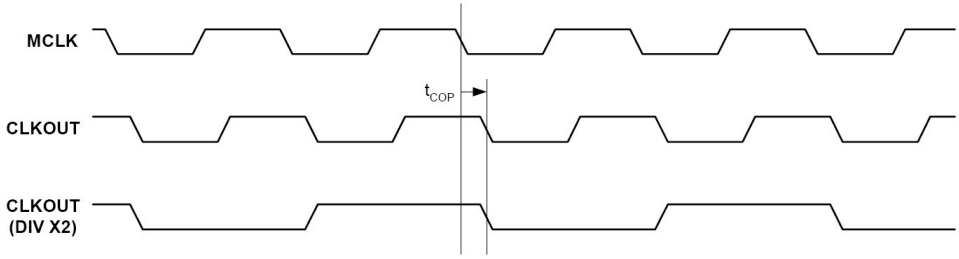


Figure 2 Clock Out Timing Requirements

Test Conditions

AVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 3.3V, DGND = 0V, TA = +25oC, Slave Mode fs = 48kHz, MCLK = 56fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
CLKOUT propagation delay from MCLK falling edge	**tCOP**		**0**		**10**	**ns**

DIGITAL AUDIO INTERFACE – MASTER MODE

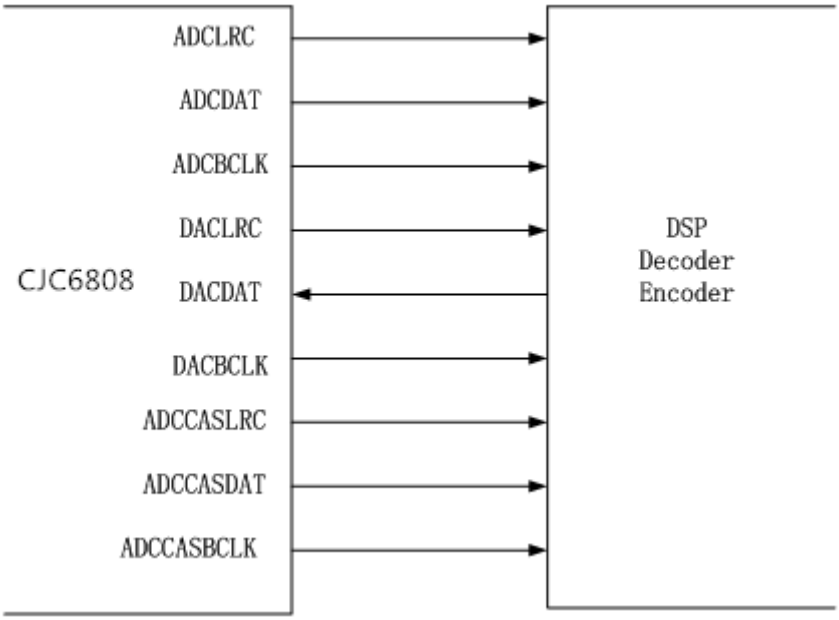


Figure 3 Master Mode Connection

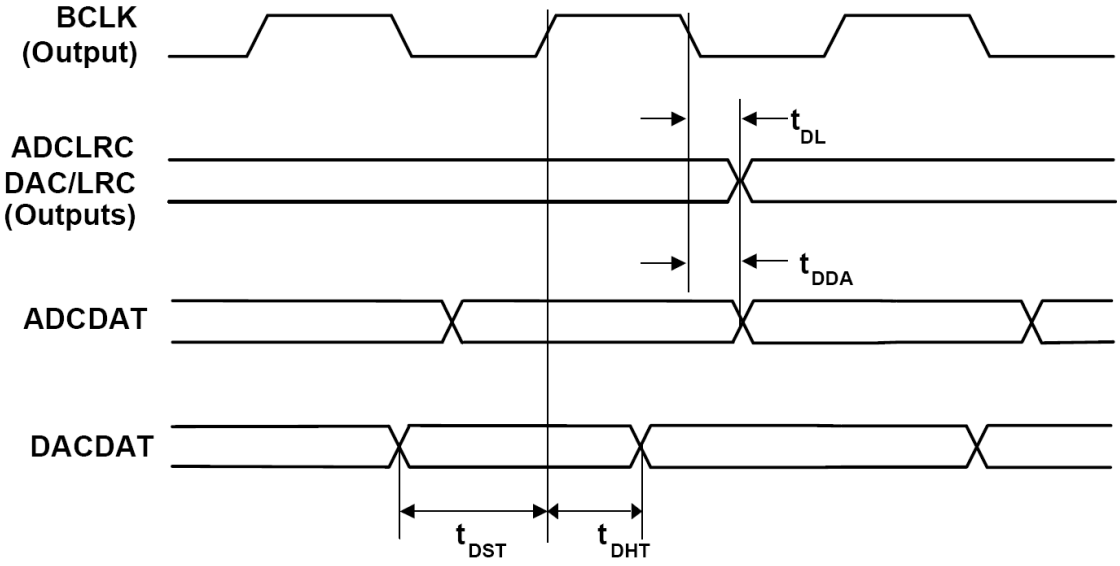


Figure 4 Digital Audio Data Timing – Master Mode

Test Conditions

AVDD, DBDD = 3.3V, AGND = 0V, DCVDD = 3.3V, DGND = 0V, TA = +25oC, Slave Mode, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
ADCLRC/DACLRC propagation delay from BCLK falling edge	**tDL**		**0**		**10**	**ns**
ADCDAT propagation delay from BCLK falling edge	**tDDA**		**0**		**15**	**ns**
DACDAT setup time to BCLCK rising edge	**tDST**		**10**			**ns**
DACDAT hold time from DACBCLK rising edge	**tDHT**		**10**			**ns**

DIGITAL AUDIO INTERFACE – SLAVE MODE

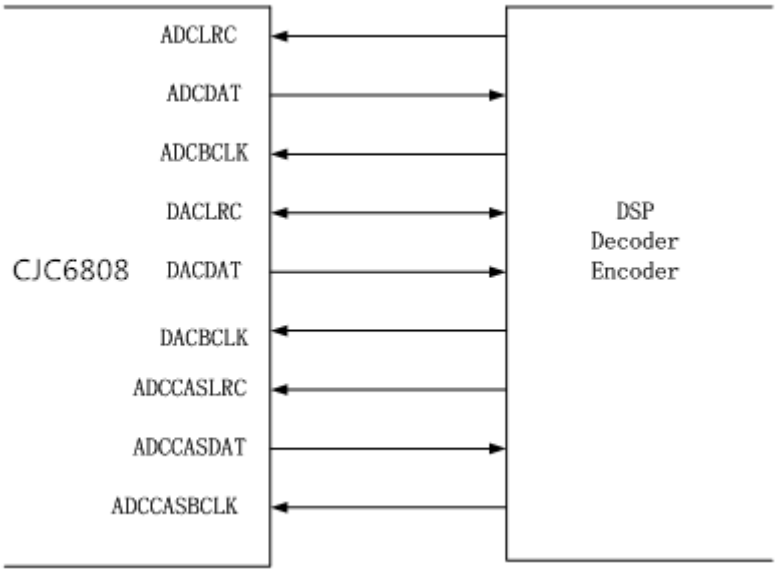


Figure 5 Slave Mode Connection

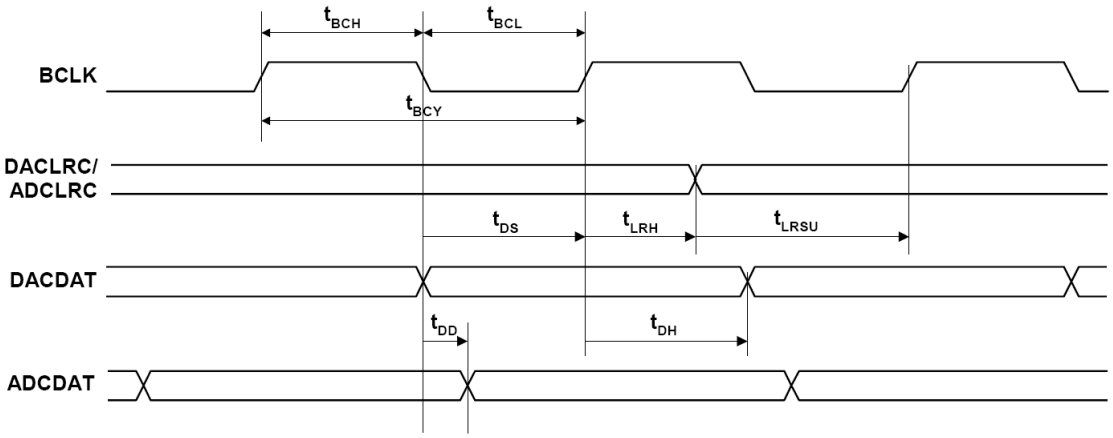


Figure 6 Digital Audio Data Timing – Slave Mode

Test Conditions

AVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 3.3V, DGND = 0V, TA = +25oC, Slave Mode, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
BCLK cycle time	tBCY		50			ns
BCLK pulse width high	tBCH		20			ns
BCLK pulse width low	tBCL		20			ns
DACLRC/ADCLRC set-up time to BCLK rising edge	tLRSU		10			ns
DACLRC/ADCLRC hold time from BCLK rising edge	tLRH		10			ns
DACDAT set-up time to BCLK rising edge	tDS		10			ns
DACDAT hold time from BCLK rising edge	tDH		10			ns
ADCDAT propagation delay from BCLK falling edge	tDD		0		10	ns

MPU INTERFACE TIMING

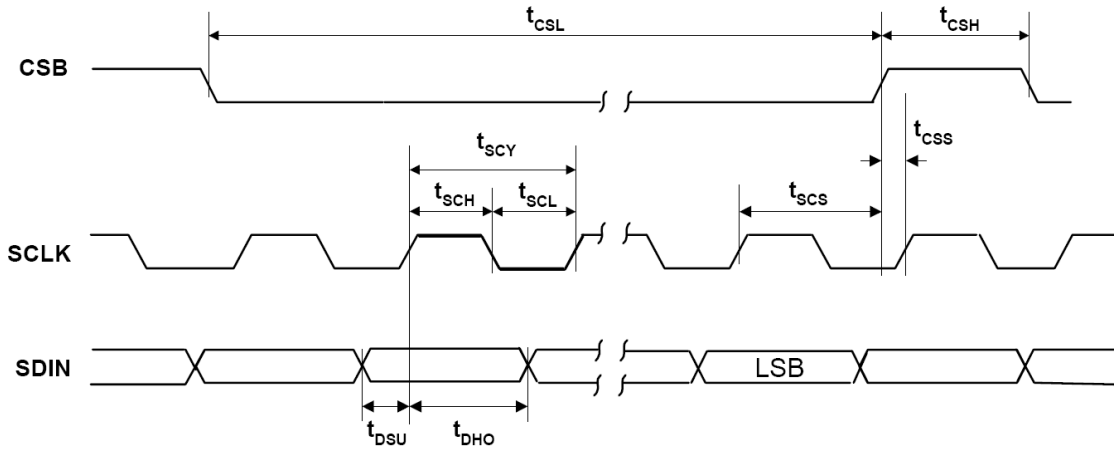


Figure 7 Program Register Input Timing - 3-Wire MPU Serial Control Mode

Test Conditions

AVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 3.3V, DGND = 0V, TA = +25oC, Slave Mode, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Program Register Input Information						
SCLK rising edge to CSB rising edge	tSCS		60			ns
SCLK pulse cycle time	tSCY		80			ns
SCLK pulse width low	tSCL		20			ns
SCLK pulse width high	tSCH		20			ns
SDIN to SCLK set-up time	tDSU		20			ns
SCLK to SDIN hold time	tDHO		20			ns
CSB pulse width low	tCSL		20			ns
CSB pulse width high	tCSH		20			ns
CSB rising to SCLK rising	tCSS		20			ns

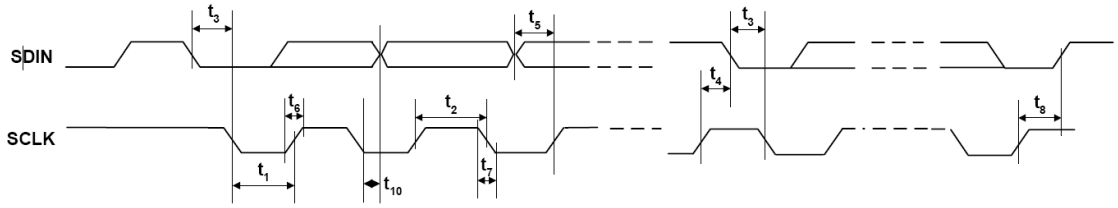


Figure 8 Program Register Input Timing – 2-Wire MPU Serial Control Mode

Test Conditions

AVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 3.3V, DGND = 0V, TA = +25oC, Slave Mode, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Program Register Input Information						
SCLK Frequency	t1		0		526	kHz
SCLK Low Pulsewidth			1.3			us
SCLK High Pulsewidth	t2		600			ns
Hold Time (Start Condition)	t3		600			ns
Setup Time (Start Condition)	t4		600			ns
Data Setup Time	t5		100			ns
SDIN, SCLK Rise Time	t6					ns
SDIN, SCLK Fall Time	t7				300	ns
Setup Time (Stop Condition)	t8		600		300	ns
Data Hold Time	t10				900	ns

DEVICE DESCRIPTION

INTRODUCTION

The CJC6808 is a low power audio CODEC designed specifically for portable audio products. It's features, performance and low power consumption make it ideal for music players and music signal accepter.

The CODEC includes six line and microphone inputs to the on-board ADCs, line outputs from the on-board DAC, a crystal oscillator, configurable digital audio interface and a choice of 2 or 3 wire MPU control interface. It is fully compatible and an ideal partner for a range of industry standard microprocessors, controllers and DSPs.

The CODEC includes six low noise inputs -differential microphone . Line inputs have 30dB to -40dB logarithmic volume level adjustments with only 1 dB step adjustment. An electret microphone bias level is also available. All the required input filtering is contained within the device with no external components required.

The on-board stereo analogue to digital converter (ADC) is of a high quality using a multi-bit highorder oversampling architecture delivering optimum performance with low power consumption. The output from the ADC is available on the digital audio interface. The ADC includes an optional digital high pass filter to remove unwanted dc components from the audio signal.

The on-board digital to analogue converter (DAC) accepts digital audio from the digital audio interface. Digital filter de-emphasis at 32kHz, 44.1kHz and 48kHz can be applied to the digital data under software control. The DAC employs a high quality multi-bit high-order oversampling architecture to again deliver optimum performance with low power consumption.

The design of the CJC6808 has given much attention to power consumption without compromising performance. It includes the ability to power off selective parts of the circuitry under software control, thus conserving power. Nine separate power save modes be configured under software control including a standby and power off mode.

A sar adc is used to wake up the whole chip when detect the music signal coming in . The main MCU will judge the input music signal wave . CJC6808 have a PDN pin to put the whole

chip power down or in sleep mode .

Special techniques allow the audio to be muted and the device safely placed into standby, sections of the device powered off and volume levels adjusted without any audible clicks, pops or zipper noises. Therefore standby and power off modes maybe used dynamically under software control,whenever recording or playing is not required.

The device caters for a number of different sampling rates including industry standard 8kHz, 32kHz, 44.1kHz, 48kHz, 88.2kHz and 96kHz. Additionally, the device has an ADC and DAC that can operate at different sample rates.

There are two unique schemes featured within the programmable sample rates of the CJC6808: Normal industry standard 256/384fs sampling mode may be used, with the added ability to mix different sampling rates. The 12.288MHZ clock or 11.2896MHZ clock can be choose by control PLL. Thus, for example, the ADC can record to the DSP at 44.1kHz and be played back from the CODEC at 16kHz with no external digital signal processing required. The digital filters used at for both record and playback are optimised for each sampling rate used.

The digitised output is available in a number of audio data formats I2S, DSP Mode (a burst mode in which frame sync plus 2 data packed words are transmitted), MSB-First, left justified and MSB-First, right justified. The digital audio interface can operate in both master or slave modes.

The software control uses either 2 or 3-wire MPU interface.

A crystal oscillator is included on board the device. The device can generate the system master clock or alternatively it can accept an external master clock from the audio system.

AUDIO SIGNAL PATH

LINE INPUTS

The CJC6808 provides six channel line inputs . The inputs are high impedance and low capacitance, thus ideally suited to receiving line level signals from external hi-fi or audio equipment.

Both line inputs include independent programmable volume level adjustments and ADC input mute. The scheme is illustrated in Figure 10. Passive RF and active Anti-Alias filters are also incorporated within the line inputs. These prevent high frequencies aliasing into the audio band or otherwise degrading performance.

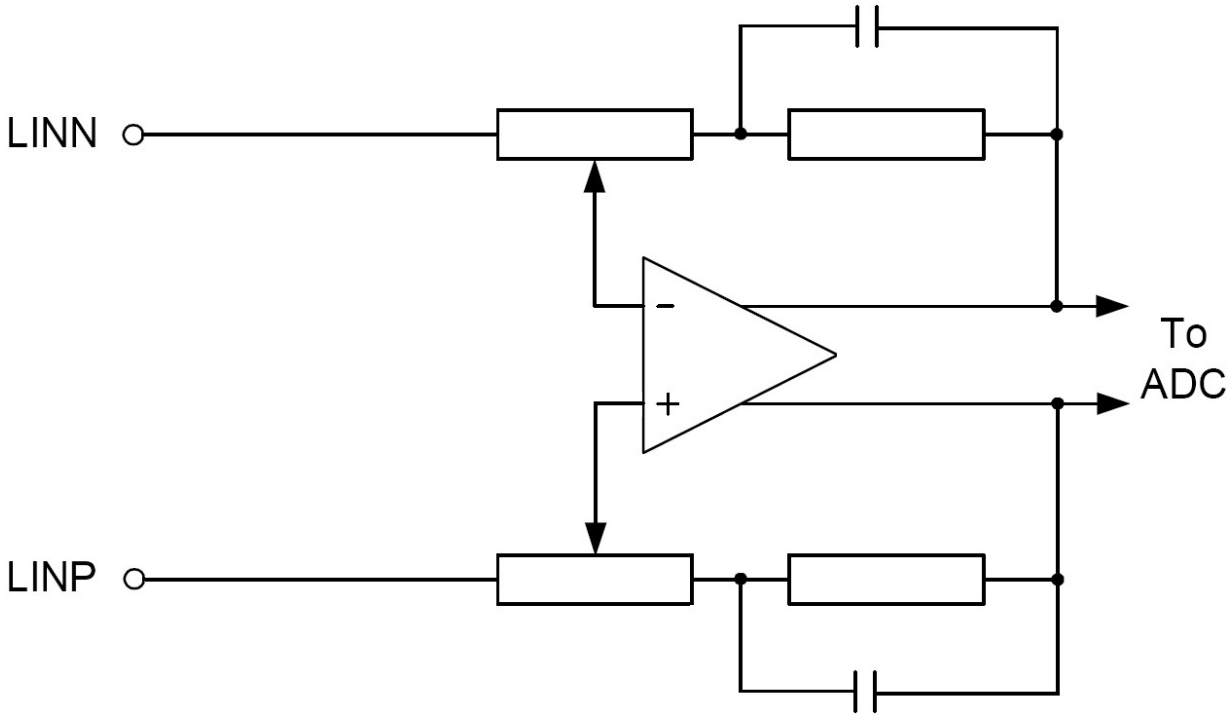


Figure 10 Line Input Schematic

The gain between the line inputs and the ADC is logarithmically adjustable has three gain range from 30dB to 0dB, 10dB to -20dB, -10 to -40dB in 1dB steps under software control. The ADC Full Scale input is 0.9VPP at AVDD = 3.3 volts. Any voltage greater than full scale will possibly overload the ADC and cause distortion. Note that the full scale input tracks directly with AVDD. The gain is independently adjustable on six Line Inputs. The line inputs to the ADC can be muted in the analogue domain under software control. The software control registers are shown Table 3. Note that the Line Input Mute only mutes the input to the ADC, this will still allow the Line Input signal to pass to the line output in Bypass Mode.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000000 Line In	1:0	RANG[1:0]	00	Gain range selection 00: -10dB~ -40dB 01: 10dB~ -20dB 10/11: 30dB~ 0dB
		ADJ<4:0>	00000 step=1dB	Line Input Volume Control 11111~00000: -10dB~ -40dB 11111~00000: 10dB~ -20dB 11111~00000: 30dB~ 0dB
	7	MUTE	1	Left Channel Line Input Mute to ADC 1 = Enable Mute 0 = Disable Mute
	8	EN_AAF	0	Line in enable signal 0: disable 1: enable

Table 3 Line Input Software Control

The line inputs are biased internally through the operational amplifier to VMID. Whenever the line inputs are muted or the device placed into standby mode, the line inputs are kept biased to VMID using special anti-thump circuitry. This reduces any audible clicks that may otherwise be heard when re-activating the inputs.

The external components required to complete the line input application is shown in the Figure 11.

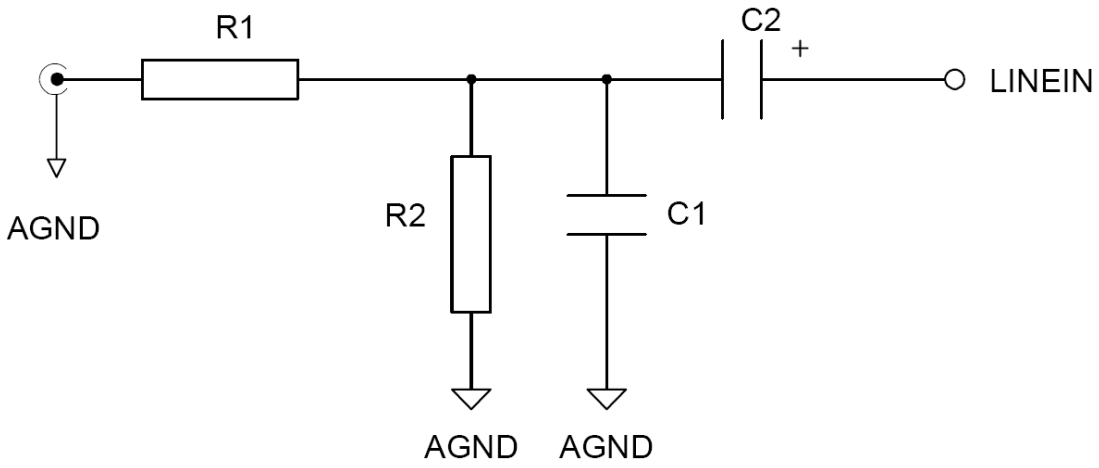


Figure 11 Line Input Application Drawing

For interfacing to a typical CD system, it is recommended that the input is scaled to ensure that there is no clipping of the signal. R1 = 5.6k, R2 = 5.6k, C1 = 220pF, C2 = 1μF.

R1 and R2 form a resistive divider to attenuate the 2 Vrms output from a CD player to a 1 Vrms level, so avoiding overloading the inputs. R2 also provides a discharge path for C2, thus preventing the input to C2 charging to an excessive voltage which may otherwise damage any equipment connected that is not suitably protected against high voltages. C1 forms an RF low pass filter for increasing the rejection of RF interference picked up on any cables. C2 forms a DC blocking capacitor to remove the DC path between the CJC6808 and the driving audio equipment. C2 together with the input impedance of the CJC6808 form a high pass filter.

MICROPHONE BIAS

The MICBIAS output provides a low noise reference voltage suitable for biasing electret type microphones and the associated external resistor biasing network. Refer to the Microphone Input section for an application drawing and further description.

The scheme for MICBIAS is shown in Figure 14. Note that there is a maximum source current capability of 3mA available for the MICBIAS. This limits the smallest value of external biasing resistors that can safely be used.

Note that the MICBIAS output is not active in standby mode.

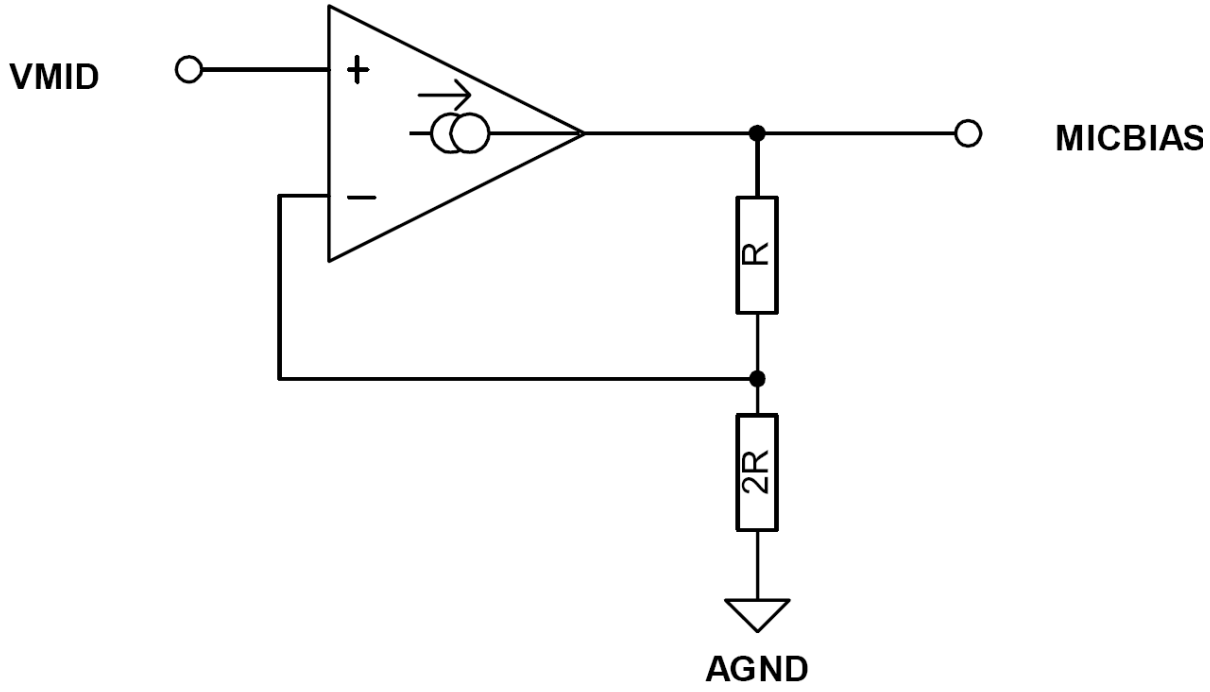


Figure 14 Microphone Bias Schematic

ADC

The CJC6808 uses a multi-bit oversampled sigma-delta ADC. A single channel of the ADC is illustrated in the Figure 15.

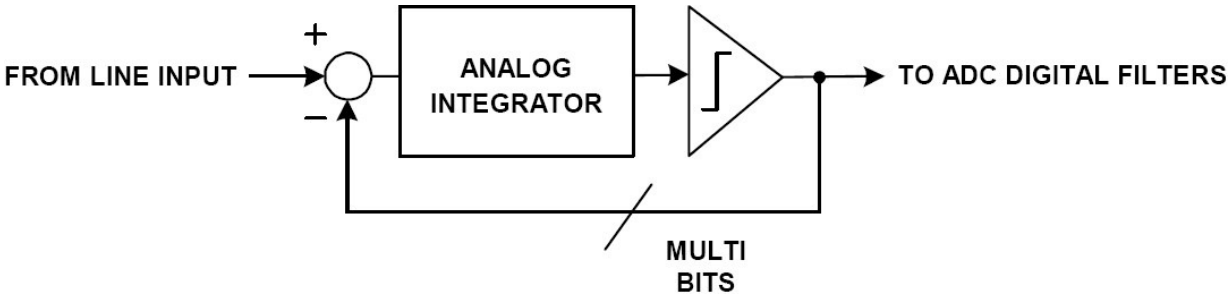


Figure 15 Multi-Bit Oversampling Sigma Delta ADC Schematic

The use of multi-bit feedback and high oversampling rates reduces the effects of jitter and high frequency noise.

The ADC Full Scale input is 0.9VPP at AVDD = 3.3 volts. Any voltage greater than full scale will possibly overload the ADC and cause distortion. Note that the full scale input tracks directly with AVDD.

The device employs 6 ADCs. The input can be selected from anyone Line Inputs under software control. The 6 channels cannot be selected independently.

ADC FILTERS

The ADC filters perform true 24 bit signal processing to convert the raw multi-bit oversampled data from the ADC to the correct sampling frequency to be output on the digital audio interface. Figure 16 illustrates the digital filter path.

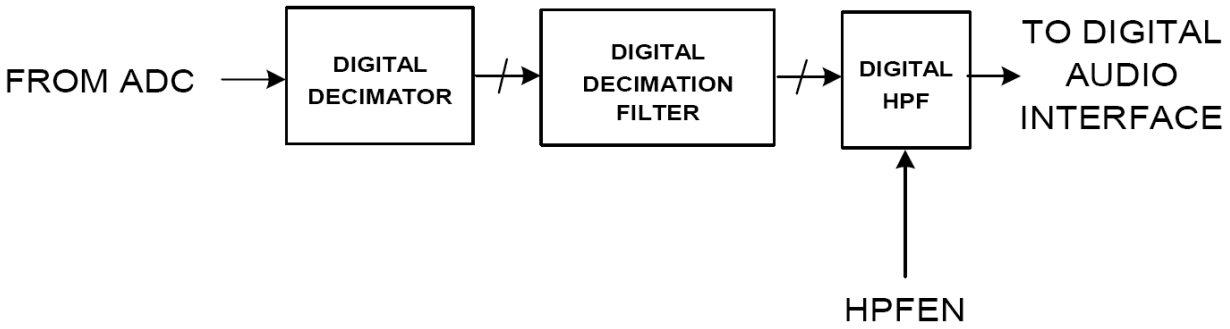


Figure 16 ADC Digital Filter

The ADC digital filters contain a digital high pass filter, selectable via software control. The high-pass filter response detailed in Digital Filter Characteristics. When the high-pass filter is enabled the dc offset is continuously calculated and subtracted from the input signal. By setting HPOR the last calculated dc offset value is stored when the high-pass filter is disabled and will continue to be subtracted from the input signal. If the dc offset changes, the stored and subtracted value will not change unless the high-pass filter is enabled. The software control is shown in Table 6.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000101 Digital Audio Path Control	0	ADCHPD	0	ADC High Pass Filter Enable (Digital) 1 = Disable High Pass Filter 0 = Enable High Pass Filter
	4	HPOR	0	Store dc offset when High Pass Filter disabled 1 = store offset 0 = clear offset

Table 6 ADC Software Control

There are several types of ADC filters, frequency and phase responses of these are shown in Digital Filter Characteristics. The filter types are automatically configured depending on the sample rate chosen. Refer to the sample rate section for more details.

DAC FILTERS

The DAC filters perform true 24 bit signal processing to convert the incoming digital audio data from the digital audio interface at the specified sample rate to multi-bit oversampled data for processing by the analogue DAC. Figure 17 illustrates the DAC digital filter path.

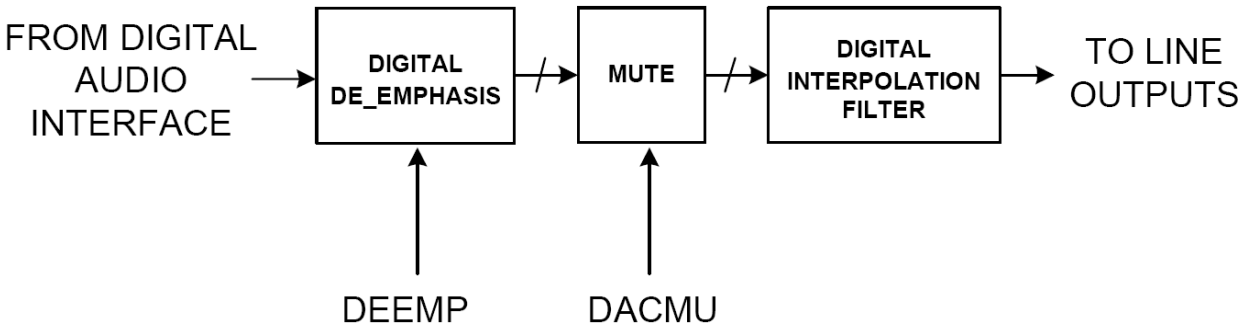


Figure 17 DAC Filter Schematic

The DAC digital filter can apply digital de-emphasis under software control, as shown in Table 7.The DAC can also perform a soft mute where the audio data is digitally brought to a mute level. This removes any abrupt step changes in the audio that might otherwise result in audible clicks in the audio outputs.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
000010001 Digital Audio Path Control	2:1	DEEMP[1:0]	00	De-emphasis Control (Digital) 11 = 48kHz 10 = 44.1kHz 01 = 32kHz 00 = Disable
	3	DACMU	1	DAC Soft Mute Control (Digital) 1 = Enable soft mute 0 = Disable soft mute

Table 7 DAC Software Control

DAC

The CJC6808 employs a multi-bit sigma delta oversampling digital to analogue converter. The scheme for the converter is illustrated in Figure 18.

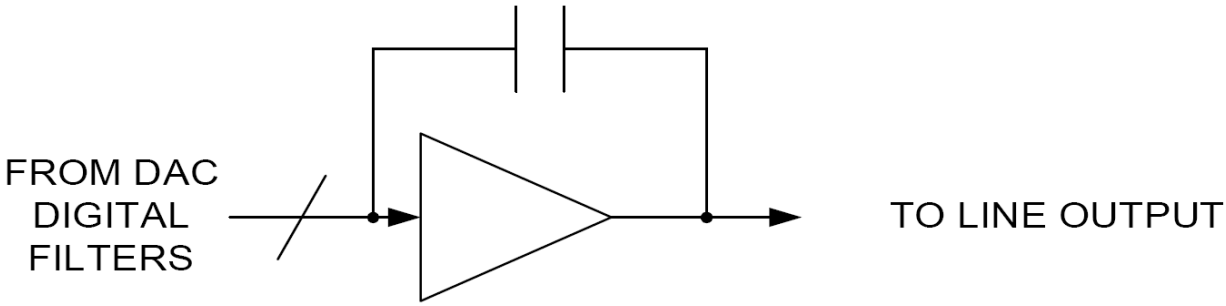


Figure 18 Multi-Bit Oversampling Sigma Delta Schematic

The DAC converts the multi-level digital audio data stream from the DAC digital filters into high quality analogue audio.

LINE OUTPUTS

The CJC6808 provides two low impedance line outputs LLINEOUT and RLINEOUT, suitable for driving typical line loads of impedance 10K and capacitance 50pF. The line output is used to selectively sum the outputs from the DAC or/and the Line inputs in bypass mode.

The LLINEOUT and RLINEOUT outputs are only available at a line output level and are not level adjustable in the analogue domain, having a fixed gain of 0dB. The level is fixed such that at the DAC full scale level the output level is VPP at AVDD = 3.3 volts. Note that the DAC full scale level tracks directly with AVDD. The scheme is shown in Figure 19. The line output includes a low order audio low pass filter for removing out-of band components from the sigma-delta DAC. Therefore no further external filtering is required in most applications.

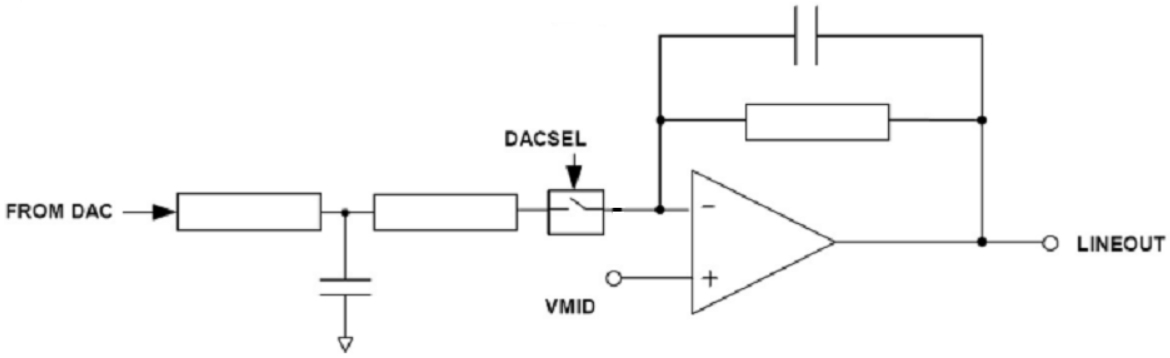


Figure 19 Line Output Schematic

The software control for the line outputs is shown in Table 8.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0010010 Analogue	3	DACPD	0	DAC RESET 1 = Enable DAC power down 0 = Disable DAC power down

Table 8 Output Software Control

The recommended external components are shown in Figure 20.

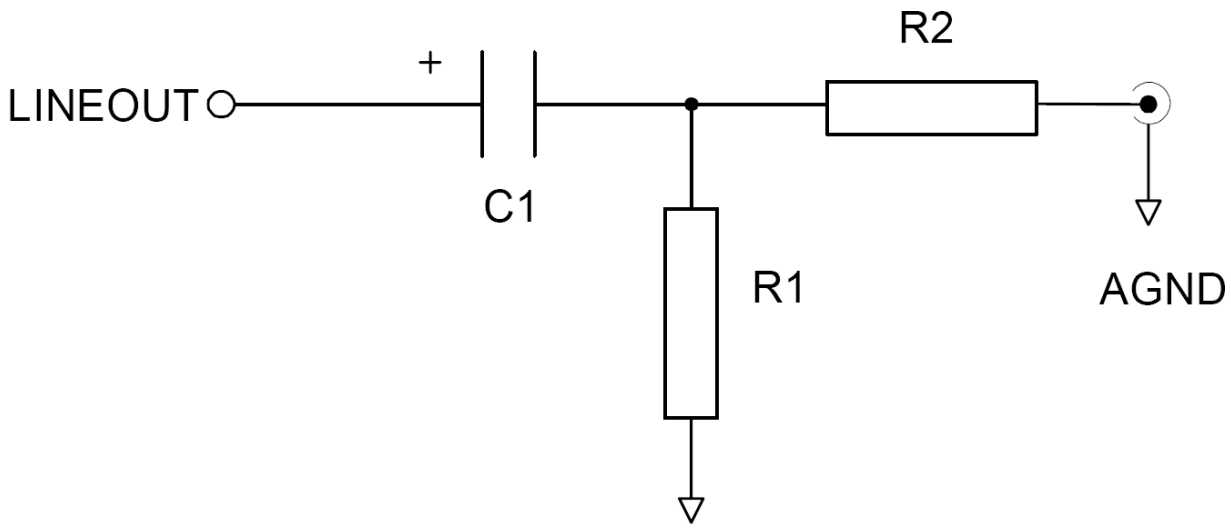


Figure 20 Line Outputs Application Drawing

Recommended values are C1 = 10μF, R1 = 47k, R2 = 100 Ω.

C1 forms a DC blocking capacitor to the line outputs. R1 prevents the output voltage from drifting so protecting equipment connected to the line output. R2 forms a de-coupling resistor preventing abnormal loads from disturbing the device. Note that poor choice of dielectric material for C1 can have dramatic effects on the measured signal distortion at the output

DEVICE OPERATION

DEVICE RESETTING and sleep mode

The CJC6808 contains a power on reset circuit that resets the internal state of the device to a known condition. The power on reset is applied as AVDD powers on and LDO output rise up. And the reset signal released only after the voltage level of DCVDD crosses a minimum turn off threshold. If DCVDD later falls below a minimum turn on threshold voltage then the power on reset is re-applied. The threshold voltages and associated hysteresis are shown in the Electrical Characteristics table.

A SAR adc is applied to detect the music signal . Four channels can be selected.

REGISTER ADDRESS	LABEL	DEFAULT	DESCRIPTION
0x1b 300 Sar channel select	SAR_ch3_EN	0	SARADC channel enable 1: Enable channel; 0: Disable channel
	SAR_ch2_EN	0	
	SAR_ch1_EN	0	
	SAR_ch0_EN	0	

ADC AUDIO INTERFACES

CJC6808 ADC may be operated in either one of the 8 offered audio interface modes. These are:

- Single chip I2S mode
- Single chip TDM mode
- CJC6808 cascaded with another CJC6808 in I2S mode
- CJC6808 cascaded with another CJC6808 in TDM mode
- CJC6808 cascaded with another codec chip in I2S mode
- CJC6808 cascaded with another codec chip in TDM mode
- CJC6808 cascaded with another codec chip and send 8 channel data in 6 channel time

All of these modes are MSB first and operate with data 16 bits, and all these modes have two justified mode: I2S mode and MSB mode.

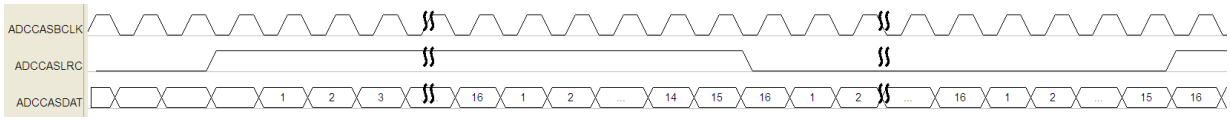
The ADC digital audio interface takes the data from the internal ADC digital filter and places it on the ADCDAT output. ADCDAT is the formatted digital audio data stream output from the ADC digital filters with several channels multiplexed together. ADCLRC is an alignment clock that controls channel data is present on the ADCDAT lines. ADCDAT and ADCLRC are synchronous with the BCLK signal with each data bit transition signified by a BCLK high to low transition. BCLK maybe an input or an output dependent on whether the device is in master or slave mode. Refer to the MASTER/SLAVE OPERATION section.

CJC6808 also presents an audio interface for cascaded with other chips. ADCCASLRC, ADCCASDAT and ADCCASBCLK are bidirectional signals. When chip is in slave cascaded mode, it send data through these ports to the master chip. When chip is in master cascaded mode, it receive data from other chip by these ports. When chip is cascaded with other chip, this audio interface can be set to master or slave mode, and data format can be set to I2S mode or Left justified mode when the slave chip is another type codec chip.

ADC CASCADE AUDIO INTERFACE

CJC6808 ADC can be cascaded with another chip with the cascade interface, if its ADC part is set as slave mode, it will send 6 channel data out, and if its ADC part is set as master mode, it will receive the data from another chip.

Slave mode:

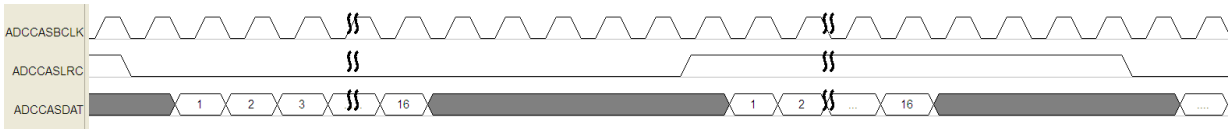


Slave cascaded transfer timing

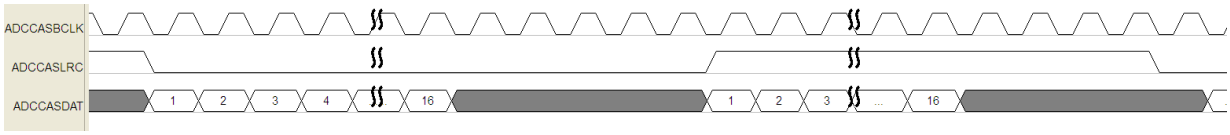
Send 6 channel data in one ADCCASLRC cycle. Every channel has 16 bits data and the justified mode is I2S mode. Although the ADC is slave mode, the cascade interface can be in master mode, that is, the ADCCASBCLK and ADCCASLRC are generated by the slave ADC chip.

Master mode:

If the cascaded chip is CJC6808, the timing is same to the slave mode. If the cascaded chip is other type codec chip, then two channel data will be transmitted and I2S or MSB type can be selected.



Cascaded I2S transfer timing

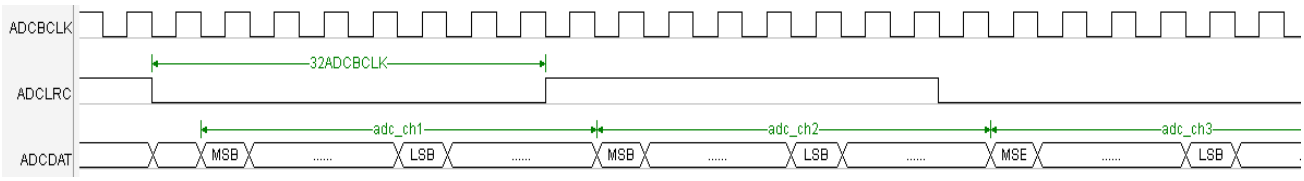


Cascaded MSB transfer timing

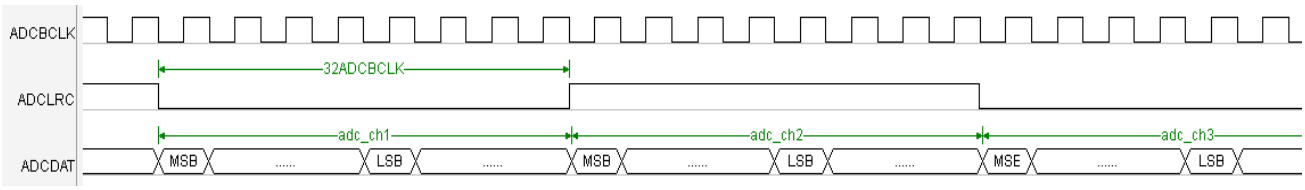
ADC OUTPUT AUDIO INTERFACE

ADC output audio interface send multi-channel ADC data in 16K or 32K sample rate. According to the cascaded mode, the output timing has several modes.

Single chip I2S mode will output six channel data. Although it is called I2S mode, the audio data justified mode has two type: I2S mode and MSB mode. The difference is the data start position.

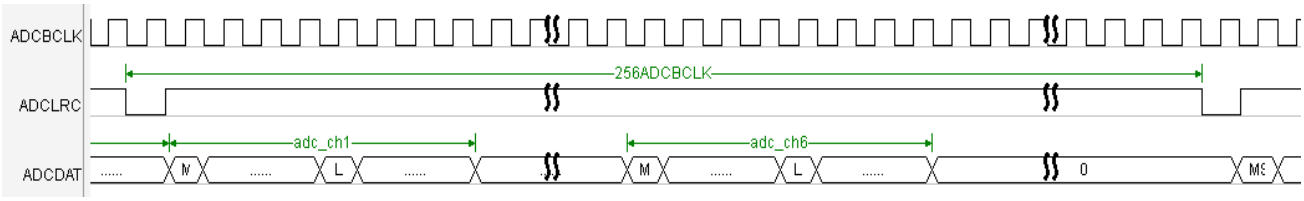


Single chip in I2S mode with I2S justified mode

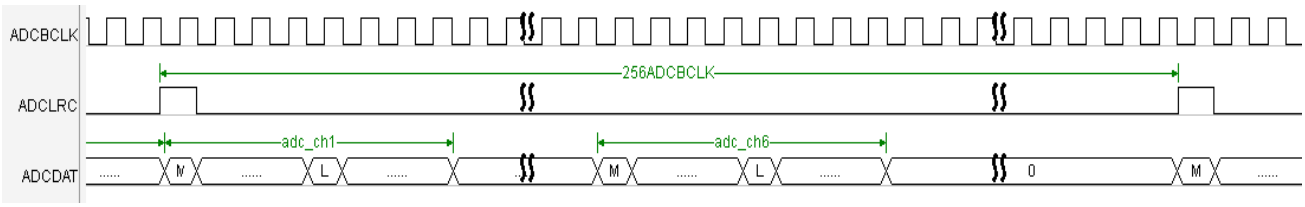


Single chip in I2S mode with MSB justified mode

Single chip TDM mode will output six channel data and two channel empty data.

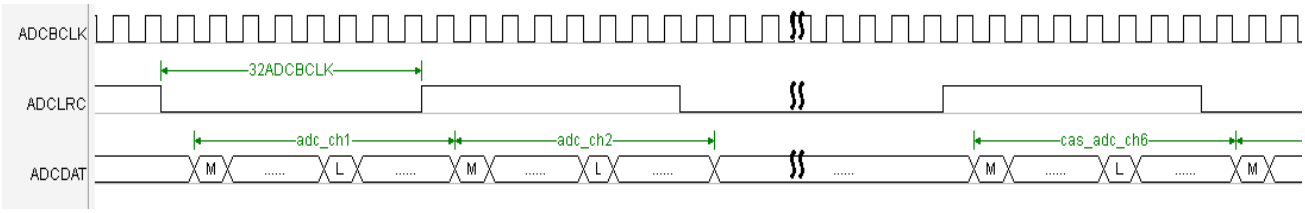


Single chip in TDM mode with I2S justified mode

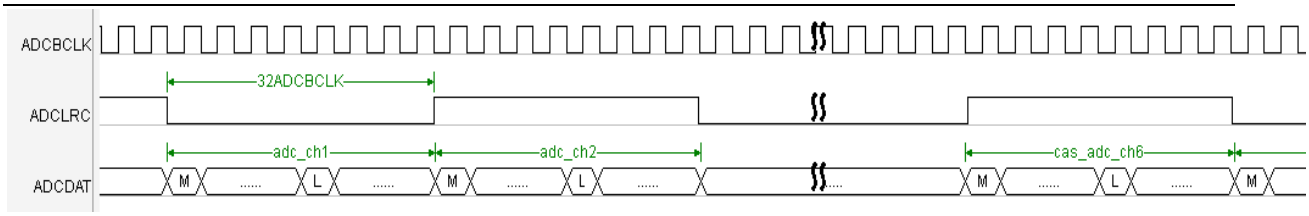


Single chip in TDM mode with MSB justified mode

CJC6808 cascaded with another CJC6808 will output 12 channel data in I2S mode.

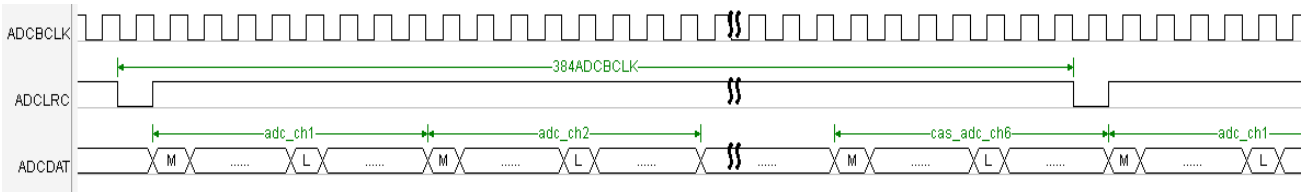


Cascaded with same chip in I2S mode with I2S justified

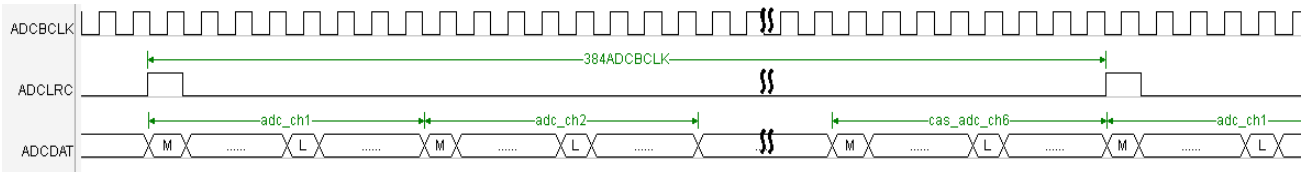


Cascaded with same chip in I2S mode with MSB justified

CJC6808 cascaded with another CJC6808 will output 12 channel data in TDM mode.

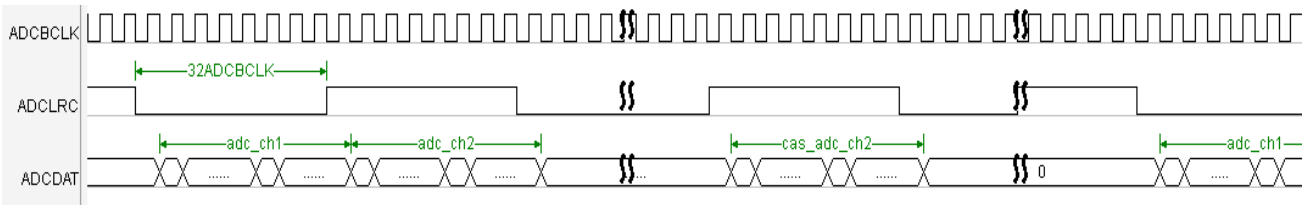


Cascaded with same chip in TDM mode with I2S justified

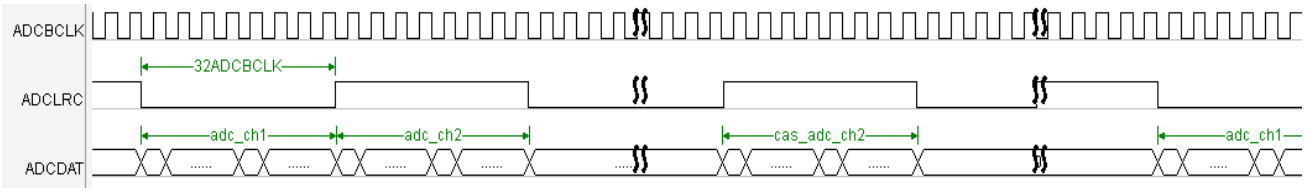


Cascaded with same chip in TDM mode with MSB justified

CJC6808 cascaded with a codec chip output 12 channel data in I2S mode. The last four channel data are empty.

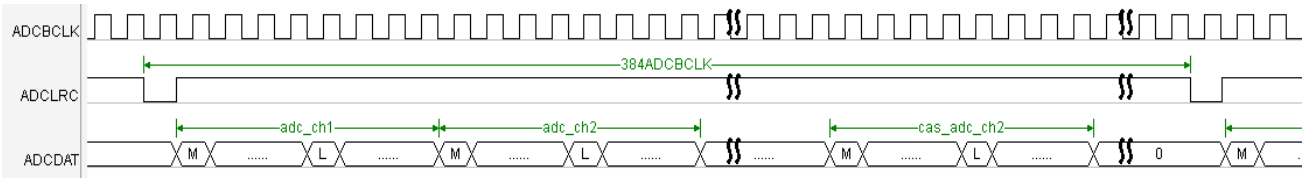


Cascaded with other chip in I2S mode with I2S justified

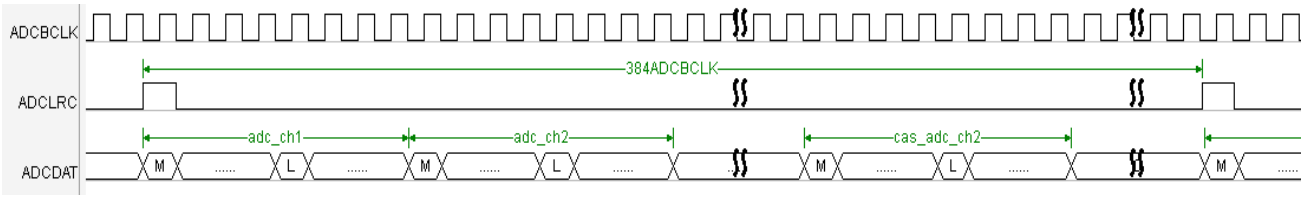


Cascaded with other chip in I2S mode with MSB justified

CJC6808 cascaded with a codec chip output 12 channel data in TDM mode.

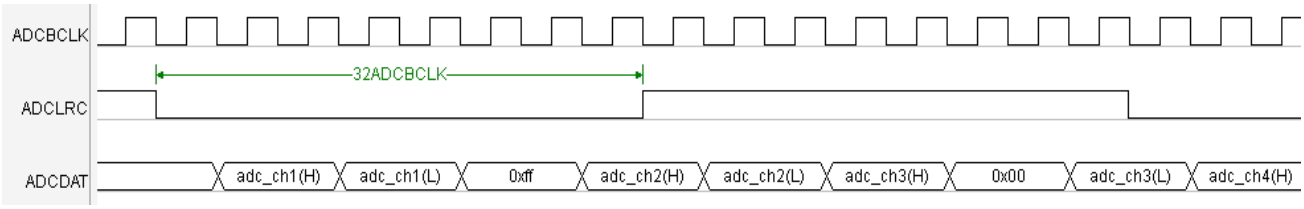


Cascaded with other chip in TDM mode with I2S justified

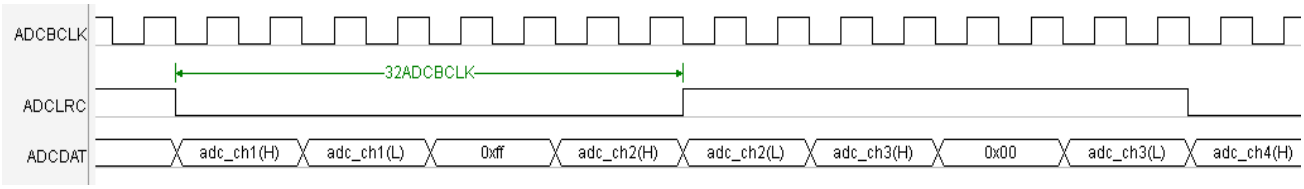


Cascaded with other chip in TDM mode with MSB justified

CJC6808 cascaded with another codec chip and send 8 channel data in 6 channel time. This is a compress mode.



Cascaded with other chip in compressed mode with I2S justified



Cascaded with other chip in compressed mode with MSB justified

ADC MASTER AND SLAVE MODE OPERATION

Cascaded interface and ADC data output interface are both can be set to slave or master, although the ADC is slave or master. Figure 3 and Figure 5 show the interface direction of master and slave mode.

ADC AUDIO DATA SAMPLING RATES

The user controls the ADC sample rate by using an appropriate MCLK or crystal frequency and the sample rate control register setting. The CJC6808 ADC can support sample rates of 16K and 32K.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0001101 ADC sample rate	5	ADC_SR	0	1: ADC sample rate is 32k.(Note 1) 0: ADC sample rate is 16k

Table 17 ADC Sample Rate Control

Note 1: Here the sample rate is one channel sample rate. Every channel in the six channels is 32K.

DAC AUDIO INTERFACES

CJC6808 DAC may be operated in either one of the 3 offered audio interface modes. These are:

• Right justified
• Left justified
• I2S

All three of these modes are MSB first and operate with data 16 to 32 bits. Note that 32 bit data is not supported in right justified mode.

The DAC digital audio interface receives the digital audio data for the internal DAC digital filters on the DACDAT input. DACDAT is the formatted digital audio data stream output to the DAC digital filters with left and right channels multiplexed together. DACLRC is an alignment clock that controls whether Left or Right channel data is present on DACDAT. DACDAT and DACLRC are synchronous with the BCLK signal with each data bit transition signified by a BCLK high to low transition. DACDAT is always an input. DACBCLK and DACLRC are either outputs or inputs depending whether the DAC ports are in master or slave mode. Refer to the MASTER/SLAVE OPERATION section

There are three digital audio interface formats accommodated by the CJC6808 DAC part. These are shown in the figures below. Refer to the Electrical Characteristic section for timing information.

Left Justified mode is where the MSB is available on the first rising edge of BCLK following a ADCLR or DACLRC transition.

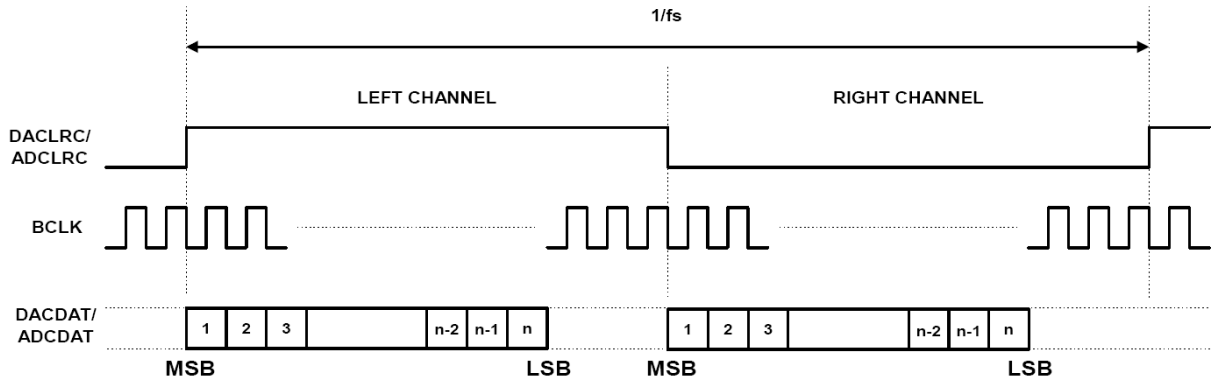


Figure 26 Left Justified Mode

I2S mode is where the MSB is available on the 2nd rising edge of BCLK following a DACLRC or ADCLRC transition.

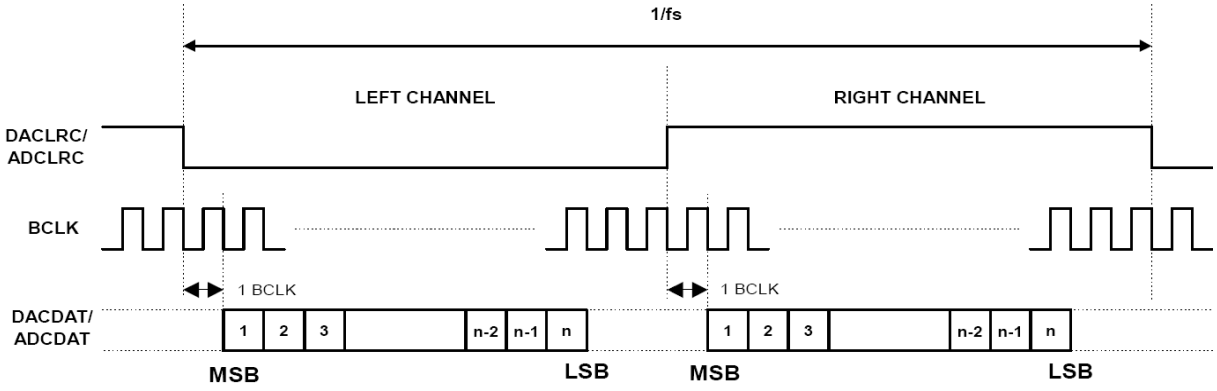


Figure 27 I2S Mode

Right Justified mode is where the LSB is available on the rising edge of BCLK preceding a DACLRC or ADCLRC transition, yet MSB is still transmitted first.

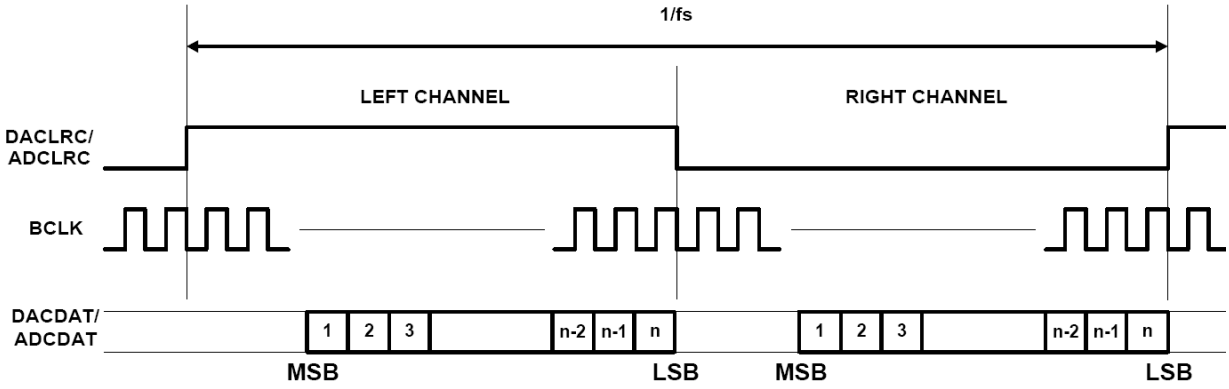


Figure 28 Right Justified Mode

The DAC digital audio interface modes are software configurable. Note that dynamically changing the software format may result in erroneous operation of the interfaces and is therefore not recommended.

The length of the DAC audio data is programmable at 16/20/24 or 32 bits, in I2S or left justified modes only. Refer to the software control table below. The data is signed 2's complement. Both ADC and DAC are fixed at the same data length. The ADC and DAC digital filters process data using 24 bits. If the ADC is programmed to output 16 or 20 bit data then it strips the LSBs from the 24 bit data. If the ADC is programmed to output 32 bits then it packs the LSBs with zeros. If the DAC is programmed to receive 16 or 20 bit data, the CJC6808 packs the LSBs with zeros. If the DAC is programmed to receive 32 bit data, then it strips the LSBs.

DACDAT is always an input. It is expected to be set low by the audio interface controller when the CJC6808

is powered off or in standby.

ADCLRC, DACLRC, ADCBCLK and DACBCLK can be either outputs or inputs depending on whether the corresponding device parts interface are configured as master or slave mode. If the device is a master then the signals are outputs that default low. If the device is a slave then the signals are inputs. It is expected that these are set low by the audio interface controller when the CJC6808 is powered off or in standby.

ADCDAT lines are always outputs. They power up and return from standby low.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0010011 DAC Audio Interface Format	1:0	DAC_FORMAT[1:0]	10	DAC Audio Data Format Select 00: Right justified 01: Left justified 10: IIS format 11: Reserved
	3:2	DAC_IWL[1:0]	10	Input Audio Data Bit Length Select 11 = 32 bits 10 = 24 bits 01 = 20 bits 00 = 16 bits
	4	DAC_MCLK_SEL	0	DAC master clock selection. 1: 11.2892 from PLL; 0: 12.288 from OSC
	5	DAC_MS	0	DAC Master Slave Mode Control 1 = Enable Master Mode 0 = Enable Slave Mode

Table 15 DAC Audio Interface Control

Note: If right justified 32 bit mode is selected then the CJC6808 defaults to 24 bits.

DAC MASTER AND SLAVE MODE OPERATION

The CJC6808 DAC can be configured as either a master or slave mode device. As a master mode device the CJC6808 controls sequencing of the data and clocks on the DAC audio interface. As a slave device the CJC6808 responds with data to the clocks it receives over the digital audio interface. The mode is set with the DAC_MS bit of the control register as shown in Table 16.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0010011 DAC Audio Interface Format	5	DAC_MS	0	DAC Master Slave Mode Control 1 = Enable Master Mode 0 = Enable Slave Mode

Table 16 Programming Master/Slave Modes

As a master mode device the CJC6808 controls the sequencing of data transfer (DACDAT) and output of clocks (DACBCLK, DACLRC) over the digital audio interface. It uses the timing generated from either its on-board crystal or the MCLK input as the reference for the clock and data transitions. This is illustrated in Figure 31. DACDAT is always an input to the CJC6808 independent of master or slave mode.

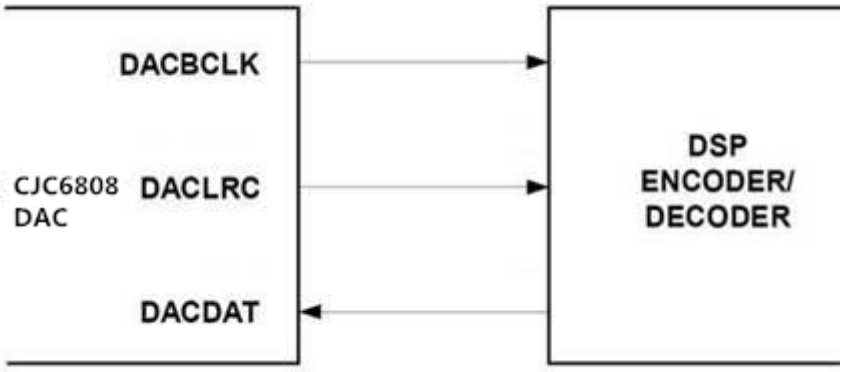


Figure 31 DAC Master Mode

As a slave device the CJC6808 sequences the data transfer (ADCDAT, DACDAT) over the digital audio interface in response to the external applied clocks (BCLK, ADCLRC, DACLRC). This is illustrated in Figure 32.

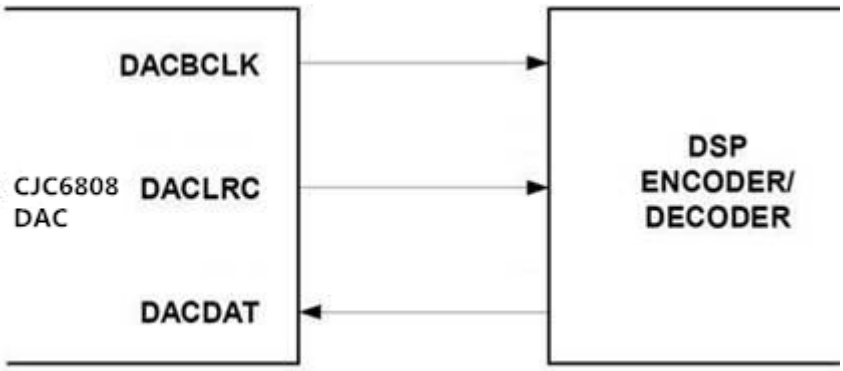


Figure 32 DAC Slave Mode

Note that the CJC6808 relies on controlled phase relationships between audio interface DACBCLK, DACLRC and the master MCLK or CLKOUT. To avoid any timing hazards, refer to the timing section for detailed information.

DAC AUDIO DATA SAMPLING RATES

The user controls the DAC sample rate by using an appropriate MCLK or crystal frequency and the sample rate control register setting. The CJC6808 DAC can support sample rates from 8ks/s up to 96ks/s.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0010100 DAC Sampling Control	5:2	DAC_SR[3:0]	0000	DAC sample rate selection. 000: 48k 001: 8k 010: 32k 011: 96k 100: 44.1k 101: 88.2k

Table 17 Sample Rate Control

DAC SAMPLE RATES

MCLK/crystal oscillator is set up according to the desired sample rates of t DAC. For sampling rates of 8, 32, 48 or 96kHz, MCLK frequencies of either 12.288MHz (256fs) is used. For DAC sampling rates of 8, 44.1 or 88.2kHz from MCLK frequencies of either 11.2896MHz (256fs) can be used.

Table 18 should be used to set up the device to work with the various sample rate combinations. For example if the user wishes to use the CJC6808 in normal mode with the ADC and DAC sample rates at 48kHz and 48kHz respectively then the device should be programmed with BOSR = 0, SR3 = 0, SR2 = 0, SR1 = 0 and SR0 = 0 with a 12.288MHz MCLK or with BOSR = 1, SR3 = 0, SR2 = 0, SR1 = 0 and SR0 = 0 with a 18.432MHz MCLK. The ADC and DAC will then operate with a Digital Filter of type 1, refer to Digital Filter Characteristics section for an explanation of the different filter types.

SAMPLING RATE	MCLK FREQUENCY	SAMPLE RATE REGISTER SETTINGS				DIGITAL FILTER TYPE
KHz	MHz	BOSR	DAC_SR[2:0]			
48	12.288	0 (256fs)	0	0	0	1
8	12.288	0 (256fs)	0	0	1	1
32	12.288	0 (256fs)	0	1	0	1

96	12.288	0 (128fs)	0	1	1	2
44.1	11.2896	0 (256fs)	1	0	0	1
88.2	11.2896	0 (128fs)	1	0	1	2

Table 18 DAC Sample Rate Look-up Table

The table above can be used to set up the DAC device to work with various sample rate combinations.

ACTIVATING DSP AND DIGITAL AUDIO INTERFACE

To prevent any communication problems from arising across the Digital Audio Interface the Audio Interface is disabled (tristate with weak 100k pulldown). Once the Audio Interface and the Sampling Control has been programmed it is activated by setting the ACTIVE bit under Software Control.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0001001 Active Control	0	ACTIVE	0	Activate Interface 1 = Active 0 = Inactive

Table 23 Activating DSP and Digital Audio Interface

It is recommended that between changing any content of Digital Audio Interface or Sampling Control Register that the active bit is reset then set.

SOFTWARE CONTROL INTERFACE

The software control interface may be operated using either a 3-wire (SPI-compatible) or 2-wire MPU interface. Selection of interface format is achieved by setting the state of the MODE pin.

In 3-wire mode, SDIN is used for the program data, SCLK is used to clock in the program data and CSB is used to latch in the program data. In 2-wire mode, SDIN is used for serial data and SCLK is used for the serial clock. In 2-wire mode, the state of CSB pin allows the user to select one of two addresses.

SELECTION OF SERIAL CONTROL MODE

The serial control interface may be selected to operate in either 2 or 3-wire modes. This is achieved by setting the state of the MODE pin.

MODE	INTERFACE

	FORMAT
0	2 wire
1	3 wire

Table 24 Control Interface Mode Selection

3-WIRE (SPI COMPATIBLE) SERIAL CONTROL MODE

The CJC6808 can be controlled using a 3-wire serial interface. SDIN is used for the program data, SCLK is used to clock in the program data and CSB is use to latch in the program data. The 3-wire interface protocol is shown in Figure 33.

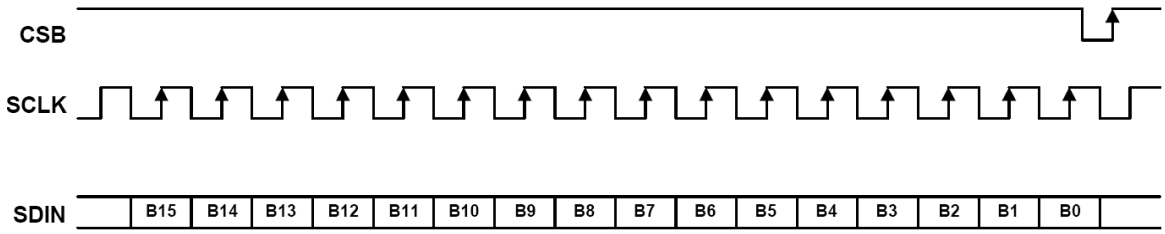


Figure 33 3-Wire Serial Interface

Notes:

1. B[15:9] are Control Address Bits
2. B[8:0] are Control Data Bits
3. CSB is edge sensitive not level sensitive. The data is latched on the rising edge of CSB.

2-WIRE SERIAL CONTROL MODE

The CJC6808 supports a 2-wire MPU serial interface. The device operates as a slave device only. The CJC6808 has one of two slave addresses that are selected by setting the state of pin 15, (CSB).

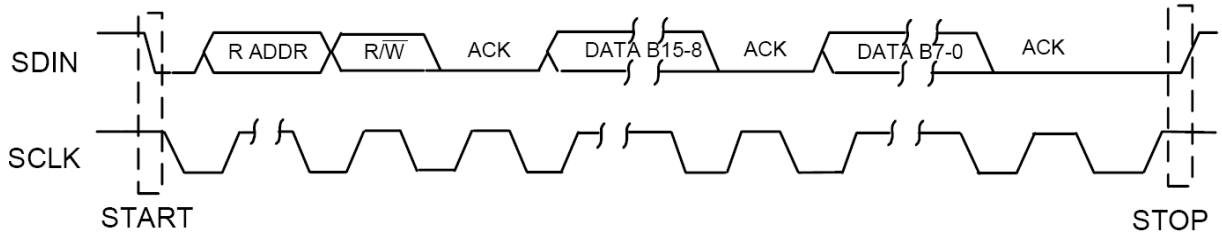


Figure 34 2-Wire Serial Interface

Notes:

1. B[15:9] are Control Address Bits
2. B[8:0] are Control Data Bits

CSB STATE	ADDRESS
0	0011010
1	0011011

Table 25 2-Wire MPU Interface Address Selection

To control the CJC6808 on the 2-wire bus the master control device must initiate a data transfer by establishing a start condition, defined by a high to low transition on SDIN while SCLK remains high. This indicates that an address and data transfer will follow. All peripherals on the 2-wire bus respond to the start condition and shift in the next eight bits (7-bit address + R/W bit). The transfer is MSB first. The 7-bit address consists of a 6-bit base address + a single programmable bit to select one of two available addresses for this device (see table 24). If the correct address is received and the R/W bit is '0', indicating a write, then the CJC6808 will respond by pulling SDIN low on the next clock pulse (ACK). The CJC6808 is a write only device and will only respond to the R/W bit indicating a write. If the address is not recognised the device will return to the idle condition and wait for a new start condition and valid address.

Once the CJC6808 has acknowledged a correct address, the controller will send eight data bits (bits B15-B8). CJC6808 will then acknowledge the sent data by pulling SDIN low for one clock pulse. The controller will then send the remaining eight data bits (bits B7-B0) and the CJC6808 will then acknowledge again by pulling SDIN low.

A stop condition is defined when there is a low to high transition on SDIN while SCLK is high. If a start or stop condition is detected out of sequence at any point in the data transfer then the device will jump to the idle condition.

After receiving a complete address and data sequence the CJC6808 returns to the idle state and waits for another start condition. Each write to a register requires the complete sequence of start condition, device address and R/W bit followed by the 16 register address and data bits.

POWER DOWN MODES

The CJC6808 contains power conservation modes in which various circuit blocks may be safely powered down in order to conserve power. This is software programmable as shown in the table below.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0010010 Power control	5	POWEROFF	1	Poweroff mode 1: Enable POWEROFF 0: Disable POWEROFF
	4	OUTPD	1	Outputs Power Down 1: Enable power down 0: Disable Power down
	3	DACPD	1	DAC Power Down 1: Enable power down 0: Disable Power down
	2	ADCPD	1	ADC Power Down 1: Enable power down 0: Disable Power down
	1	ADC_CAS_PD	1	ADC cascade part power down 1: Enable power down 0: Disable Power down
	0	ADC_AIF_PD	1	ADC Digital audio interface power down 1: Enable power down 0: Disable Power down

Table 26 Power Conservation Modes Software Control

The power down control can be used to either a) permanently disable functions when not required in certain applications or b) to dynamically power up and down functions depending on the operating mode, e.g.: during playback or record. Please follow the special instructions below if dynamic implementations are being used.

ADCPD: Powers down the ADC and ADC Filters. If this is done dynamically then audible pops will result if any signals were present through the ADC. To overcome this whenever the ADC is to be powered down, either mute the Microphone Input (MUTEIN) or MUTELINEIN, then change ADCPD. This is of use when the device enters Playback, Pause or Stop modes regardless of whether Microphone or Line Inputs are selected.

DACPD: Powers down the DAC and DAC Digital Filters. If this is done dynamically then audible pops will result unless the following guidelines are followed. In order to prevent pops, the DAC should first be soft-muted (DACMU), the output should then be de-selected from the line and headphone output (DACSEL), then the DAC powered down (DACPD). This is of use when the device enters Record, Pause, Stop or Bypass modes.

OUTPD: Powers down the Line and Headphone outputs. If this is done dynamically then audible pops may result unless the DAC is first soft-muted (DACMU). This is of use when the device enters Record, Pause or Stop modes.

ADC_CAS_PD: Powers off the ADC.

ADC_AIF_PD: Powers down the ADC interface.

REGISTER MAP

The complete register map is shown in Table 29. The detailed description can be found in Table 30 and in the relevant text of the device description. There are 11 registers with 16 bits per register (7 bit address + 9 bits of data). These can be controlled using either the 2 wire or 3 wire MPU interface.

Register	Bit	LABEL	Default	Description
0x00 L1_VOL_CTRL	8	L1IVU	0	Line1 input volume control
	7	L1INMUTE	0	Channel 1 input mute to ADC 1: Enable mute; 0: Disable mute
	6	L1ZCEN	1	Channel 1 zero cross detector 1: Change gain on zero cross only 0: Change gain immediately

	5	***Reserved***		
	[4:0]	L1INVOL	111	Channel 1 input volume control. 11111: +12dB -1.5dB per step 00000: -34.5dB
0x01 L2_VOL_CTRL	8	L2IVU	0	Line2 input volume control
	7	L2INMUTE	0	Channel 2 input mute to ADC 1: Enable mute; 0: Disable mute
	6	L2ZCEN	1	Channel 2 zero cross detector 1: Change gain on zero cross only 0: Change gain immediately
	5	***Reserved***		
	[4:0]	L2INVOL	111	Channel 2 input volume control.
0x02 L3_VOL_CTRL	8	L3IVU	0	Line3 input volume control
	7	L3INMUTE	0	Channel 3 input mute to ADC 1: Enable mute; 0: Disable mute
	6	L3ZCEN	1	Channel 3 zero cross detector 1: Change gain on zero cross only 0: Change gain immediately
	5	***Reserved***		
	[4:0]	L3INVOL	111	Channel 3 input volume control.
0x03 L4_VOL_CTRL	8	L4IVU	0	Line 4 input volume control
	7	L4INMUTE	0	Channel 4 input mute to ADC 1: Enable mute; 0: Disable mute
	6	L4ZCEN	1	Channel 4 zero cross detector 1: Change gain on zero cross only 0: Change gain immediately
	5	***Reserved***		
	[4:0]	L4INVOL	111	Channel 4 input volume control.
0x04 L5_VOL_CTRL	8	L5IVU	0	Line 5 input volume control
	7	L5INMUTE	0	Channel 5 input mute to ADC 1: Enable mute; 0: Disable mute
	6	L5ZCEN	1	Channel 5 zero cross detector 1: Change gain on zero cross only 0: Change gain immediately
	5	***Reserved***		
	[4:0]	L5INVOL	111	Channel 5 input volume control.
0x05 L6_VOL_CTRL	8	L6IVU	0	Line 6 input volume control
	7	L6INMUTE	0	Channel 6 input mute to ADC 1: Enable mute; 0: Disable mute
	6	L6ZCEN	1	Channel 6 zero cross detector 1: Change gain on zero cross only 0: Change gain immediately

	5	***Reserved***		
	[4:0]	L6INVOL	111	Channel 6 input volume control.
0x06 LINE1_CTRL	7	L1_RST_MODU	0	ADC1 RESET, low active
	[6:5]	L1_RANG	0	LINE1 gain range
	4	L1_MUTE_AAF	0	AGC/AAF mute, 1: Enable mute;0: Disable mute
	3	L1_EN_MODU	0	ADC1 Enable; 1: Enable ; 0: disable
	2	L1_EN_CMP	0	AGC/AFF zero cross comparator enable
	1	L1_EN_ADC_CLK	0	ADC1 clock enable
	0	L1_EN_AAF	0	AGC/AFF zero cross comparator enable
0x07 LINE2_CTRL	7	L2_RST_MODU	0	ADC2 RESET, low active
	[6:5]	L2_RANG	0	LINE2 gain range
	4	L2_MUTE_AAF	0	AGC/AAF mute, 1: Enable mute;0: Disable mute
	3	L2_EN_MODU	0	ADC2 Enable; 1: Enable ; 0: disable
	2	L2_EN_CMP	0	AGC/AFF zero cross comparator enable
	1	L2_EN_ADC_CLK	0	ADC2 clock enable
	0	L2_EN_AAF	0	AGC/AFF zero cross comparator enable
0x08 LINE3_CTRL	7	L3_RST_MODU	0	ADC3 RESET, low active
	[6:5]	L3_RANG	0	LINE3 gain range
	4	L3_MUTE_AAF	0	AGC/AAF mute, 1: Enable mute;0: Disable mute
	3	L3_EN_MODU	0	ADC3 Enable; 1: Enable ; 0: disable
	2	L3_EN_CMP	0	AGC/AFF zero cross comparator enable
	1	L3_EN_ADC_CLK	0	ADC3 clock enable
	0	L3_EN_AAF	0	AGC/AFF zero cross comparator enable
0x09 LINE4_CTRL	7	L4_RST_MODU	0	ADC4 RESET, low active
	[6:5]	L4_RANG	0	LINE4 gain range
	4	L4_MUTE_AAF	0	AGC/AAF mute, 1: Enable mute;0: Disable mute
	3	L4_EN_MODU	0	ADC4 Enable; 1: Enable ; 0: disable
	2	L4_EN_CMP	0	AGC/AFF zero cross comparator enable
	1	L4_EN_ADC_CLK	0	ADC4 clock enable
	0	L4_EN_AAF	0	AGC/AFF zero cross comparator enable
0x0a LINE5_CTRL	7	L5_RST_MODU	0	ADC5 RESET, low active
	[6:5]	L5_RANG	0	LINE5 gain range
	4	L5_MUTE_AAF	0	AGC/AAF mute, 1: Enable mute;0: Disable mute
	3	L5_EN_MODU	0	ADC5 Enable; 1: Enable ; 0: disable
	2	L5_EN_CMP	0	AGC/AFF zero cross comparator enable
	1	L5_EN_ADC_CLK	0	ADC5 clock enable
	0	L5_EN_AAF	0	AGC/AFF zero cross comparator enable
0x0b LINE6_CTRL	7	L6_RST_MODU	0	ADC6 RESET, low active
	[6:5]	L6_RANG	0	LINE6 gain range
	4	L6_MUTE_AAF	0	AGC/AAF mute, 1: Enable mute;0: Disable mute
	3	L6_EN_MODU	0	ADC6 Enable; 1: Enable ; 0: disable
	2	L6_EN_CMP	0	AGC/AFF zero cross comparator enable
	1	L6_EN_ADC_CLK	0	ADC6 clock enable

	0	L6_EN_AAF	0	AGC/AFF zero cross comparator enable
0x0c MICB_CTRL	[8:3]	***Reserved***	0	Control microphone enable
	2	EN_MICB3	0	
	1	EN_MICB2	0	
	0	EN_MICB1	0	
0x0d ADC TDM interface mode	[8:6]	***Reserved***		
	5	ADC_SR	0	ADC sample rate control. 0:16K； 1:32K
	4	ADC_TDM_FMT	0	TDM port data justified format 0:MSB; 1:IIS
	3	ADC_TDM_MS	0	1: TMD master mode; 0: TDM slave mode
	[2:0]	ADC_TDM_MODE	0	ADC master mode TDM interface mode select: 0: Single chip I2S mode， 6 channel data 1: Single chip TDM mode，8 channel with 6 channel data. 2: Same chip cascaded together and I2S mode 3: Same chip cascaded together and TDM mode 4: Cascaded with one codec chip with I2S mode，12 channel data output. 5: Cascaded with one codec chip with TDM mode，12 channel data output. 6: Cascaded with one codec chip and output 8 channel data in sequence
0x0e ADC cascade mode	[8:5]	***Reserved***		
	4	ADC_CAS_INF_ACTIVE	0	ADC cascaded interface enable 1：Enable；0：Disable
	3	ADC_CAS_INF_MS	0	ADC cascade interface mode select： 1: Master 0: Slave
	2	ADC_CAS_MS	0	ADC cascade master or slave mode select： 1： master mode, receive another chip ADC data 0：slave mode, send ADC data to another chip
	[1:0]	ADC_CAS_FMT	0	Cascade interface mode select： 2’b00: IIS; 2’b01: left justified; 2’b10: With another CJC6808 2’b11: Single chip output When slave mode, the setting is not cared.
0x11 DAC path control	[8:6]	***Reserved***		
	5	BYPAS		ADC Bypass
	4	HPOR		Store dc offset when High Pass Filter disabled 1: store offset; 0: clear offset
	3	DACMU	1	DAC soft mute control

				1: Enable soft mute 0: disable soft mute
	[2:1]	DEEMP	0	De-emphasis control 11: 48kHz; 10: 44.1kHz; 01: 32kHz; 00: Disable
	0	ADCHPD	0	ADC High Pass Filter Enable 1: Disable High Pass Filter 0: Enable High Pass filter
0x12 Power control	[8:6]	***Reserved***		
	5	POWEROFF	1	Poweroff mode 1: Enable POWEROFF 0: Disable POWEROFF
	4	OUTPD	1	Outputs Power Down 1: Enable power down 0: Disable Power down
	3	DACPD	1	DAC Power Down 1: Enable power down 0: Disable Power down
	2	ADCPD	1	ADC Power Down 1: Enable power down 0: Disable Power down
	1	ADC_CAS_PD	1	ADC cascade part power down 1: Enable power down 0: Disable Power down
	0	ADC_AIF_PD	1	ADC Digital audio interface power down 1: Enable power down 0: Disable Power down
0x13 Dac interface format	[8:6]	***Reserved***		
	5	DAC_MS	0	DAC master/slave mode control 1: Enable master mode; 0: Enable slave mode
	4	DAC_MCLK_SEL	0	DAC master clock select 1: 11.2892 from PLL; 0: 12.288 from OSC
	[3:2]	DAC_IWL	10	DAC Audio data width 00: 16 bits; 01: 20 bits; 10: 24 bits; 11: 32 bits;
	[1:0]	DAC_FORMAT	10	00: Right justified 01: Left justified 10: IIS format 11: Reserved
0x14 DAC sample control 1	[8:3]	***Reserved***		
	[2:0]	DAC_SR	0	DAC sample rate selection. 000: 48k 001: 8k 010: 32k

				011: 96k 100: 44.1k 101: 88.2k
0x15 DAC interface active control	[8:1]	***Reserved***		
	0	DAC_ACTIVE	0	DAC interface active control 1: active; 0: not active
0x16 ADC ALC Control 1	[8:6]	***Reserved***		
	5	L6_ALC_EN	0	ADC ALC control 1: ALC enable; 0: ALC disabled;
	4	L5_ALC_EN	0	
	3	L4_ALC_EN	0	
	2	L3_ALC_EN	0	
	1	L2_ALC_EN	0	
	0	L1_ALC_EN	0	
0x17 ADC ALC control 2	[8:7]	***Reserved***		
	[6:4]	MAXGAIN	111	Set max gain of PGA 111: 30 dB; ….-6dB per step; 000: -12dB
	[3:0]	ALCL	1011	ALC target, set signals level at ADC input 0000: -28.5dB FS 0001: -27dB FS …(1.5dB steps) 1110: -7.5dB FS 1111: -6dB FS
0x18 ADC ALC control 3	[8:6]	***Reserved***		
	[5]	TOEN	0	Timeout enable 0: timeout disabled 1: timeout enabled
	[4]	ALCZC	0	ALC used zero cross detection circuit
	[3:0]	HLD	0000	ALC hold time before gain is increased. 0000 : 0ms 0001: 2.67ms 0010: 5.33ms …(time doubles with every step) 1111: 43.7s
0x19 ADC ALC control 4	[8]	***Reserved***		
	[7:4]	DCY	0011	ALC decay(gain ramp-up) time 0000: 24ms 0001: 48ms 0010: 96ms …(time doubles with every step) 1010 or higher: 24.58s
	[3:0]	ATK	0010	ALC attack(gain ramp-down) time

				0000: 6ms 0001: 12ms 0010: 24ms …(time doubles with every step) 1010 or higher: 6.14s
0x1a Noise gate Control	8	***Reserved***		
	[7:3]	ngth	0	Noise gate threshold 00000: -76.5dBfs 00001: -75dBfs …1.5dB Steps 11110: -31.5dBfs 11111: -30dBfs
	[2:1]	ngg	0	Noise gate type X0: PGA gain held constant 01: mute ADC output 11: Reserved(do not use this setting)
	0	ngate	0	Noise gate function enable 1: enable; 0: disable
0x1b 300	[8:4]	***Reserved***		
	[3]	SAR_ch3_EN	0	SARADC channel enable 1: Enable channel; 0: Disable channel
	[2]	SAR_ch2_EN		
	[1]	SAR_ch1_EN		
	[0]	SAR_ch0_EN		
0x1c SARADC result0	[7:0]	SAR_RESULT0	-	SARADC Channel 0 result
0x1d SARADC result1	[7:0]	SAR_RESULT1	-	SARADC Channel 1 result
0x1e SARADC result2	[7:0]	SAR_RESULT2	-	SARADC Channel 2 result
0x1f SARADC result3	[7:0]	SAR_RESULT3	-	SARADC Channel 3 result

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DIGITAL FILTER CHARACTERISTICS

The ADC and DAC employ different digital filters. There are 4 types of digital filter, called Type 0, 1, 2 and 3. The performance of Types 0 and 1 is listed in the table below, the responses of all filters is shown in the proceeding pages.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Filter Type 0 (USB Mode, 250fs operation)					
Passband	+/- 0.05dB	0		0.416fs	
	-6dB		0.5fs		
Passband Ripple				+/- 0.05	dB
Stopband		0.584fs			
Stopband Attenuation	f > 0.584fs	-60			dB
ADC Filter Type 1 (USB mode, 272fs or Normal mode operation)					
Passband	+/- 0.05dB	0		0.4535fs	
	-6dB		0.5fs		
Passband Ripple				+/- 0.05	dB
Stopband		0.5465fs			
Stopband Attenuation	f > 0.5465fs	-60			dB
High Pass Filter Corner Frequency	-3dB		3.7		Hz
	-0.5dB		10.4		
	-0.1dB		21.6		
DAC Filter Type 0 (USB mode, 250fs operation)					
Passband	+/- 0.03dB	0		0.416fs	
	-6dB		0.5fs		
Passband Ripple				+/-0.03	dB
Stopband		0.584fs			
Stopband Attenuation	f > 0.584fs	-50			dB
DAC Filter Type 1 (USB mode, 272fs or Normal mode operation)					
Passband	+/- 0.03dB	0		0.4535fs	
	-6dB		0.5fs		
Passband Ripple				+/- 0.03	dB
Stopband		0.5465fs			
Stopband Attenuation	f > 0.5465fs	-50			dB

Table 31 Digital Filter Characteristics

DAC FILTERS		ADC FILTERS	
Mode	Group Delay	Mode	Group Delay
0	11/FS	0	12/FS
1	18/FS	1	20/FS
2	5/FS	2	3/FS
3	5/FS	3	6/FS

Table 32 ADC/DAC Digital Filters Group Delay

TERMINOLOGY

1. Stop Band Attenuation (dB) - the degree to which the frequency spectrum is attenuated (outside audio band)

2. Pass-band Ripple – any variation of the frequency response in the pass-band region

DIGITAL DE-EMPHASIS CHARACTERISTICS

Figure 35 De-Emphasis Frequency Response (48kHz)

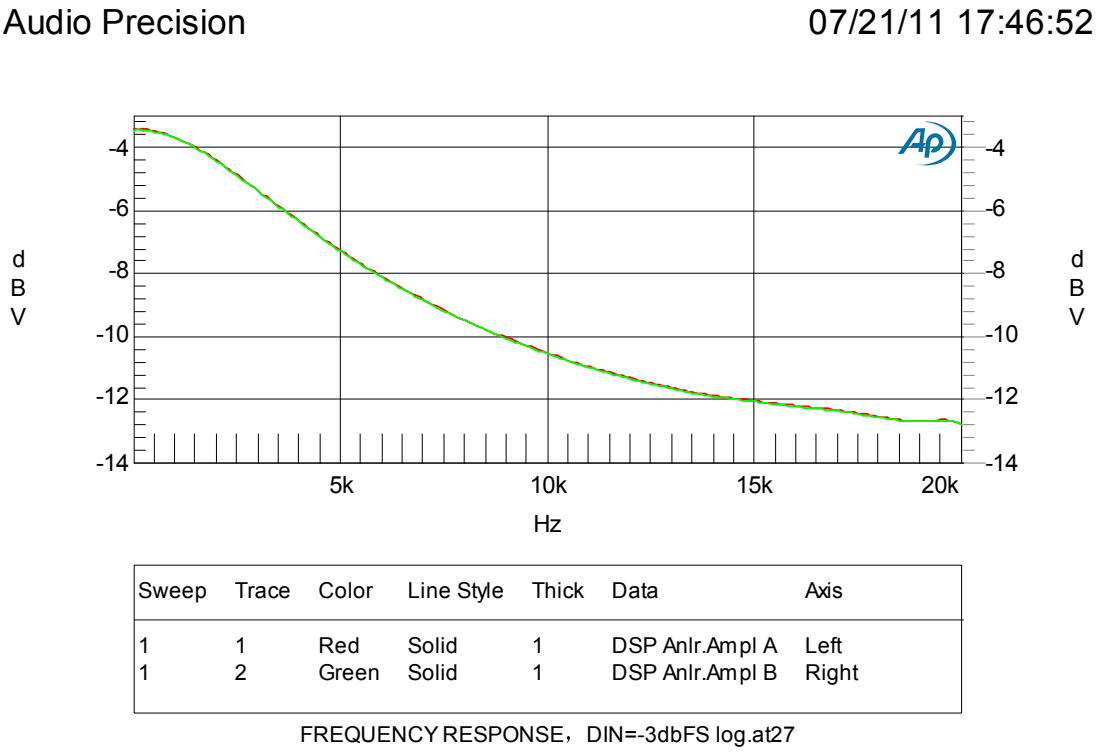
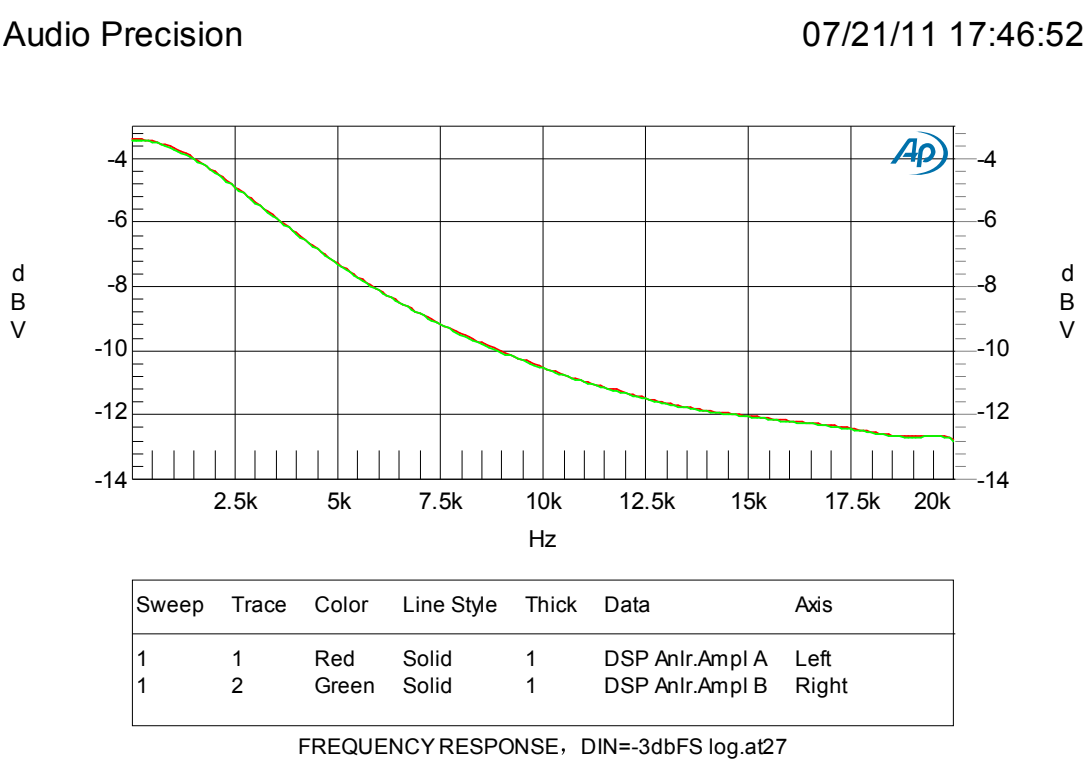


Figure 36 De-Emphasis Frequency Response (44.1kHz)



Sweep	Trace	Color	Line Style	Thick	Data	Axis
1	1	Red	Solid	1	DSP Anlr.Ampl A	Left
1	2	Green	Solid	1	DSP Anlr.Ampl B	Right

FREQUENCY RESPONSE，DIN=-3dbFS log.at27

Figure 37 De-Emphasis Frequency Response (32kHz)

APPLICATIONS INFORMATION

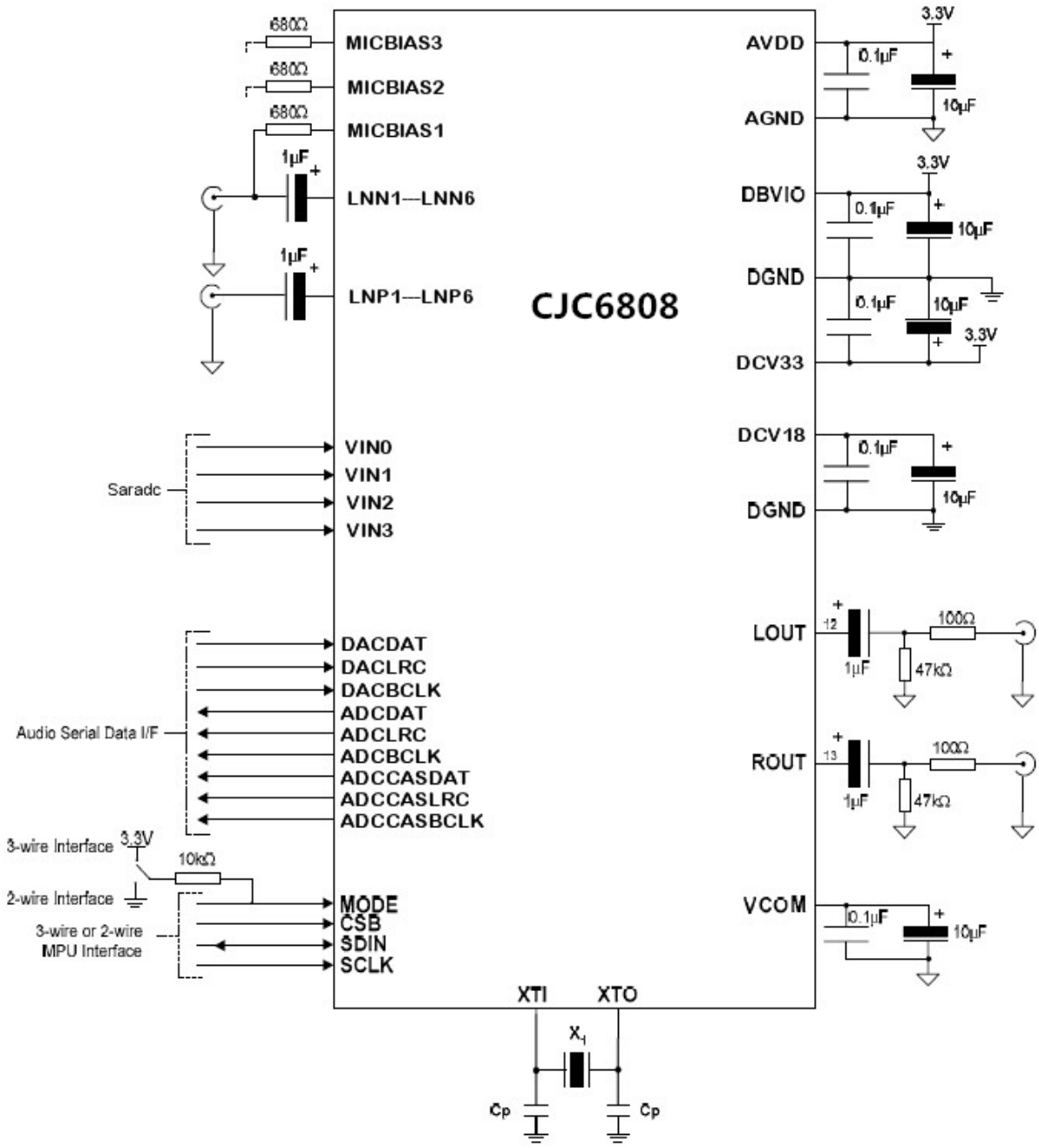


Figure 57 External Components Diagram

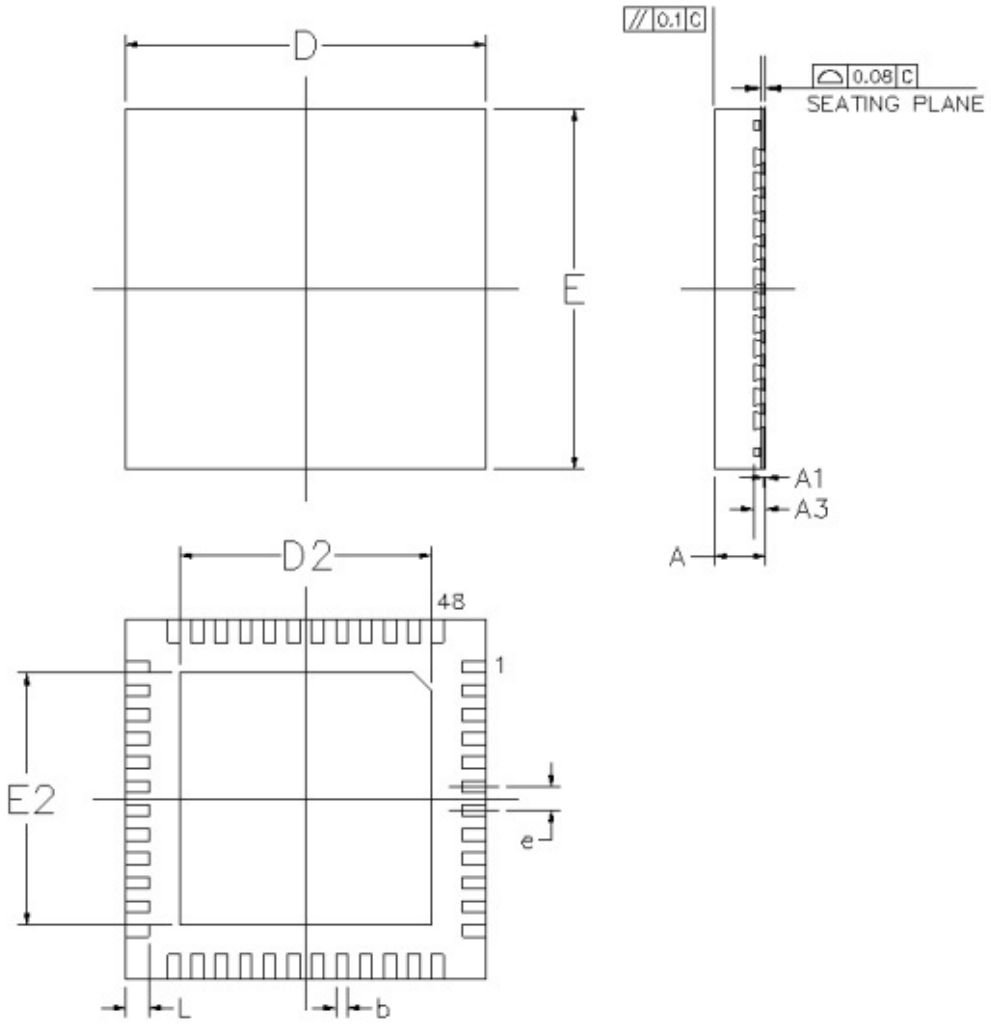
MINIMISING POP NOISE AT THE ANALOGUE OUTPUTS

To minimise any pop or click noise when the system is powered up or down, the following procedures are recommended.

POWER UP SEQUENCE

- Switch on power supplies. By default the CJC6808 is in Standby Mode, the DAC is digitally muted and the Audio Interface and Outputs are all OFF.
- Set all required bits in the Power Down register (0Ch) to '0'; EXCEPT the OUTPD bit, this should be set to '1' (Default).
- Set required values in all other registers except 12h (Active).
- Set the 'Active' bit in register 12h.
- The last write of the sequence should be setting OUTPD to '0' (active) in register 0Ch, enabling the DAC signal path, free of any significant power-up noise. POWER DOWN SEQUENCE
- Set the OUTPD bit to '1' (power down).
- Remove the CJC6808 supplies.

PACKAGE DIMENSIONS – QFN48



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.85	1.00	0.030	0.034	0.039
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_3		0.20 REF			0.008 REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E		6.00BSC			0.236BSC	
D2/E2	4.15	4.4	4.65	0.163	0.173	0.183
e		0.40BSC			0.016BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes··

1. CONTROLLING DIMENSION·· MILLIMETER(mm).
2. REFERENCE DOCUMENTL·· JEDEC MO-220.