2x30 W, 60-W Filter-Free Highly efficient mode Class-D Stereo Amplifier with Spread Spectrum Modulation

FEATURES

- Input Supply Voltage Range: 4.5V to 26V
- Support large output power:
  - ✧ 2×30W into a 8Ω BTL load at 24 V
  - ✧ 1×60W into a 4Ω PBTL load at 24 V
- High Power Efficiency ： up to 94%
- Low output offset voltage: 1.5mV
- Low EMI with spread spectrum modulation
- Low THD: 0.01%@1W@8ohm@24V
- 600-KHz or 500 ± 12%-KHz Selected Switching Frequency
- Master and Slave Synchronization
- Programmable Power Limit
- Parallel BTL Mode Support（PBTL）
- Single and Dual Power Supply Support
- DC-Detect, and Short Circuit Protection with Error Reporting
- Undervoltage and Overvoltage Protection (UVLO and OVP)
- Thermal Shutdown (OTP)
- Package HTSSOP-28 with pad down

GENERAL DESCRIPTION

The iML6603 is a high efficiency stereo Class-D audio amplifier, The high efficiency allows it can support 2 × 30 W without external heat sink on a dual layer PCB. The device provides Parallel BTL application can deliver 60W into 4Ω load at 24V supply voltage.

The iML6603 is achieved together with an option of either master or slave option, making it possible to synchronize multiple devices.

The adjustable power limit function allows to set the PLIMIT voltage rail to limit the amount of current through the speaker. This device is fully protected includes UVLO, OVP, OTP, DC Protection and short-circuit protection.

APPLICATIONS

- Soundbars
- Bluetooth Speaker
- TV audio
- Home Theaters

TYPICAL APPLICATION

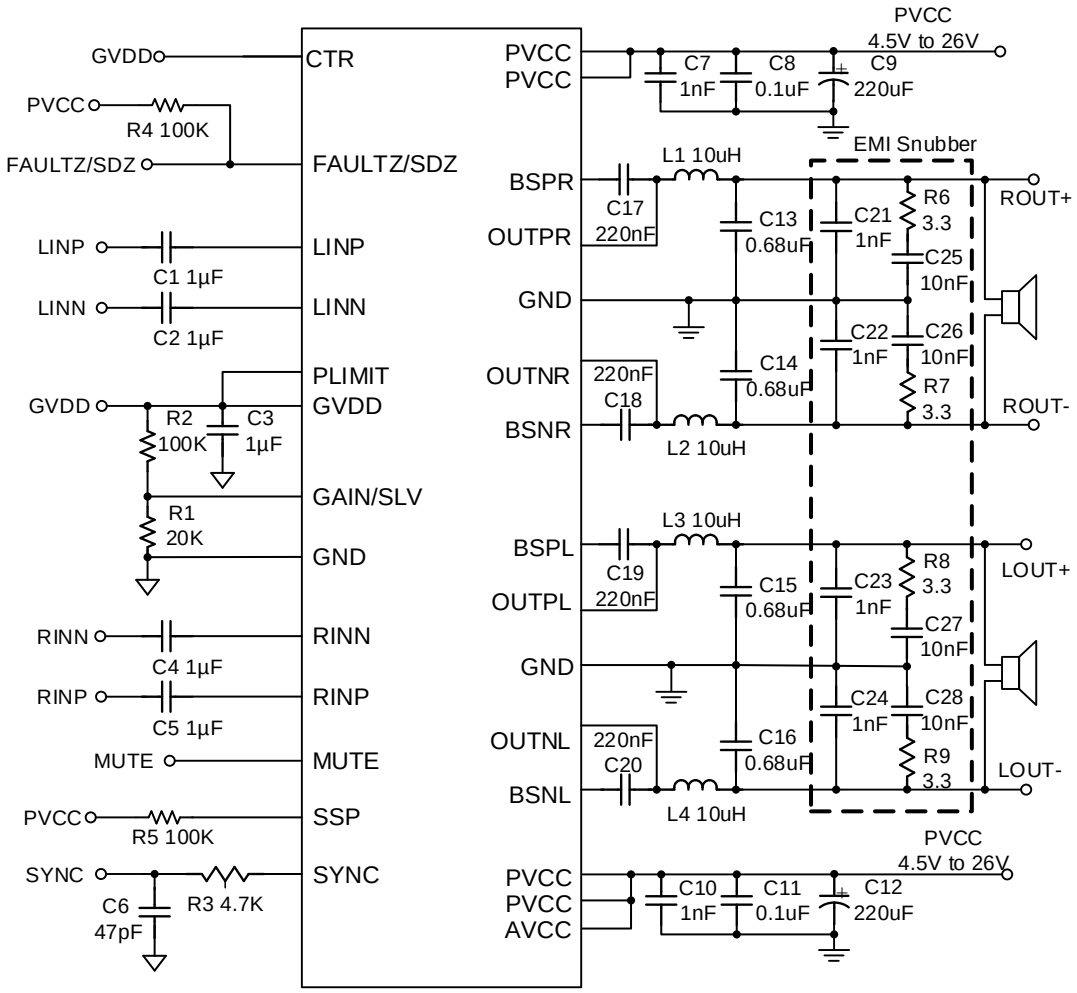


Fig1. Typical Applications

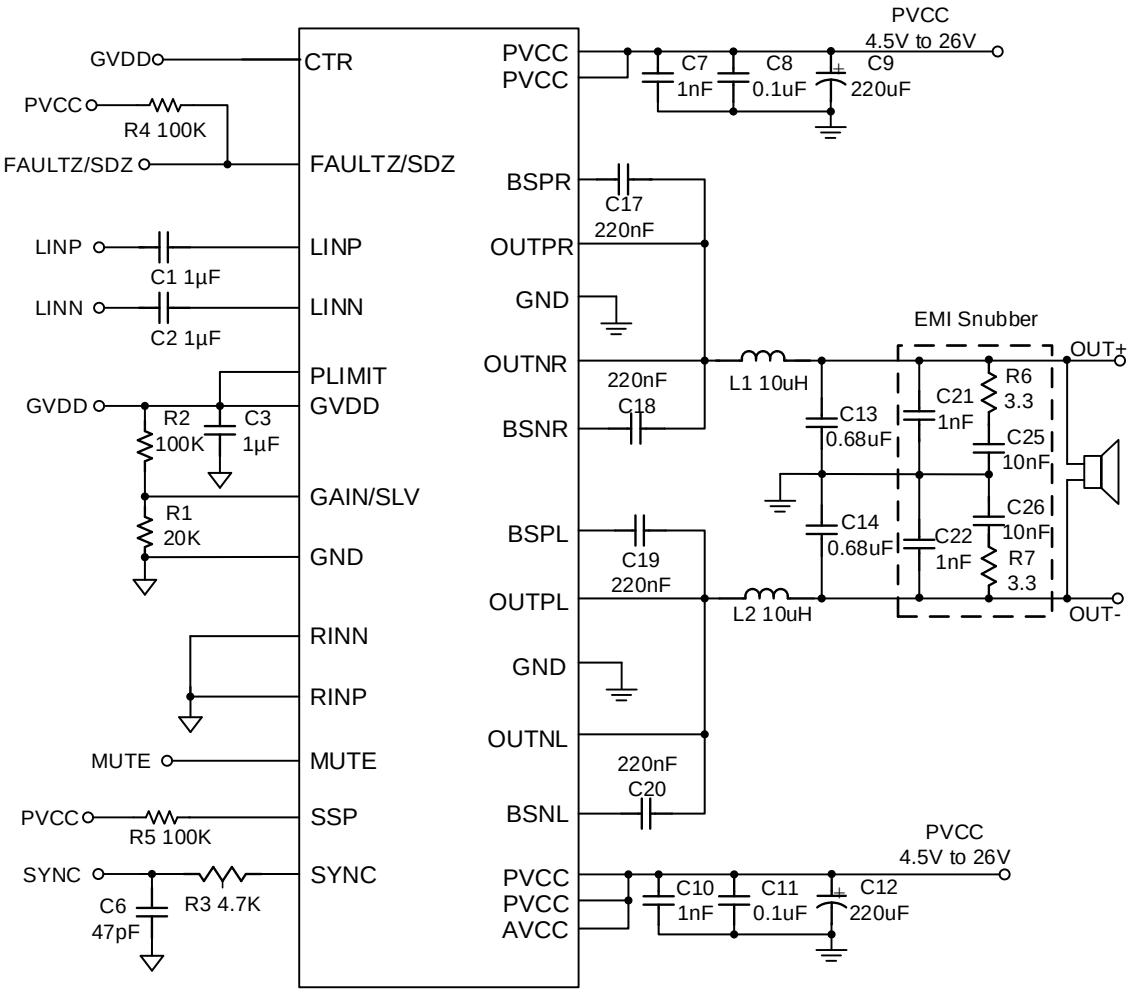


Fig2. Typical PBTL Mode Applications

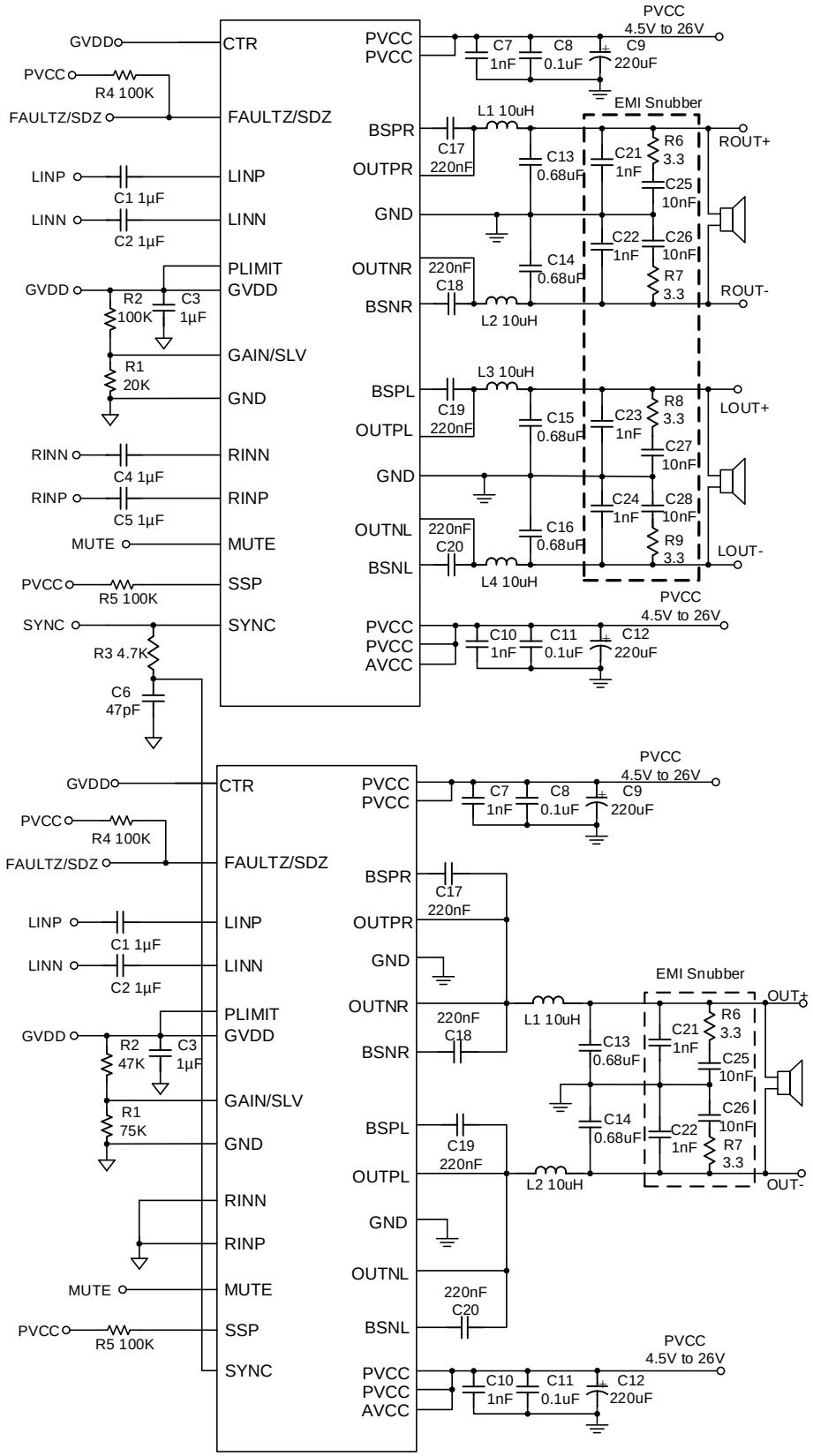


Fig3.Typical 2.1 Master and Slave Applications

ORDERING INFORMATION

DEVICE TYPE	PART NUMBER	PACKAGE	PACKING	TEMP. RANGE	MARKING	MARKING DESCRIPTION
iML6603	iML6603IS -TR	IS: HTSSOP-28	Tape and Reel	–40 °C to +85 °C	iML6603 ZYYWWXXX	iML6603 Part Name YYWW: Date Code XXX: Lot No.

Note: All CHIPONE products are lead free and halogen free.

PIN CONFIGURATION

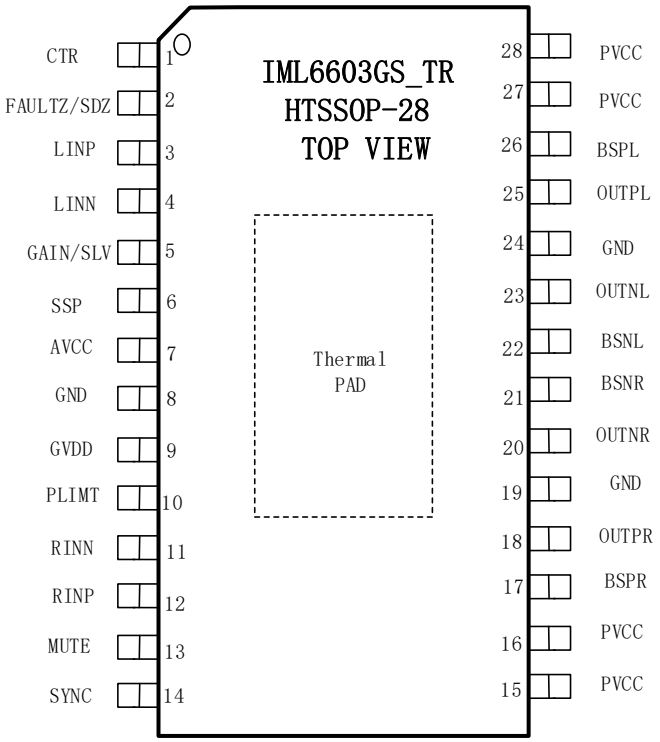


Fig.4 Top View

PIN DESCRIPTION

Name	PIN No.	I/O	Description
CTR	1	I	Connect to GVDD Power。
FAULTZ/SDZ	2	I/O	TTL logic levels with compliance to AVCC. Shutdown logic input for audio amp (LOW, outputs Hi-Z; HIGH, outputs enabled). General fault reporting including Over-Temp, Over-Current, DC Detect. FAULTZ/SDZ=High, normal operation； FAULTZ/SDZ/=Low, fault condition. Device will auto-recover once the OT/OC/DC Fault has been removed.
LINP	3	I	Light channel Positive audio input.
LINN	4	I	Light channel Negative audio input.
GAIN/SLV	5	I	Gain selects least significant bit. TTL logic levels with compliance to AVDD. Low = 20 dB Gain, High =26 dB Gain.
SSP	6	I	Spread spectrum selection： Low=SS disable High=SS enable
AVCC	7	P	Analog Power Supply.
GND	8	P	GND.
GVDD	9	O	Power supply for internal logic. And a supply for PLIMIT and GAIN/SLV resistor dividers.
PLIMIT	10	I	Power limit level adjust. Connect a resistor divider from GVDD to GND to set power limit. Connect directly to GVDD for no power limit.
RINN	11	I	Right channel Negative audio input. Connect to GND for PBTL mode.
RINP	12	I	Right channel Positive audio input. Connect to GND for PBTL mode.
MUTE	13	I	Mute signal for fast disable/enable outputs: High = outputs Hi-Z Low = outputs enabled
SYNC	14	I/O	Clock input/output for synchronizing multiple class-D devices.
PVCC	15	P	Power Supply.
PVCC	16	P	Power Supply.
BSPR	17	I	Boot strap for positive right channel output.
OUTPR	18	O	Positive right channel output.
GND	19	P	Power GND.
OUTNR	20	O	Negative right channel output.
BSNR	21	O	Boot strap for negative right channel output.
BSNL	22	I	Boot strap for negative left channel output.
OUTNL	23	O	Negative left channel output.
GND	24	P	Power GND.

OUTPL	25	O	Positive left channel output.
BSPL	26	I	Boot strap for negative right channel output.
PVCC	27	P	Negative right channel output.
PVCC	28	P	Power GND.
Thermal Pad		P	Connect to GND for best system performance. Also leave floating.

ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Parameters		MIN.	MAX.	Units
Voltage Range	PVCC, AVCC	-0.3	30	V
	INPL, INNL, INPR, INNR	-0.3	6.3	V
	PLIMIT, GAIN / SLV, SYNC	-0.3	GVDD+0.3	V
	SSP, MUTE, SDZ, CTR	-0.3	PVCC+0.3	V
Slew rate Range (2)	SSP, MUTE, SDZ, CTR		10	V/ms
ESD	Human body model (HBM)	±2000		kV
	Charged device model (CDM)	±500		V
Ambient Operating Temperature, T_A		-40	85	℃
Junction Temperature, T_J		-40	150	℃
Storage Information, T_{STG}		-65	150	℃

Note 1 Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2 100-kΩ series resistor is required if maximum slew rate is exceeded.

RECOMMEND OPERATING CONDITIONS (NOTE 2)

Parameters		MIN.	TYP.	MAX.	Units
INPUT VOLTAGE					
PVCC, AVCC	Input voltage range	4.5	--	26	V
C_{PVCC}	PVCC input capacitance (Note 3)	--	220	--	µF
C_{AVCC}	AVCC input capacitance (Note 3)	--	10	--	µF
Logic Input and Output					
SSP, MUTE, SDZ, SYNC, CTR	V_{IH} , High-level input voltage	2			V
SSP, MUTE, SDZ, SYNC, CTR	V_{IL} , Low-level input voltage			0.8	V
FAULTZ, RPULL-UP = 100 kΩ, PVCC = 26 V	V_{OL} , Low-level output voltage	--		0.8	V
SSP, MUTE, SDZ, CTR (VI = 2V, PVCC = 18V)	I_{IH} ,High-level input current			30	uA
Amplifier Output Load					
R_L(BTL), L = 10 µH, C = 680 nF	BTL Minimum load Impedance	3.2	4		Ω
R_L(PBTL), L = 10 µH, C = 1 µF	PBTL Minimum load Impedance	1.6	2		
Lo	Minimum output filter inductance under	1		--	µH

	short-circuit condition				
TEMPERATURE(TSSOP32)					
θ_{JA}	Junction-to-ambient thermal resistance	--	22	--	℃/W
θ_{JC}	Junction-to-case(top) thermal resistance	--	0.3	--	℃/W

Note 2 The device is not guaranteed to function outside its operating conditions.

Note 3 The resulting capacitance of a capacitor changes over voltage and temperature. X7R (or better dielectric material) is recommend.

ELECTRICAL CHARACTERISTICS

TA = 25°C, AVCC = PVCC = 12 V to 24 V, RL = 4 Ω, fs = 500 kHz+-15%, BD mode (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
| VOS |	Class-D output offset voltage (measured differentially)	VI = 0 V		1.5	5	mV
ICC	Quiescent supply current	SDZ = 2 V, No load or filter, PVCC = 12 V	--	13	--	mA
		SDZ = 2 V, No load or filter, PVCC = 24 V	--	17	--	mA
ICC(SD)	Quiescent supply current in shutdown mode	SDZ = 0.8 V, With load and filter, PVCC = 12 V	--	5	--	uA
		SDZ = 0.8 V, With load and filter, PVCC = 24 V	--	9	--	uA
RDS(on)	Drain source on state resistance, measured pin to pin	PVCC = 21 V, Iout = 500 mA, TJ = 25°C		100		mΩ
G	Gain (BTL)	R1 = 5.6 Ω, R2 = Open	19	20	21	dB
		R1 = 20 kΩ, R2 = 100 kΩ	25	26	27	dB
		R1 = 39 kΩ, R2 = 100 kΩ	31	32	33	dB
		R1 = 47 kΩ, R2 = 75 kΩ	35	36	37	dB
G	Gain (SLV)	R1 = 51 kΩ, R2 = 51 kΩ	19	20	21	dB
		R1 = 75 kΩ, R2 = 47 kΩ	25	26	27	dB
		R1 = 100 kΩ, R2 = 39 kΩ	31	32	33	dB
		R1 = 100 kΩ, R2 = 16 kΩ	35	36	37	dB
ton	Turn-on time	SDZ = 2 V	--	80	--	ms
toff	Turn-off time	SDZ = 0.8 V	--	2	--	µs
GVDD	Gate drive voltage	IGVDD<0.2mA	5	5.5	6.2	V
VO	Output voltage maximum under PLIMIT control	V(PLIMIT) = 2 V; VI = 1 Vrms	6.75	8.2	8.75	V

TA = 25°C, AVCC = PVCC = 12 V to 24 V, RL = 4 Ω(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
KSVR	Power supply ripple rejection	200 mVPP ripple at 1 kHz, Gain = 20 dB, Inputs AC coupled to GND		–70		dB
PO	Continuous output power	THD+N = 10%, f = 1 kHz, PVCC = 14.4 V	--	28	--	W
		THD+N = 10%, f = 1 kHz, PVCC = 21 V	--	35	--	W
THD+N	Total harmonic distortion + noise	PVCC = 24 V, f = 1 kHz, PO = 1 W		0.01%		
		PVCC = 24 V, f = 1 kHz, PO = 15 W		0.02%		
Vn	Output integrated noise	20 Hz to 20 kHz, A-weighted filter, Gain = 20 dB，PVCC=12V	--	58	--	μV
			--	–85	--	dBV
	Crosstalk	VO = 1 Vrms, Gain = 20 dB, f = 1 kHz		–100		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N < 1%, f = 1 kHz, Gain = 20 dB, A-weighted		106		dB
Fosc	Oscillator frequency	SSP =0	Fix Frequency：600			KHz
		SSP =1	SSM：500±15%			
TSD	Thermal trip point		--	160	--	°C
TSD_H	Thermal hysteresis		--	20	--	°C
IOCP	Over current trip point			9		A

Functional Block Diagram

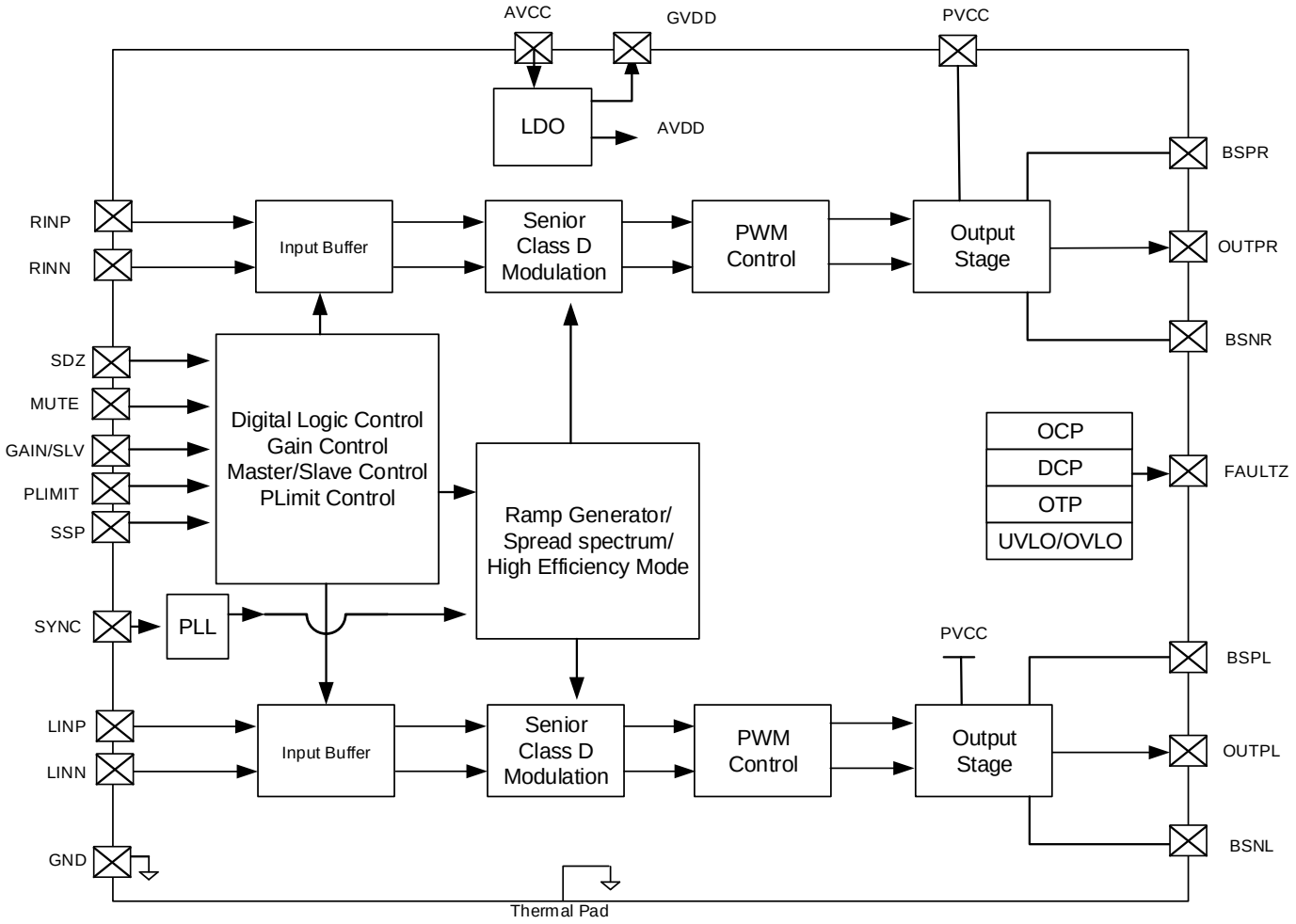


Fig5. iML6603 Functional Block Diagram

Typical Performance Characteristics

fs = 400 kHz, High Efficiency of Modulation, Tested with AP525B. (unless otherwise noted)

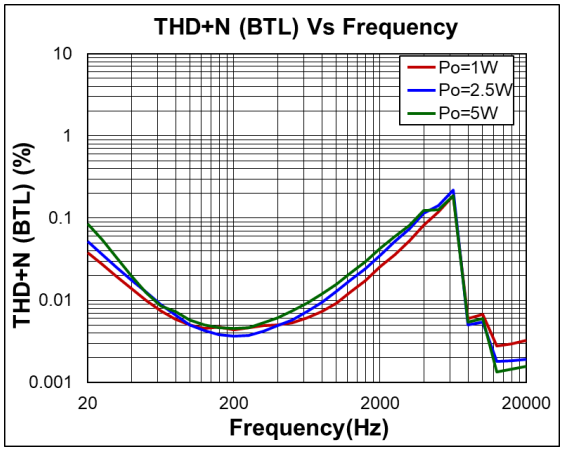


Fig6. THD+N (BTL) vs Frequency

PVCC=AVCC=12V, Load=8ohm

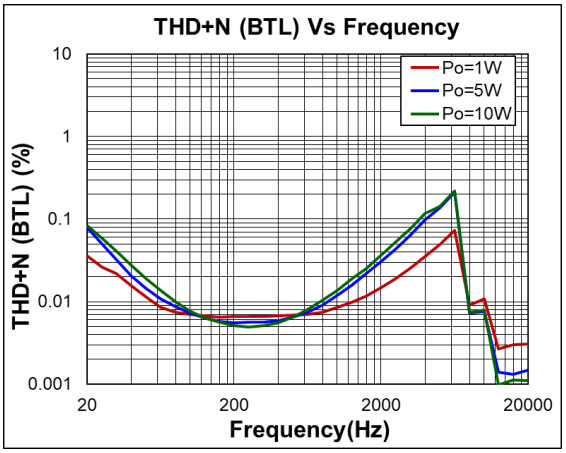


Fig7. THD+N (BTL) vs Frequency

PVCC=AVCC=24V, Load=8ohm

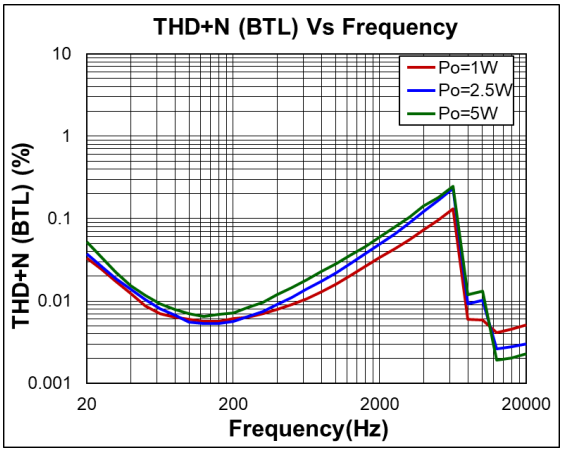


Fig8. THD+N (BTL) vs Frequency

PVCC=AVCC=12V, Load=4ohm

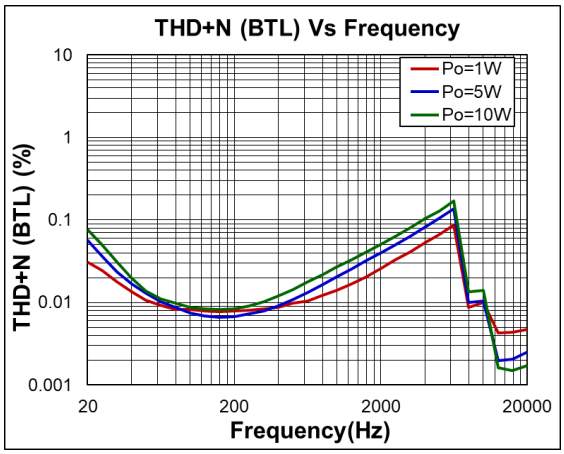


Fig9. THD+N (BTL) vs Frequency

PVCC=AVCC=24V, Load=4ohm

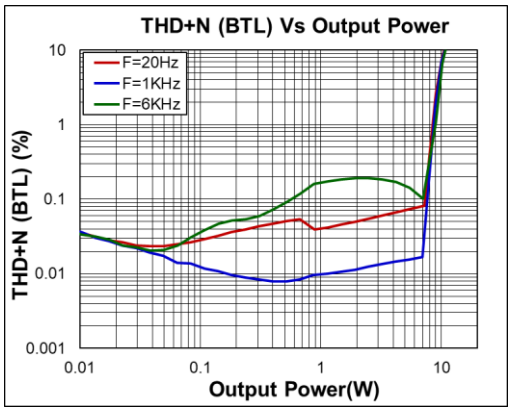


Fig10. THD+N (BTL) vs Power

PVCC=AVCC=12V, Load=8ohm

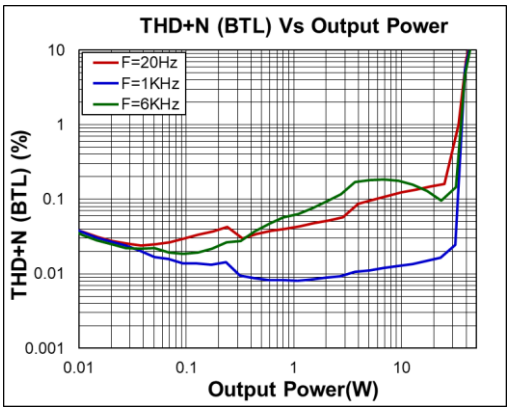


Fig11. THD+N (BTL) vs Power

PVCC=AVCC=24V, Load=8ohm

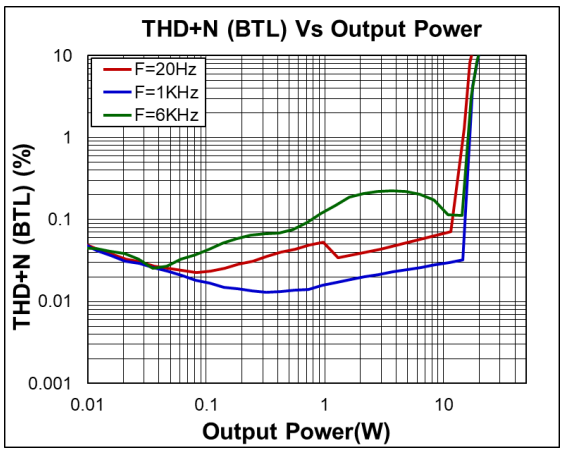


Fig12. THD+N (BTL) vs Output Power

PVCC=AVCC=12V, Load=4ohm

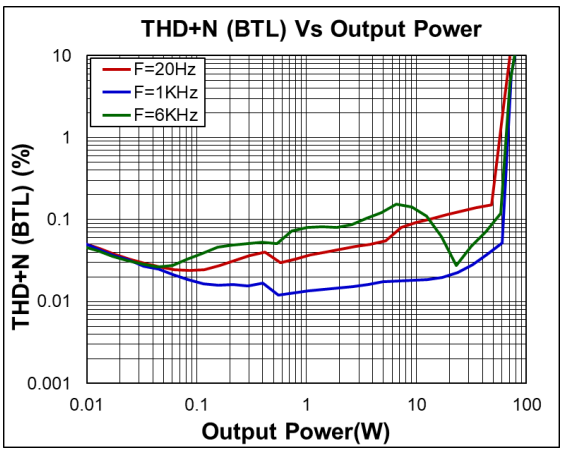


Fig13. THD+N (BTL) vs Output Power

PVCC=AVCC=24V, Load=4ohm

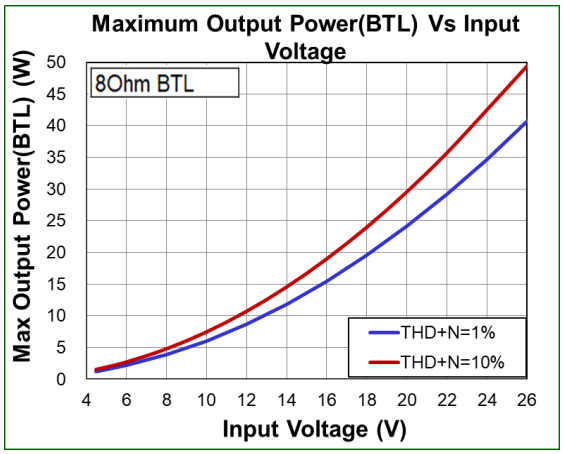


Fig14. Maximum Output Power vs Input Voltage

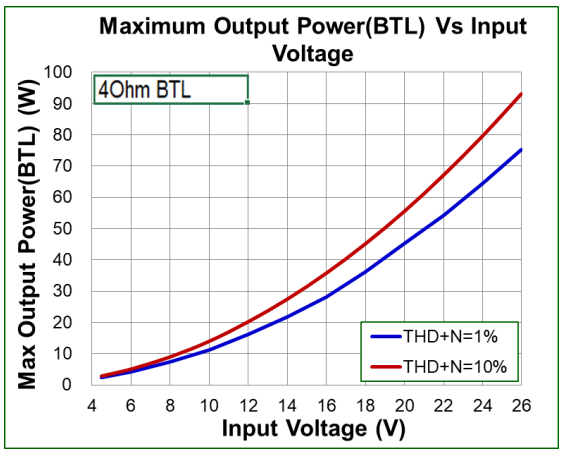


Fig15. Maximum Output Power vs Input Voltage

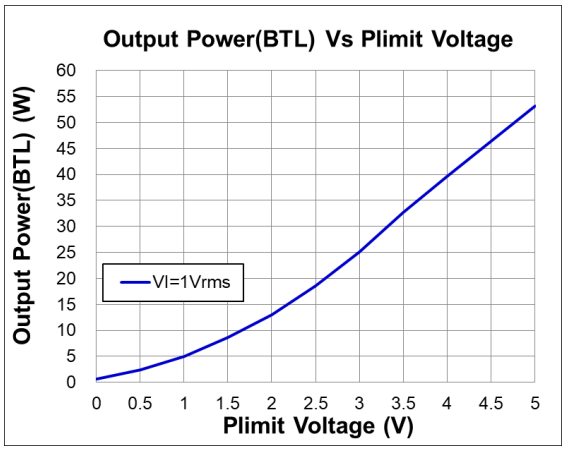


Fig16. Output Power vs Plimit Voltage

PVCC=AVCC=24V, Load=4ohm

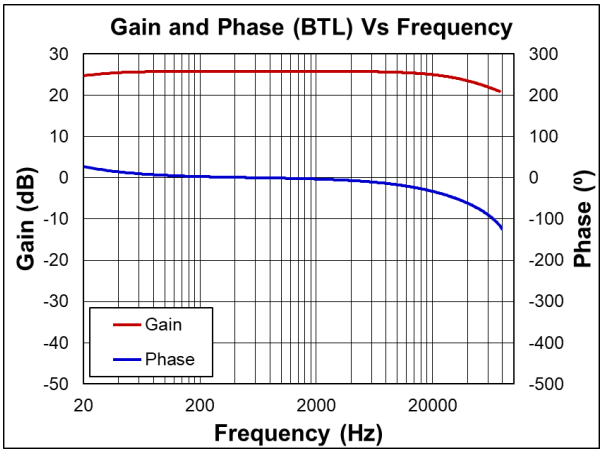


Fig17. Gain and Phase (BTL) vs Frequency

PVCC=AVCC=12V, Load=4ohm, Po=1W

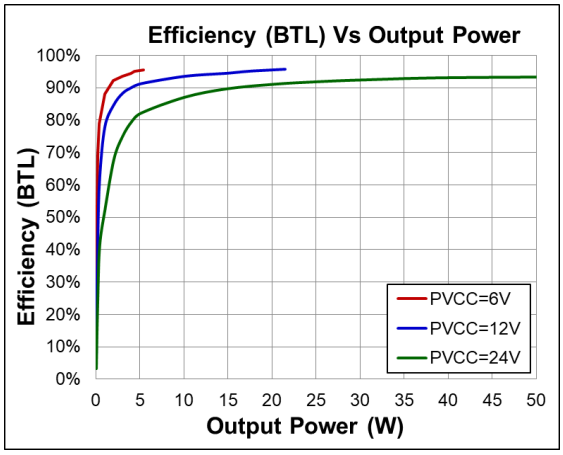


Fig18. Efficiency (BTL) vs Output Power

Load=8ohm, Gain=26dB

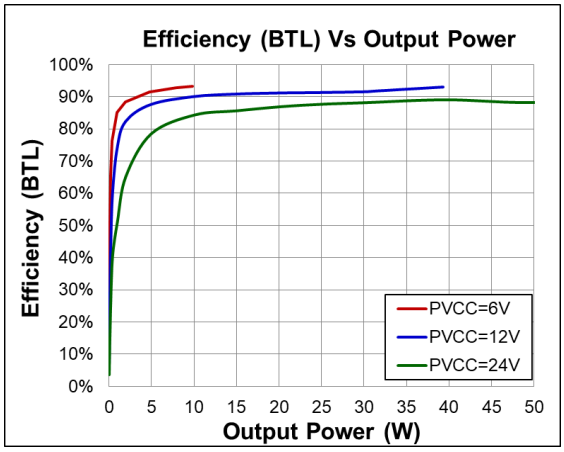


Fig19. Efficiency (BTL) vs Output Power

Load=4ohm, Gain=26dB

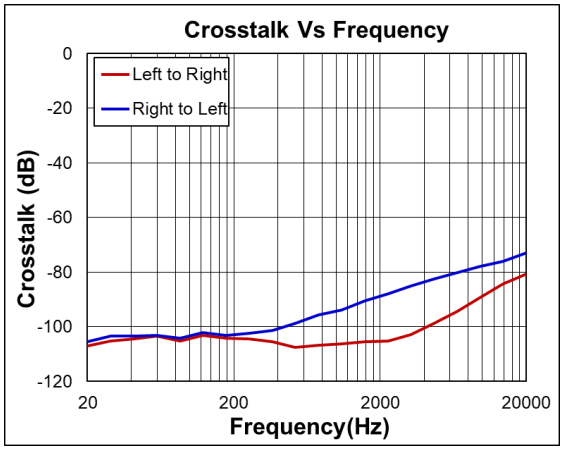


Fig20. Maximum Output Power vs Input Voltage

PVCC=AVCC=12V, Load=8ohm, Gain=26dB

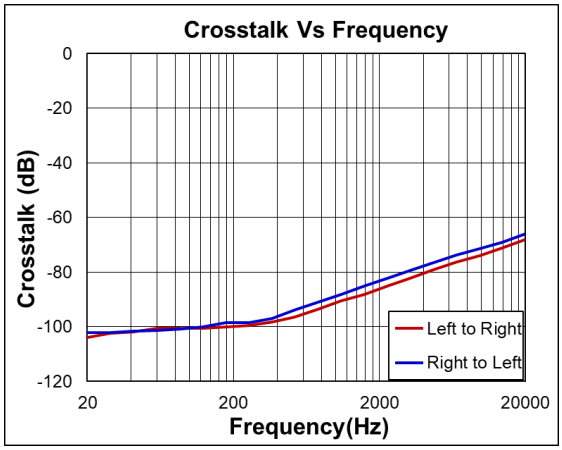


Fig21. Maximum Output Power vs Input Voltage

PVCC=AVCC=12V, Load=4ohm, Gain=26dB

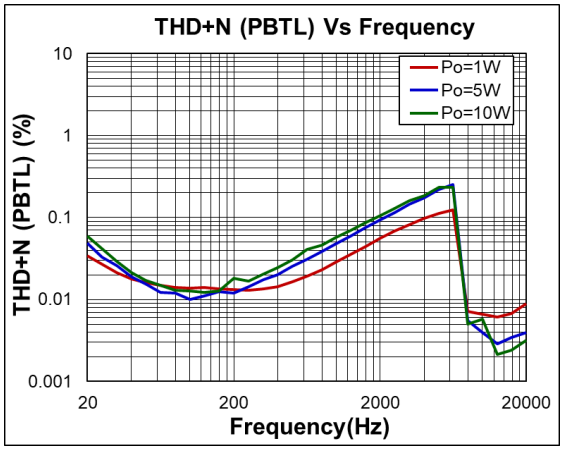


Fig22. THD+N (PBTL) vs Frequency

PVCC=AVCC=12V, Load=2ohm, PBTL mode

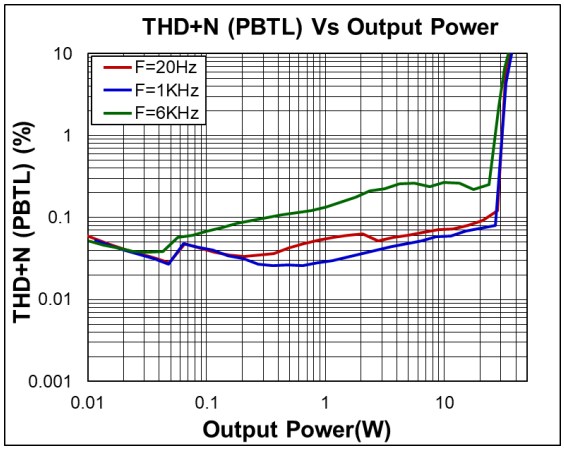


Fig23. THD+N (PBTL) vs Power

PVCC=AVCC=12V, Load=2ohm, PBTL mode

Detailed Description

Overview

The iML6603 is a highly efficient amplifier with extreme low idle power dissipation. It can support as low as 15-mA idle loss current using standard LC filter configurations. It is integrated with 100-mΩ MOSFET that allows output currents up to 9 A. The high efficiency allows the amplifier to provide an excellent performance without the requirement for a bulky heat sink.

The device can be configured for either master or slave operation by using the SYNC pin. Configuring using the SYNC pin helps to prevent audible beats noise.

Feature Description

Undervoltage Lockout Function

The device has a build in undervoltage lockout function that disables the device when the input supply voltages is too low for normal operation.

Gain Setting and Master and Slave

The gain of the iML6603 is set by the voltage divider connected to the GAIN/SLV control pin. Master or Slave mode is also controlled by the same pin. An internal ADC is used to detect the 8 input states. The first four stages set the GAIN in Master mode in gains of 20, 26, 32, 36 dB respectively, while the next four stages sets the GAIN in Slave mode in gains of 20, 26, 32, 36 dB respectively. The gain setting is latched during power-up and cannot be changed while device is powered. Table 1 lists the recommended resistor values and the state and gain, Resistor tolerance should be 5% or better.

MASTER / SLAVE MODE	GAIN	R1 (to GND)	R2 (to GVDD)
Master	20 dB	5.6 kΩ	OPEN
Master	26 dB	20 kΩ	100 kΩ
Master	32 dB	39 kΩ	100 kΩ
Master	36 dB	47 kΩ	75 kΩ
Slave	20 dB	51 kΩ	51 kΩ
Slave	26 dB	75 kΩ	47 kΩ
Slave	32 dB	100 kΩ	39 kΩ
Slave	36 dB	100 kΩ	16 kΩ

Table 1. Gain and Master/Slave Table

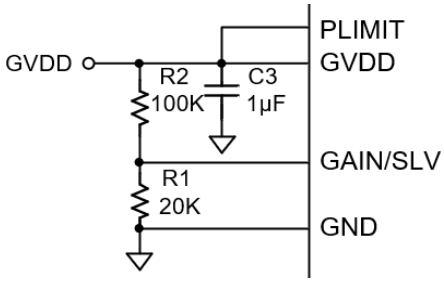


Figure 24. Gain, Master/Slave

In Master mode, SYNC terminal is an output, in Slave mode, SYNC terminal is an input for a clock input. TTL logic levels with compliance to GVDD.

Input Impedance

The iML6603 input stage is a fully differential input stage and the input impedance changes with the gain setting from 7.2 kΩ at 36 dB gain to 48 kΩ at 20 dB gain. Table 1 lists the values from min to max gain. The tolerance of the input resistor value is ±20% so the minimum value will be higher than 5.76 kΩ. The inputs must be AC-coupled to minimize the output dc-offset and ensure correct ramping of the output voltages during power ON and power OFF. The input ac-coupling capacitor together with the input impedance forms a high-pass filter with the following cut-off frequency:

$f=1/2\pi Z_i R_i$ (1)

If a flat bass response is required down to 20 Hz the recommended cut-off frequency is a tenth of that, 2 Hz. Table 2 lists the recommended ac-couplings capacitors for each gain step. If a –3-dB capacitor is accepted at 20 Hz 10 times lower capacitors can used – for example, a 1-μF capacitor can be used.

GAIN	INPUT IMPEDANCE (k ohm)	INPUT CAPACITANCE (uF)	HIGH-PASS FILTER (HZ)
20 dB	48	1.5	2.25 Hz
26 dB	24	3.3	2 Hz
32 dB	12	5.6	2.88 Hz
36 dB	7.2	10	2.3 Hz

Table 2. Recommended Input AC-Coupling Capacitors

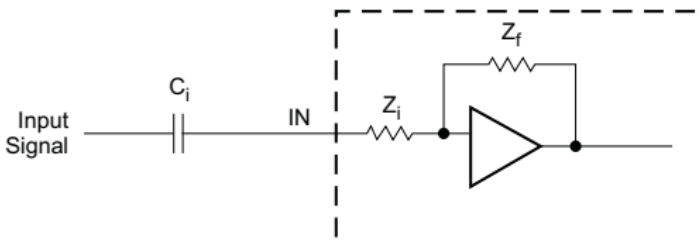


Figure 25. Input Impedance

The input capacitors used should be a type with low leakage, such as quality electrolytic, tantalum, or ceramic capacitors. If a polarized type is used the positive connection should face the input pins which are biased to 3Vdc.

Startup and Shutdown Operation

The iML6603 employs a shutdown mode of operation designed to reduce supply current (Icc) to the absolute minimum level during periods of nonuse for power conservation. The SDZ input terminal should be held high(see specification table for trip point) during normal operation when the amplifier is in use. Pulling SDZ low will put the outputs to mute and the amplifier to enter a low-current state. Do not leave SDZ unconnected, because amplifier operation would be unpredictable.

For the best power-off pop performance, place the amplifier in the shutdown mode prior to removing the power supply. The gain setting is selected at the end of the start-up cycle. At the end of the start-up cycle, the gain is selected and cannot be changed until the next power-up.

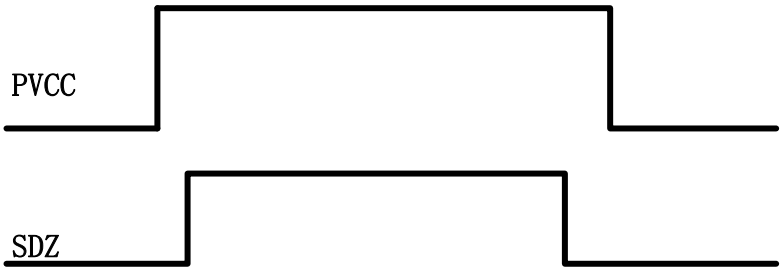


Fig26. Timing Requirement for SDZ and PVCC

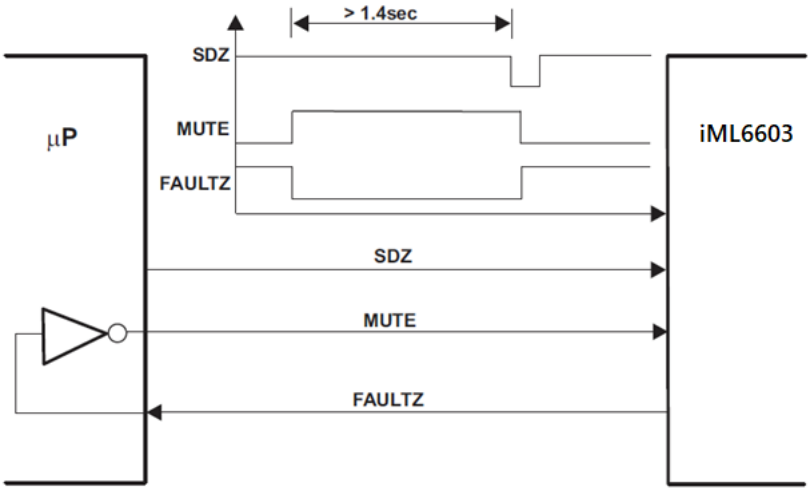


Fig27. Timing Requirement for SDZ

PLIMIT Operation

The iML6603 has a built-in voltage limiter that can be used to limit the output voltage level below the supply rail, the amplifier operates as if it was powered by a lower supply voltage, and thereby limits the output power. Add a resistor divider from GVDD to ground to set the voltage at the PLIMIT pin. An external reference may also be used if tighter tolerance is required. Add a 1-µF capacitor from pin PLIMIT to ground to ensure stability.

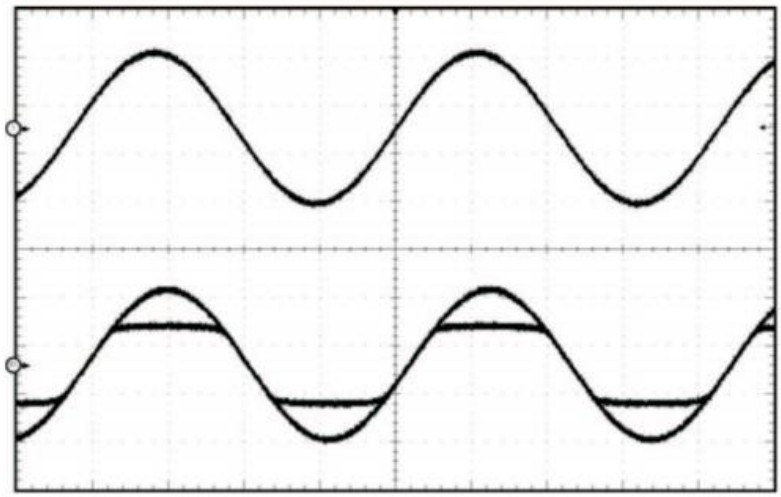


Figure 28. Power Limit Example

The PLIMIT circuit sets a limit on the output peak-to-peak voltage. The limiting is done by limiting the duty cycle to a fixed maximum value. The limit can be thought of as a "virtual" voltage rail which is lower than the supply connected to PVCC. The "virtual" rail is approximately four times the voltage at the PLIMIT pin. The output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L} \quad \text{for unclipped power} \qquad (2)$$

- P_{OUT} (10%THD) = 1.25 × P_{OUT} (unclipped)
- R_L is the load resistance.
- R_S is the total series resistance including RDS(on), and output filter resistance.
- V_P is the peak amplitude, which is limited by "virtual" voltage rail.

PVCC (V)	PLIMIT VOLTAGE (V)(1)	R to GND	R to GVDD	OUTPUT VOLTAGE (Vrms)
24 V	GVDD	Open	Short	17.9
24 V	3.5	45 kΩ	35 kΩ	12.4
24 V	2	24 kΩ	50 kΩ	8
12 V	GVDD	Open	Short	10.76
12 V	2	24 kΩ	50 kΩ	8
12 V	1.5	18 kΩ	56 kΩ	6.5

Table 3. Power Limit Example

(1) PLIMIT measurements taken with EVM gain set to 26 dB and input voltage set to 1 Vrms.

GVDD Supply

The GVDD Supply is used to power the gates of the output full bridge transistors. The GVDD Supply can also be used to supply the PLIMIT and GAIN/SLV voltage dividers. Decouple GVDD with a X5R ceramic 1-µF capacitor to GND. The GVDD supply is not intended to be used for external supply. The current consumption should be limited by using resistor voltage dividers for GAIN/SLV and PLIMIT of 100 kΩ or more.

BSPx AND BSNx Capacitors

The full H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 220-nF ceramic capacitor of quality X5R or better, rated for at least 16 V, must be connected from each output to the corresponding bootstrap input. (See the application circuit diagram in Figure 1.) The bootstrap capacitors connected between the BSxx pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

Differential Inputs

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the iML6603 with a differential source, connect the positive lead of the source to the RINP or LINP input and the negative lead from the source to the RINN or LINN input. To use the iML6603 with a single-ended source, ac ground the negative input through a capacitor equal in value to the input capacitor on positive and apply the source to either input. In a single-ended input application, the unused input should be ac grounded at the source instead of at the device input for best noise performance. For good transient performance, the impedance seen at each of the two differential inputs should be the same.

The impedance seen at the inputs should be limited to an RC time constant of 1 ms or less if possible to allow the input dc blocking capacitors to become completely charged during the 40-ms power-up time. If the input capacitors are not allowed to completely charge, there will be some additional sensitivity to component matching which can result in pop if the input components are not well matched.

Protection Features

The iML6603 contains a complete set of protection circuits carefully designed to make system design efficient as well as to protect the device against any kind of permanent failures due to short circuits, overload, over temperature, and under-voltage. The FAULTZ pin will signal if an error is detected according to Table 4:

FAULT	TRIGGERING CONDITION (typical value)	FAULTZ	ACTION	LATCHED /SELFCLEARING
Over Current	Output short or short to PVCC or GND	Low	Output high impedance	Latched
Over Temperature	Tj > 160°C	Low	Output high impedance	Latched

Too High DC Offset	DC output voltage	Low	Output high impedance	Latched
Under Voltage on PVCC	PVCC < 4.5V	–	Output high impedance	Self-clearing
Over Voltage on PVCC	PVCC > 28V	–	Output high impedance	Self-clearing

Table 4. Fault Reporting

DC Detect Protection

The iML6603 has circuitry which will protect the speakers from DC current which might occur due to defective capacitors on the input or shorts on the printed circuit board at the inputs. A DC detect fault will be reported on the FAULT pin as a low state. The DC Detect fault will also cause the amplifier to shutdown by changing the state of the outputs to Hi-Z.

FAULTZ and SDZ pins are connected internally to allow the FAULTZ pin function to automatically drive the SDZ pin low which clears the DC Detect protection latch.

A DC Detect Fault is issued when the output differential voltage of either channel exceeds DC protection threshold level for more than 640ms at the same polarity. Table 5 below shows some examples of the typical DC Detect Protection threshold for several values of the supply voltage. The Detect Protection Threshold feature protects the speaker from large DC currents or AC currents less than 2 Hz. To avoid nuisance faults due to the DC detect circuit, hold the SD pin low at power-up until the signals at the inputs are stable. Also, take care to match the impedance seen at the positive and negative inputs to avoid nuisance DC detect faults.

Table 5 lists the minimum output offset voltages required to trigger the DC detect. The outputs must remain at or above the voltage listed in the table for more than 640 ms to trigger the DC detect.

PVCC (V)	VOS - OUTPUT OFFSET VOLTAGE (V)
4.5	0.9
6	1.2
12	2.4
18	3.6

Table5. DC Detect Threshold

Short-Circuit Protection and Automatic Recovery Feature

The iML6603 has protection from over current conditions caused by a short circuit on the output stage. The short circuit protection fault is reported on the FAULTZ pin as a low state. The amplifier outputs are switched to a high impedance state when the short circuit protection latch is engaged. The latch can be cleared by cycling the SDZ pin through the low state.

FAULTZ and SDZ pins are connected internally to allows the FAULTZ pin function to automatically drive the SDZ pin low which clears short-circuit protection latch.

In systems where a possibility of a permanent short from the output to PVDD or to a high voltage battery like a car battery can occur, pull the MUTE pin low with the FAULTZ signal with a inverting transistor to ensure a High-Z restart.

Thermal Protection

Thermal protection on the iML6603 prevents damage to the device when the internal die temperature exceeds 160°C. This trip point has a ±15°C tolerance from device to device. Once the die temperature exceeds the thermal trip point, the device enters into the shutdown state and the outputs are disabled. This is a latched fault.

Thermal protection faults are reported on the FAULTZ terminal as a low state.

FAULTZ and SDZ pins are connected internally to allows the FAULTZ pin function to automatically drive the SDZ pin low which clears the thermal protection latch.

Device Modulation Scheme

The iML6603 have the option of running in either BD modulation or high efficient mode.

BD-Modulation

This is a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load with short speaker wires. Each output is switching from 0 volts to the supply voltage. The OUTPx and OUTNx are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUTPx is greater than 50% and OUTNx is less than 50% for positive output voltages. The duty cycle of OUTPx is less than 50% and OUTNx is greater than 50% for negative output voltages. The voltage across the load sits at 0V throughout most of the switching period, reducing the switching current, which reduces any I2R losses in the load.

Efficiency: LC Filter Required with the Traditional Modulation Scheme

The main reason that the traditional amplifier-based on AD modulation requires an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme, because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is 2 × PVCC, and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is required to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The iML6603 modulation schemes have little loss in the load without a filter because the pulses are short and the change in voltage is PVCC instead of 2 × PVCC. As the output power increases, the pulses widen, making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not required.

An LC filter with a cutoff frequency less than the switching frequency allows the switching current to flow through the

filter instead of the load. The filter has less resistance but higher impedance at the switching frequency than the speaker, which results in less power dissipation, therefore increasing efficiency.

Ferrite Bead Filter Considerations

Using the Advanced Emissions Suppression Technology in the iML6603 amplifiers, a high efficiency amplifier can be designed while minimizing interference to surrounding circuits. Designing the amplifier can also be accomplished with only a low-cost ferrite bead filter. In this case the user must carefully select the ferrite bead used in the filter. One important aspect of the ferrite bead selection is the type of material used in the ferrite bead. Not all ferrite material is alike, therefore the user must select a material that is effective in the 10-MHz to 100-MHz range which is key to the operation of the amplifier. Many of the specifications regulating consumer electronics have emissions limits as low as 30MHz. The ferrite bead filter should be used to block radiation in the 30-MHz and above range from appearing on the speaker wires and the power supply lines which are good antennas for these signals. The impedance of the ferrite bead can be used along with a small capacitor with a value in the range of 1000 pF to reduce the frequency spectrum of the signal to an acceptable level. For best performance, the resonant frequency of the ferrite bead/ capacitor filter should be less than 10MHz.

Also, the ferrite bead must be large enough to maintain its impedance at the peak currents expected for the amplifier. Some ferrite bead manufacturers specify the bead impedance at a variety of current levels. In this case the user can make sure the ferrite bead maintains an adequate amount of impedance at the peak current the amplifier will see. If these specifications are not available, the device can also estimate the bead current handling capability by measuring the resonant frequency of the filter output at low power and at maximum power. A change of resonant frequency of less than fifty percent under this condition is desirable.

A high-quality ceramic capacitor is also required for the ferrite bead filter. A low ESR capacitor with good temperature and voltage characteristics will work best.

Additional EMC improvements may be obtained by adding snubber networks from each of the outputs to ground. Suggested values for a simple RC series snubber network would be 18 Ω in series with a 330-pF capacitor although design of the snubber network is specific to every application and must be designed taking into account the parasitic reactance of the printed circuit board as well as the amp. Take care to evaluate the stress on the component in the snubber network especially if the amp is running at high PVCC. Also, make sure the layout of the snubber network is tight and returns directly to the GND pins on the IC.

When to Use an Output Filter for EMI Suppression

A complete LC reconstruction filter should be added in some circuit instances. These circumstances might occur if there are nearby circuits which are sensitive to noise. In these cases a classic second order Butterworth filter similar to those shown in the figures below can be used.

Some systems have little power supply decoupling from the AC line but are also subject to line conducted interference (LCI) regulations. These include systems powered by "wall warts" and "power bricks." In these cases, LC reconstruction filters can be the lowest cost means to pass LCI tests. Common mode chokes using low frequency ferrite material can

also be effective at preventing line conducted interference.

Device Functional Modes

PBTL Mode

The iML6603 can be connected in PBTL mode enabling up to 60W output power. This is done by:

- Connect RINN and RINP directly to Ground (without capacitors) this sets the device in Mono mode during power up.
- Connect OUTPR and OUTNR together for the positive speaker terminal and OUTNL and OUTPL together for the negative pin.
- Analog input signal is applied to LINP and LINN.

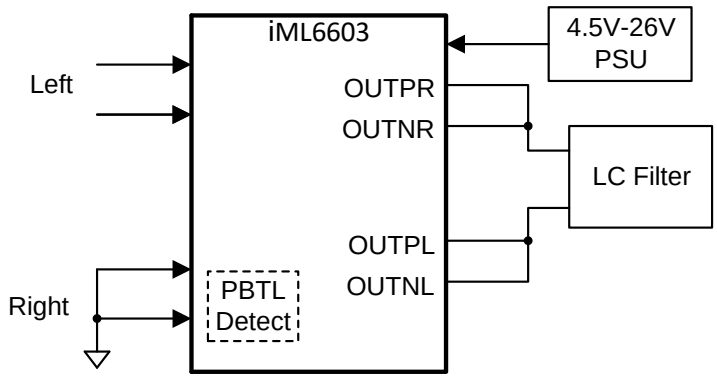


Figure 29. PBTL Mode

Layout

layout Guidelines

The iML6603 is the class-D structure, the switching edges are fast, so the layout of the printed circuit board must be planned carefully. The following suggestions will help to meet EMC requirements.

- Decoupling capacitors — The high-frequency decoupling capacitors should be placed as close to the PVCC and AVCC terminals as possible. Large (220uF or greater) bulk power supply decoupling capacitors should be placed near the iML6603 on the PVCC supplies. Local, high-frequency bypass capacitors should be placed as close to the PVCC pins as possible. These caps can be connected to the IC GND pad directly for an excellent ground connection. Consider adding a small, good quality low ESR ceramic capacitor between 220 pF and 1nF and a larger mid-frequency cap of value between 100nF and 1µF also of good quality to the PVCC connections at each end of the chip.
- Keep the current loop from each of the outputs through the LC filter and the small filter cap and back to GND as small and tight as possible. The size of this current loop determines its effectiveness as an antenna.
- Grounding — The PVCC decoupling capacitors should connect to GND. All ground should be connected at

the IC GND, which should be used as a central ground connection or star ground for the iML6603.

- Output filter — The LC filter should be placed as close to the output terminals as possible, the capacitors used in the LC filters should be grounded.

layout Example

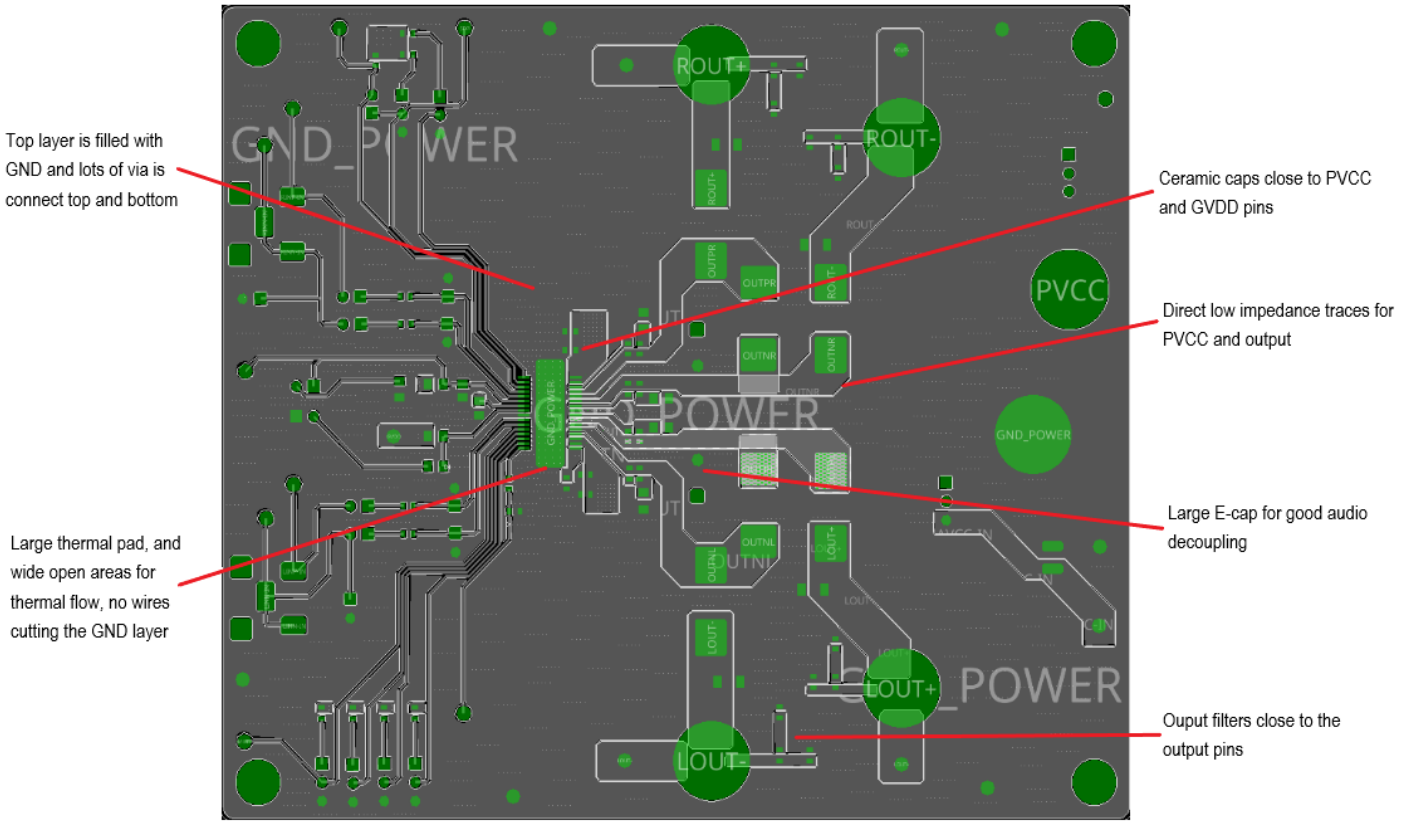


Figure30. Layout Example Top

Continue

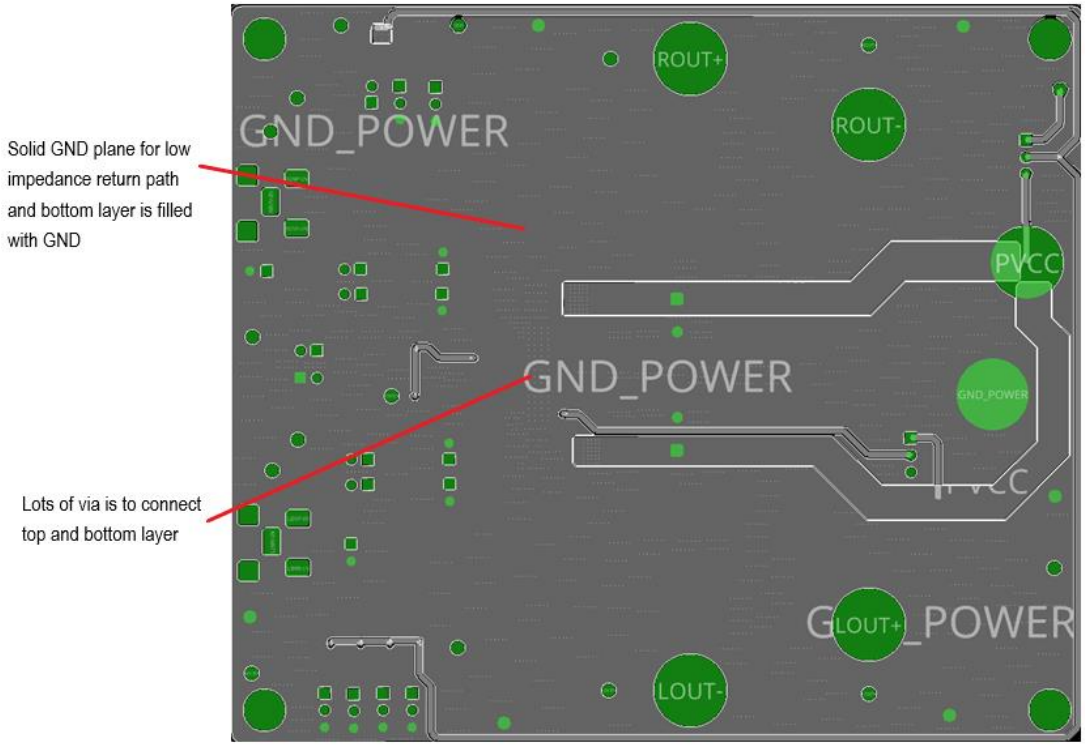
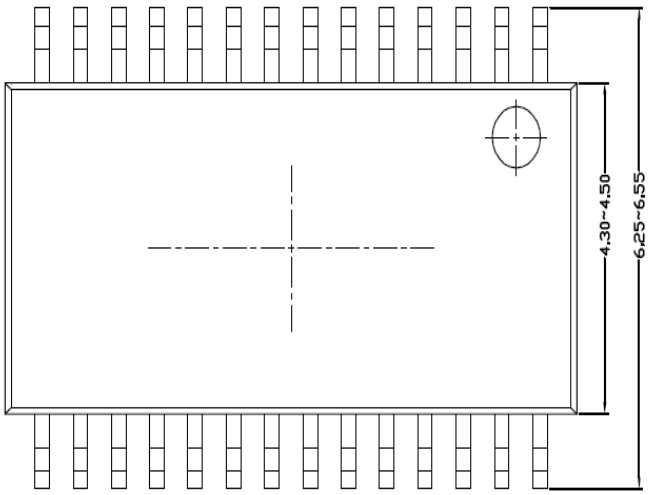
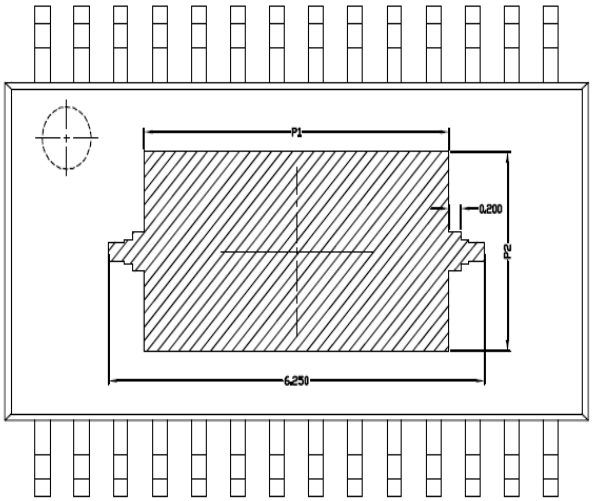


Figure31. Layout Example Bottom

Package Information



TOP VIEW



BOTTOM VIEW

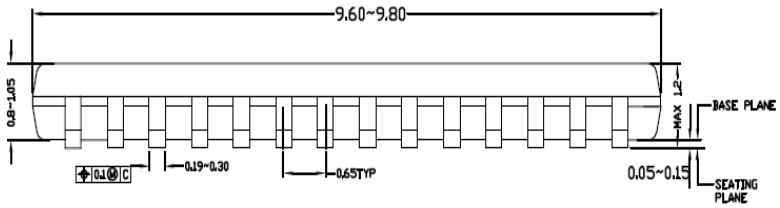


Table for TSSOP-EP/28 of exposed die pad size

Pad Size	Symbol	Min	Nom	Max
118*232	P1	5.40	5.50	5.60
	P2	2.50	2.60	2.70

NOTE

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