LOW POWER TOUCH SENSOR

The Best Touch Sensor Solution!

GREENCHIP

GreenTouch3LP™ GTX314L Capacitive Touch Sensor

DATASHEET
VER6.01

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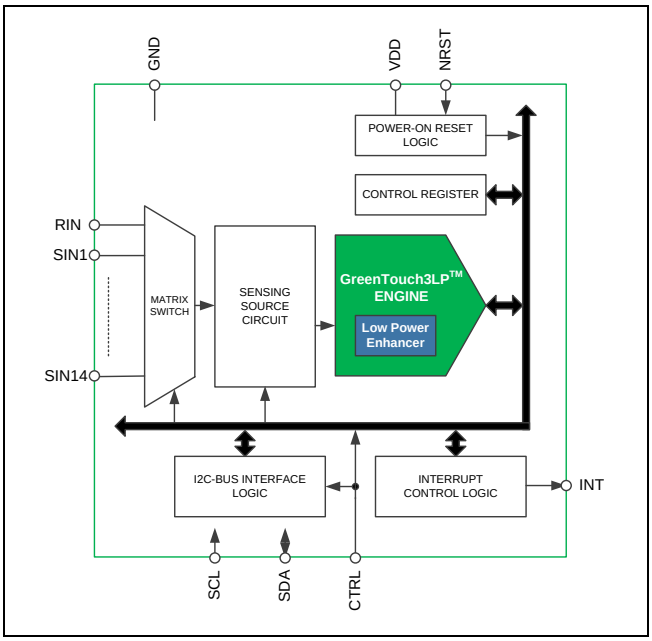
1. INTRODUCTION

The GTX314L is one of the GreenTouch3LP™ capacitive touch sensor series. Especially the GTX314L can do capacitance sensing with 14 channels under above GreenTouch3LP™ engine operation. Thanks to the GreenTouch3LP™ low power engine, a variety of battery powered applications can increase product usage time. Also based on the technology of the existing GreenTouch3™ engine, reliability can be secured against various noise and environmental changes.
The internal control registers are readable and writable using I2C interface.
The GTX314L can be applied under wide supply voltage range from 1.8V to 5.5V. The CTRL pin of the GTX314L provides switchable chip ID that make a couple of chip parallel operations on the same I2C bus.

2. FEATURES

- 14 channels cap. sensing input
- Embedded GreenTouch3LP™ Engine
  - Analog compensation circuit
  - Embedded digital noise filter
  - Intelligent sensitivity calibration
  - Low power enhancer
- I2C interface support
- Provide interrupt function
- Provide slide mode
- Provide “REGISTER WRITING LOCK” function
- Wide supply voltage range: 1.8V to 5.5V
  - Single supply operation
- Package type
  - QFN-24L (4.00x4.00x0.75,e=0.50)
- RoHS compliant

3. BLOCK DIAGRAM



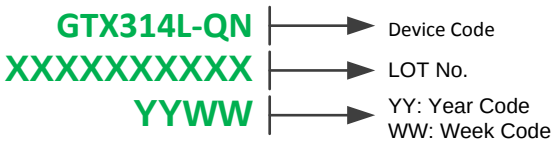
4. APPLICATIONS

- Multi key application – Door lock, Remote controller and Etc.
- Portable Electronics - Mobile phone, MP3, PMP, PDA, Navigation, Digital Camera, Video Camera and Etc.
- Multimedia Devices - Digital photo frame, Home theater system and Etc.

5. ORDERING INFORMATION

Part No.	Package
GTX314L-QN	QFN-24L (4.00x4.00x0.75,e=0.50)

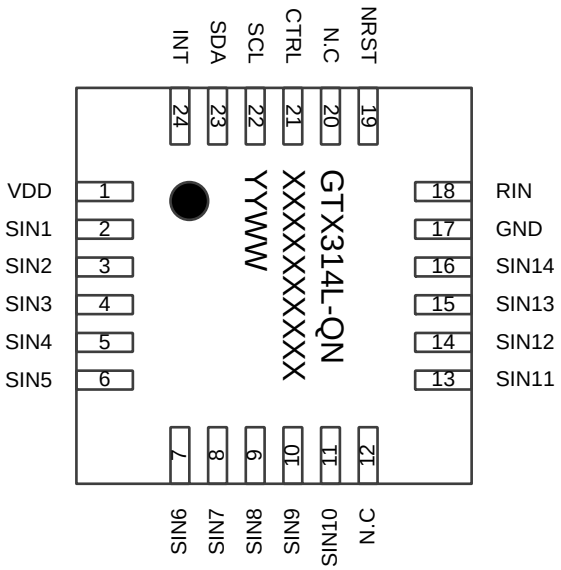
6. MARKING INFORMATION



7. PIN DESCRIPTION

This section describes the pin names and pin functions of GTX314L. Pinout configuration also illustrated as below. The GTX314L device is available in the following packages.

7.1 PACKAGE INFORMATION (QFN-24L PACKAGE)



(TOP view)

7.2 PIN CONFIGURATION

No.	Name	Type	Description
1	VDD	PWR	Supply Voltage
2	SIN1	AO	Channel 1: Touch sensing input
3	SIN2	AO	Channel 2: Touch sensing input
4	SIN3	AO	Channel 3: Touch sensing input
5	SIN4	AO	Channel 4: Touch sensing input
6	SIN5	AO	Channel 5: Touch sensing input
7	SIN6	AO	Channel 6: Touch sensing input
8	SIN7	AO	Channel 7: Touch sensing input
9	SIN8	AO	Channel 8: Touch sensing input
10	SIN9	AO	Channel 9: Touch sensing input
11	SIN10	AO	Channel 10: Touch sensing input
12	N.C	-	-
13	SIN11	AO	Channel 11: Touch sensing input
14	SIN12	AO	Channel 12: Touch sensing input
15	SIN13	AO	Channel 13: Touch sensing input
16	SIN14	AO	Channel 14: Touch sensing input
17	GND	GND	Ground connection
18	RIN	AO	Capacitance reference input
19	NRST	DI	Reset control pin (Active LOW)
20	N.C	-	-
21	CTRL	AO/DI	CTRL Option (Refer to CTRL OPTION SELECTION)
22	SCL	DI	I2C serial clock input
23	SDA	DIO	I2C serial data communication pin
24	INT	DO	Interrupt output pin

NOTE: DI: Digital Input, DO: Digital Output, DIO: Digital Input and Output, AI: Analog Input, AO: Analog Output, PWR: POWER

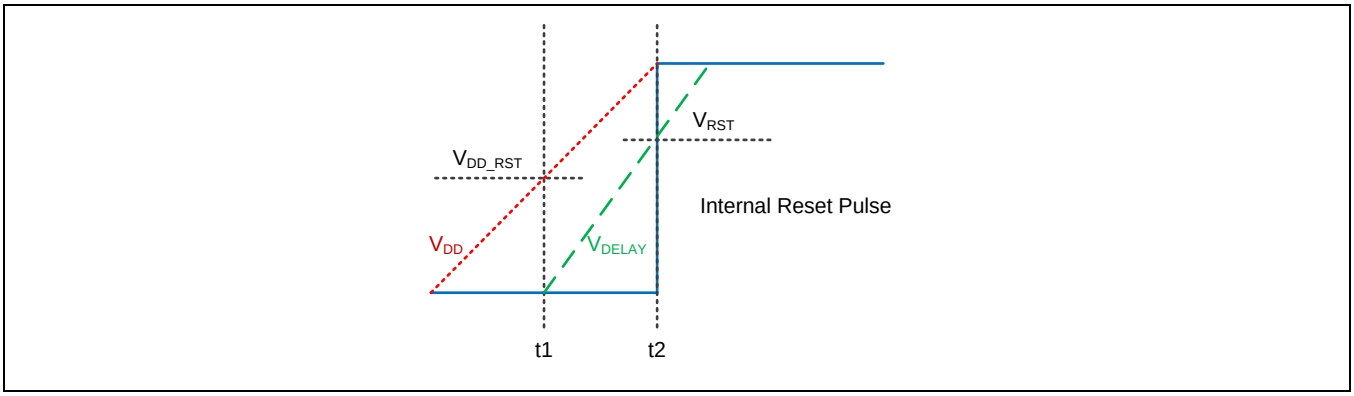
8. FUNCTION DESCRIPTION

8.1 INTERNAL AND EXTERNAL RESET (NRST)

The GTX314L has both internal power-on reset and external reset functions. The internal reset operation is used for initial power-on reset and the external reset operation is done by NRST pin.

Low pulse signal by NRST pin is for an abrupt reset which is required for intensive system reset. The NRST pin might be floating and no external reset components are required when the external reset is not in use.

The internal power reset sequence is represented as below.



The internal V_{DELAY} voltage starts to rise when VDD come up to V_{DD_RST} level. The internal reset pulse is maintained as low between t1 and t2. During this low pulse period, the internal power reset operation is finished. Every time when VDD drops under V_{DD_RST} internal reset block makes V_{DELAY} signal low and then internal reset pulse drops to low. By above internal reset operation sequence GTX314L gets more certain and more correct power reset function than any others.

The external reset using NRST pin is activated during low input pulse. The intensive system reset can be easily obtained by this low pulse input to the NRST pin. More than 10usec low pulse period is required for proper reset. Because NRST pin has an internal pull-up resistor (typical value is 30KΩ), the NRST pin might be floating.

8.2 IMPLEMENTATION FOR TOUCH SENSING (SIN1 ~ SIN14, RIN)

SIN inputs (SIN1~SIN14) and RIN input are used for touch detection of capacitance variation sensing. The SIN input pins are connected to touch sensing pad and catches capacitance variation caused by direct touch or approach. And RIN input for the reference capacitance is connected to a capacitor and resistor to compensate capacitance difference between SIN inputs and RIN input. The GTX314L compares each capacitance of SIN input and that of RIN input and determines touch detection of each channel when capacitance of each SIN input increases. So, for correct capacitance comparison between SIN inputs and RIN input, approximately equal initial-steady state capacitance between SIN inputs and RIN input are recommended. User can compensate initial-steady state capacitance difference between SIN inputs and RIN input by adding capacitor to RIN pin.

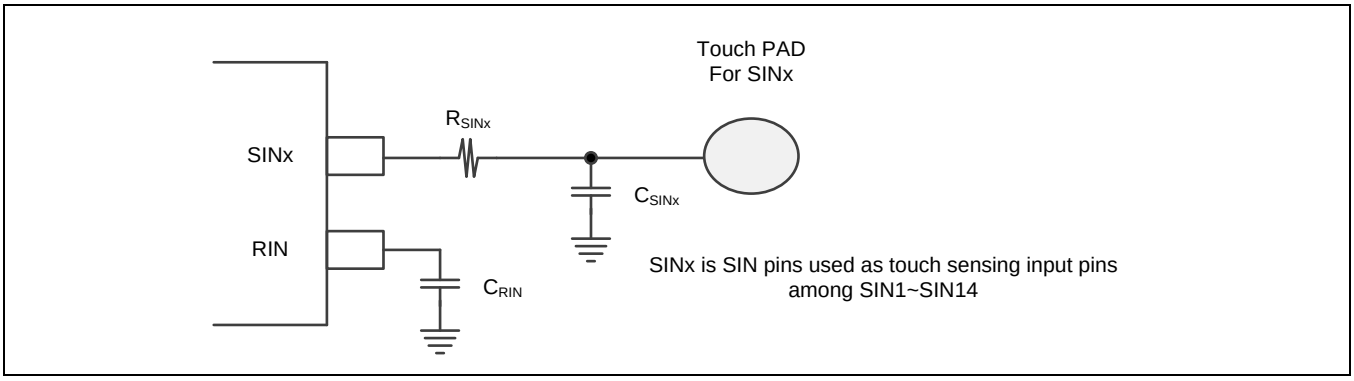
The GTX314L also has various intelligent sensing functions to determine valid touch from error or sensitivity problems caused by various environmental noise effects. These advanced sensing methods will help making faultless touch key systems under the worst conditions.

The internal intelligent sensitivity adjustment algorithm removes sensitivity rolling caused by system noise, circuit deviation, and circumstantial drift. The GTX314L has a special noise elimination filter for more powerful noise rejection and it will be very helpful for proper touch operation even if the system operates under deteriorative environment conditions.

The GTX314L SIN inputs have an internal series resistor for ESD protection. The additional external series resistors are profitable for prevention of abnormal actions caused by radiation noise or electrical surge pulse. In any case, if the additional external series resistor ($R_{SIN1~14}$) of each SIN input is required, then it should be less than 1.5KΩ to SIN and the location of resister is recommended as closer to the SIN pins. For $C_{SIN1~14}$, C_{RIN} capacitor, less than 50pF capacitor can be used.

The SIN input routing lines are desirable to be routed as short as possible and the width of routing lines should be as narrow as possible and should be placed on bottom metal. In other words, a touch PAD and other parts should be placed on different metal each other. The additional extension line pattern of RIN input on application PCB can help prevention of abnormal actions caused by radiation noise, but excessive long RIN input line can be a reason for failure of touch detect. The SIN inputs and RIN input lines are desirable to be routed as far as possible from impedance varying path such as LED drive current path. All touch sensing pads are recommended to be surrounded by GND pattern in order to reduce noise influence.

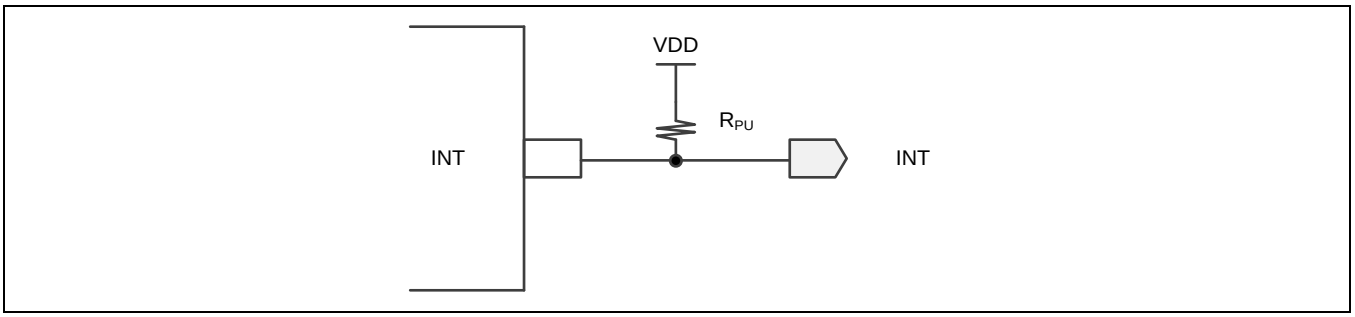
Implementation circuit for SIN pins and RIN pin is shown in the following figure.



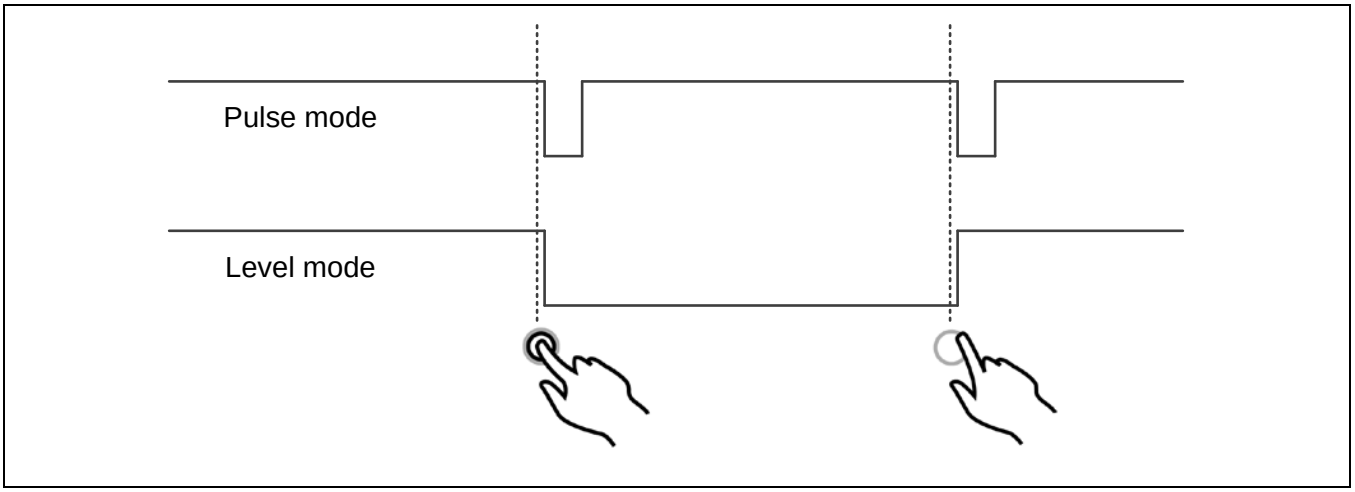
8.3 IMPLEMENTATION FOR INTERRUPT (INT)

The GTX314L provides an interrupt (INT) function to reduce a communication load between MCU and GTX314L. The INT will indicate a point of time that the output status registers at the address 02h and 03h changes and MCU needs to read it. The INT pin has an open drain NMOS structure hence a couple of kΩ pull-up resistor must be required.
(See register address 10h = INT_MODE)

The basic implementations for active low modes are shown in the following figure.



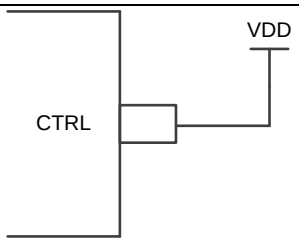
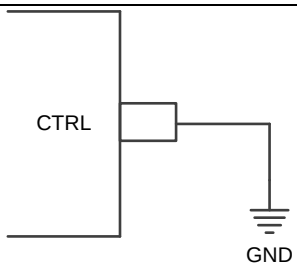
Two interrupt mode operations are shown in the following figure.



8.4 CTRL OPTION SELECTION (CTRL)

In the GTX314L, three options are available by CTRL pin connection. Each option and its connections are shown in the table and figures below. This CTRL pulse signal starts at internal power reset time and finishes after a few operation period and options setting. For more detail sensitivity adjustment, C_{SIN} capacitors should be used.

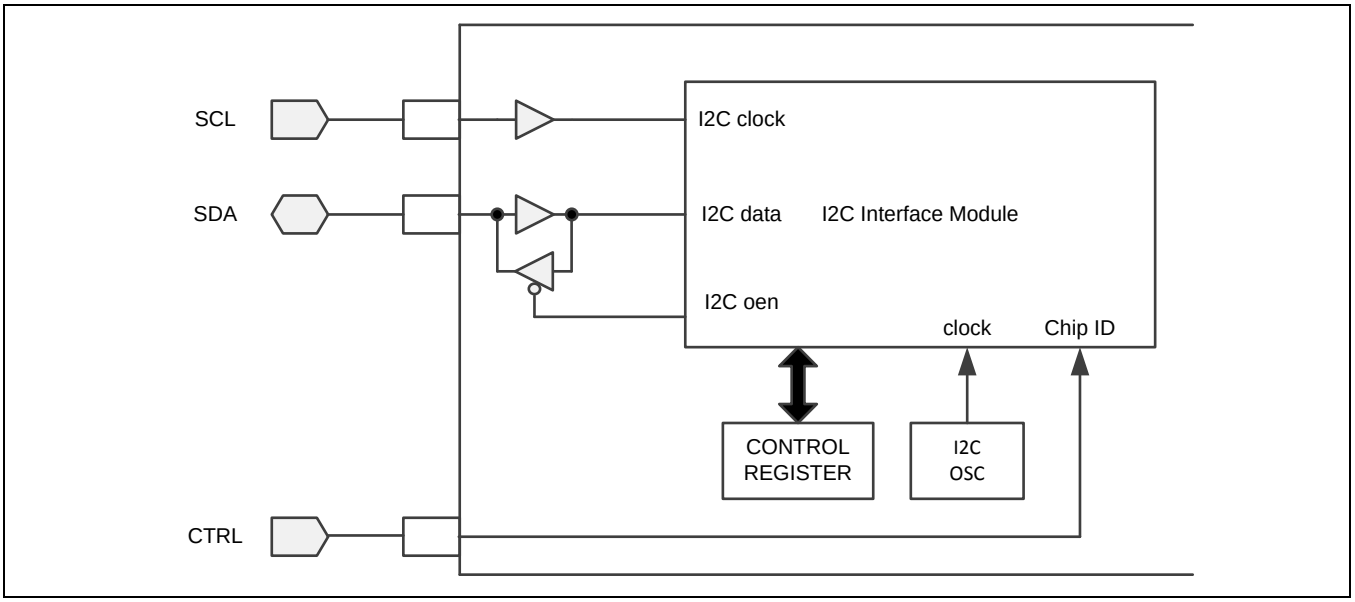
Each options and respective connection are shown in the following table.

CTRL Option	 Option 1 (Connect to VDD)	 Option 3 (Connect to GND)
I2C Address	B6h	B0h

8.5 I2C INTERFACE (SCL, SDA, CTRL)

The I2C-bus is for 2-way, 2-line communication between different ICs or modules. The serial bus consists of two bidirectional lines; one for data signals (SDA), and one for clock signals (SCL).
Both the SDA and SCL lines be connected to a positive supply voltage via a internal pull-up resistor (typical 10kΩ) to prevent open gate leakage current in input mode. But the lines must be connected to a positive supply voltage via a pull-up additional external resistor.
The internal oscillator is disabled when all of both the SDA and SCL lines are high for saving current consumption.

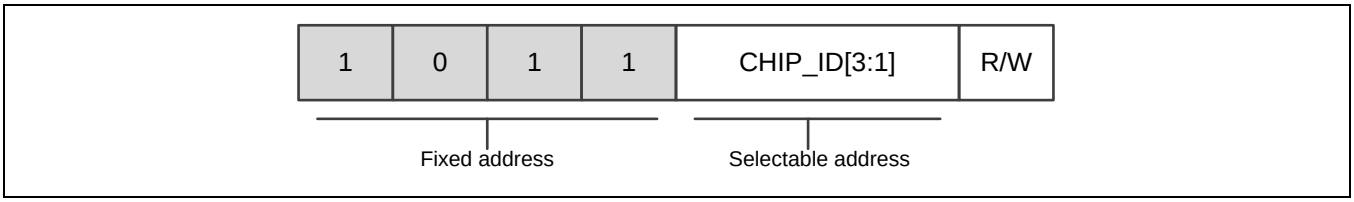
The simple internal block diagram for SCL and SDA is shown in the following figure.



8.5.1 DEVICE ADDRESSING

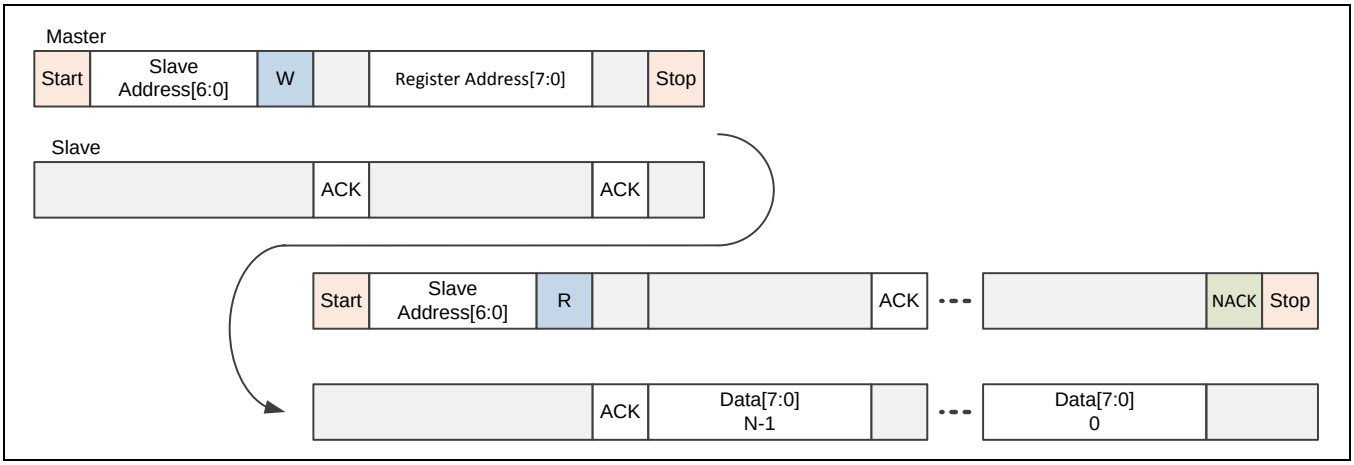
Following a START condition, the bus master must output the address of the slave it is accessing. To conserve power, no internal pull-up resistors are incorporated on the hardware selectable pins(CTRL) and it must be connected to VDD or GND.
The last bit of the slave address defines the operation to be performed. When set to logic 1, a read operation is selected, while a logic 0 selects a write operation.

The following figure represents the I2C slave address map.



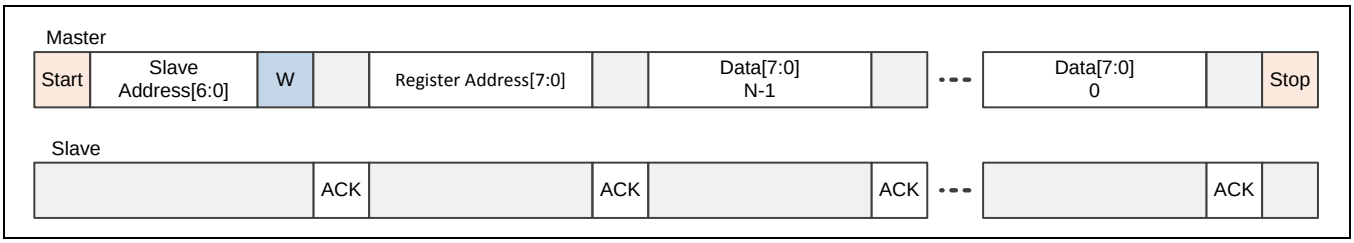
8.5.2 READ OPERATION

The following figure represents the I2C normal mode read operation.



8.5.3 WRITE OPERATION

The following figure represents the I2C normal mode write operation.



9. REGISTER DESCRIPTION

9.1 QUICK REGISTER MAP

Address	R/W	Reset Value	Data							
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h										
01h	R/W	B6h B0h	1	0	1	1	CHIP_ID[3:1]			0
02h	R	-	TOUCH_ OUT8	TOUCH_ OUT7	TOUCH_ OUT6	TOUCH_ OUT5	TOUCH_ OUT4	TOUCH_ OUT3	TOUCH_ OUT2	TOUCH_ OUT1
03h	R	-	0	0	TOUCH_ OUT14	TOUCH_ OUT13	TOUCH_ OUT12	TOUCH_ OUT11	TOUCH_ OUT10	TOUCH_ OUT9
04h	R/W	FFh	SIN8_ CH_EN	SIN7_ CH_EN	SIN6_ CH_EN	SIN5_ CH_EN	SIN4_ CH_EN	SIN3_ CH_EN	SIN2_ CH_EN	SIN1_ CH_EN
05h	R/W	3Fh	0	0	SIN14_ CH_EN	SIN13_ CH_EN	SIN12_ CH_EN	SIN11_ CH_EN	SIN10_ CH_EN	SIN9_ CH_EN
06h										
07h										
08h										
09h										
0Ah	R/W	31h	0	0	1	1	0	0	0	MON_ RST
0Bh	R/W	00h	0	0	0	0	0	0	0	SOFT_ RST
0Ch	R/W	00h	0	0	0	0	0	0	0	I2C_ PU_DIS
0Dh										
0Eh										
0Fh	R/W	5Ah	REGISTER_WRITE_LOCK							

NOTE: The blank register is assigned FFh data.

Address	R/W	Reset Value	Data							
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
10h	R/W	11h	0	0	0	INT_ MODE	0	0	0	MULTI_ MODE
11h	R/W	32h	0	EXP_TIME			0	0	EXP_EN	EXP_ MODE
12h										
13h	R/W	0Ah	0	0	0	0	CAL_TIME			
14h	R/W	00h	0	0	0	0	SEN_IDLE_TIME			
15h	R/W	01h	0	0	0	0	SEN_IDLE_TIME_SUFFIX			
16h										
17h	R/W	03h	0	0	0	0	0	BUSY_TO_IDLE_TIME		
18h	R/W	00h	0	0	0	0	0	0	0	I2B_ MODE
19h	R/W	00h	0	0	0	0	0	0	0	SLIDE _MODE
1Ah										
1Bh										
1Ch										
1Dh										
1Eh										
1Fh										

NOTE: The blank register is assigned FFh data.

Address	R/W	Reset Value	Data							
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
20h	R/W	0Fh	0	0	SENSITIVITY1					
21h			0	0	SENSITIVITY2					
22h			0	0	SENSITIVITY3					
23h			0	0	SENSITIVITY4					
24h			0	0	SENSITIVITY5					
25h			0	0	SENSITIVITY6					
26h			0	0	SENSITIVITY7					
27h			0	0	SENSITIVITY8					
28h			0	0	SENSITIVITY9					
29h			0	0	SENSITIVITY10					
2Ah			0	0	SENSITIVITY11					
2Bh			0	0	SENSITIVITY12					
2Ch			0	0	SENSITIVITY13					
2Dh			0	0	SENSITIVITY14					
2Eh										
2Fh										

NOTE: The blank register is assigned FFh data.

9.2 REGISTER CONFIGURATION

9.2.1 01H REGISTER

Address	R/W	Reset Value	Data							
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
01h	R/W,		1	0	1	1	CHIP_ID[3:1]			0
		B6h(1)	1	0	1	1	0	1	1	0
		B0h(3)	1	0	1	1	0	0	1	0

CHIP_ID[3:1]	Hardware selectable chip ID bit
	CTRL pin = VDD, CHIP_ID[3:1] = 011 CTRL pin = GND, CHIP_ID[3:1] = 000
	NOTE: This bit might be controlled by CTRL pin.

NOTE: (1) CTRL pin = VDD, (2) CTRL pin = GND

9.2.2 02H, 03H REGISTER

Address	R/W	Reset Value	Data							
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
02h	R	-	TOUCH_OUT8	TOUCH_OUT7	TOUCH_OUT6	TOUCH_OUT5	TOUCH_OUT4	TOUCH_OUT3	TOUCH_OUT2	TOUCH_OUT1
03h	R	-	0	0	TOUCH_OUT14	TOUCH_OUT13	TOUCH_OUT12	TOUCH_OUT11	TOUCH_OUT10	TOUCH_OUT9

TOUCH_OUTn(1)	Each of SIN touch detection status bit 0 = No touch detection 1 = Touch detection.
	NOTE: It's set '1' when touch detection occur.

NOTE: (1) n = SIN1~SIN14 pin

9.2.3 04H, 05H REGISTER

Address	R/W	Reset Value	Data							
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
04h	R/W		SIN8_ CH_EN	SIN7_ CH_EN	SIN6_ CH_EN	SIN5_ CH_EN	SIN4_ CH_EN	SIN3_ CH_EN	SIN2_ CH_EN	SIN1_ CH_EN
		FFh	1	1	1	1	1	1	1	1
05h	R/W		0	0	SIN14_ CH_EN	SIN13_ CH_EN	SIN12_ CH_EN	SIN11_ CH_EN	SIN10_ CH_EN	SIN9_ CH_EN
		3Fh	0	0	1	1	1	1	1	1

SINn(1)_CH_EN	Each of channel(SIN1~14) enable/disable bits 0 = disable 1 = enable
	NOTE: It's configured with the new offset when the SINn(1)_CH_EN bit is enabled.

NOTE: (1) n = SIN1~SIN14 pin

9.2.4 0AH REGISTER

Address	R/W	Reset Value	Data							
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Ah	R/W		0	0	0	0	0	0	0	MON_RST
		31h	0	0	1	1	0	0	0	1

MON_RST	Internal and external reset monitoring bit 0 = not active and clear bit by user 1 = active and set bit by GTX314L
	NOTE: It's set '1' when GTX314L is reset.

9.2.5 0BH REGISTER

Address	R/W	Reset Value	Data							
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Bh	R/W		0	0	0	0	0	0	0	SOFT_RST
		00h	0	0	0	0	0	0	0	0

SOFT_RST	Soft reset bit 0 = Operation mode 1 = Sleep mode.
	NOTE: Current consumption can be saved and Touch engine is not work in sleep mode. **NOTE:** It's configured with the new offset when the SOFT_RST bit is changed from sleep mode to operation mode. **NOTE:** All the value of register are not changed by SOFT_RST bit.

9.2.6 0CH REGISTER

Address	R/W	Reset Value	Data							
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Ch	R/W		0	0	0	0	0	0	0	I2C_ PU_DIS
		00h	0	0	0	0	0	0	0	0

I2C_PU_DIS	I2C pull-up control bit 0 = I2C pull-up enable 1 = I2C pull-up disable

9.2.7 0FH REGISTER

Address	R/W	Reset Value	Data							
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Fh	R/W		REGISTER_WRITE_LOCK							
		5Ah	0	1	0	1	1	0	1	0

REGISTER_WRITE_LOCK	Register write lock bit 5Ah = All of registers can be read and write. Other = All of registers are locked. But it's possible to read registers.
	NOTE: When I2C is not used to write operation, it is recommended to prevent the write operation by using the "REGISTER_WRITE_LOCK" function.

9.2.8 10H REGISTER

Address	R/W	Reset Value	Data							
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
10h	R/W		0	0	0	INT_ MODE	0	0	0	MULTI_ MODE
		11h	0	0	0	1	0	0	0	1

INT_MODE	Interrupt operation mode selection bit 0 = Pulse mode. 1 = Level mode.
MULTI_MODE	Touch engine mode selection bit 0 = Single touch mode 1 = Multi touch mode.

9.2.9 11H REGISTER

Address	R/W	Reset Value	Data							
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
11h	R/W		0	EXP_TIME			0	0	EXP_EN	EXP_ MODE
		32h	0	0	1	1	0	0	1	0

EXP_TIME(1)	Touch expire time selection bit	
	000 = 5sec 001 = 10sec 010 = 15sec 011 = 20sec	100 = 25sec 101 = 30sec 110 = 35sec 111 = 40sec
EXP_EN	Touch expire enable bit 0 = disable 1 = enable	
	NOTE: It's configured with the new offset when the touch expire function is executed.	
EXP_MODE	Touch expire mode bit 0 = expire count is not restarted whenever a different touch occurs 1 = expire count is restarted if a different touch occur	

NOTE: (1) Test condition: VDD = 3.0V, TA = 25℃

9.2.10 13H REGISTER

Address	R/W	Reset Value	Data							
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
13h	R/W		0	0	0	0	CAL_TIME			
		0Ah	0	0	0	0	1	0	1	0

CAL_TIME(1)	Calibration time selection bit	
	0000 = 0msec + 1 period	1000 = 800msec + 1 period
	0001 = 100msec + 1 period	1001 = 900msec + 1 period
	0010 = 200msec + 1 period	1010 = 1000msec + 1 period
	0011 = 300msec + 1 period	1011 = 1100msec + 1 period
	0100 = 400msec + 1 period	1100 = 1200msec + 1 period
	0101 = 500msec + 1 period	1101 = 1300msec + 1 period
	0110 = 600msec + 1 period	1110 = 1400msec + 1 period
	0111 = 700msec + 1 period	1111 = No Calibration
	NOTE: (1) The calibration time to protect from environmental change (2) Deviation : ±30% (@5.0V)	

NOTE: (1) Test condition: VDD = 3.0V, TA = 25℃

9.2.11 14H REGISTER

Address	R/W	Reset Value	Data							
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
14h	R/W		0	0	0	0	SEN_IDLE_TIME			
		00h	0	0	0	0	0	0	0	0

SEN_IDLE_TIME(1)	Idle time section bit			
	0000= 1msec	0100= 400msec	1000= 800msec	1100= 1200msec
	0001= 100msec	0101= 500msec	1001= 900msec	1101= 1300msec
	0010= 200msec	0110= 600msec	1010= 1000msec	1110= 1400msec
	0011= 300msec	0111= 700msec	1011= 1100msec	1111= 1500msec
	NOTE: The idle time equation is as follows. IDLE_TIME = SEN_IDLE_TIME[3:0] + SEN_IDLE_TIME_SUFFIX[3:0] Ex> 110msec = 100msec + 10msec			

NOTE: (1) Test condition: VDD = 3.0V, TA = 25℃

9.2.12 15H REGISTER

Address	R/W	Reset Value	Data							
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
15h	R/W		0	0	0	0	SEN_IDLE_TIME_SUFFIX			
		01h	0	0	0	0	0	0	0	1

SEN_IDLE_TIME_SUFFIX(1)	Idle time suffix section bit			
	0000= 0msec	0100= 40msec	1000= 80msec	1100= 120msec
	0001= 10msec	0101= 50msec	1001= 90msec	1101= 130msec
	0010= 20msec	0110= 60msec	1010= 100msec	1110= 140msec
	0011= 30msec	0111= 70msec	1011= 110msec	1111= 150msec
	NOTE: The idle time equation is as follows. IDLE_TIME = SEN_IDLE_TIME[3:0] + SEN_IDLE_TIME_SUFFIX[3:0] Ex> 110msec = 100msec + 10msec			

NOTE: (1) Test condition: VDD = 3.0V, TA = 25℃

9.2.13 17H REGISTER

Address	R/W	Reset Value	Data							
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
17h	R/W		0	0	0	0	0	BUSY_TO_IDLE_TIME		
		03h	0	0	0	0	0	0	1	1

BUSY_TO_IDLE_TIME(1)	Busy to Idle time selection bit	
	000 = 0sec (disable)	100= 4sec
	001 = 1sec	101= 5sec
	010 = 2sec	110= 6sec
	011 = 3sec	111= 7sec

NOTE: (1) Test condition: VDD = 3.0V, TA = 25℃

9.2.14 18H REGISTER

Address	R/W	Reset Value	Data							
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
18h	R/W		0	0	0	0	0	0	0	I2B_ MODE
		00h	0	0	0	0	0	0	0	0

I2B_MODE	Idle to busy mode control bit 0 = auto mode 1 = manual mode

9.2.15 19H REGISTER

Address	R/W	Reset Value	Data							
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
19h	R/W		0	0	0	0	0	0	0	SLIDE _MODE
		00h	0	0	0	0	0	0	0	0

SLIDE_MODE	Slide mode enable bit 0 = disable 1 = enable

9.2.16 20H~2DH REGISTER

Address	R/W	Reset Value	Data							
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
20h ~ 2Dh	R/W		0	0	SENSITIVITY1					
			0	0	SENSITIVITY2					
			0	0	SENSITIVITY3					
			0	0	SENSITIVITY4					
			0	0	SENSITIVITY5					
			0	0	SENSITIVITY6					
			0	0	SENSITIVITY7					
			0	0	SENSITIVITY8					
			0	0	SENSITIVITY9					
			0	0	SENSITIVITY10					
			0	0	SENSITIVITY11					
			0	0	SENSITIVITY12					
			0	0	SENSITIVITY13					
			0	0	SENSITIVITY14					
		0Fh	0	0	0	0	1	1	1	1

SENSITIVITYn(1)	Touch sensitivity control bit 03h = Very high sensitive 3Fh = Very high insensitive
	NOTE: It's recommended to use 0Ch~3Fh values at the sensitivity setting.

NOTE: (1) n = SIN1~SIN14 pin

10. ELECTRICAL CHARACTERISTICS

10.1 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Min	Typ.	Max	Units
Maximum supply voltage	V_{DD_MAX}		-0.3		6.0	V
Supply voltage range(1)	V_{DD_RNG}		-0.3		6.0	V
Voltage on any input pin	V_{IN_MAX}		-0.3		VDD +0.3	V
Maximum current into any pin	I_{MIO}		-100		100	mA
Power dissipation	P_{MAX}		-		800	mW
Storage temperature	T_{STG}		-65		150	℃
Operating humidity	H_{OP}	8 hours	5		95	%
Operating temperature	T_{OPR}		-40		85	℃
Junction temperature	T_J		-40		125	℃

NOTE: (1) This is the real valid power supply voltage range considering allowable supply tolerance. It cannot be used as target supply voltage range which is separately presented at below I/O ELECTRICAL CHRACTERISTICS.

10.2 I/O ELECTRICAL CHARACTERISTICS

This section includes information about power supply requirements and I/O pin characteristics.

(TA = -25 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Target supply voltage	V_{DD}		1.8	3.0 / 5.0	5.5	V
Current consumption	I_{DD} (VDD=3.0V)	Standby mode @IDLE_TIME=200msec(1) @SENSING_CNT=3,000cnt(2)	-	18	-	uA
		Standby mode @IDLE_TIME=200msec(1) @SENSING_CNT=2,000cnt(3)	-	16	-	uA
	I_{DD} (VDD=5.0V)	Standby mode @IDLE_TIME=200msec(1) @SENSING_CNT=3,000cnt(2)	-	32	-	uA
		Standby mode @IDLE_TIME=200msec(1) @SENSING_CNT=2,000cnt(3)	-	29	-	uA
Input high voltage	V_{IH}	All input pins	0.7VDD	-	VDD + 0.3	V
Input low voltage	V_{IL}	All input pins	-0.3	-	0.3VDD	V
Output low voltage	V_{VOL}	All output pins (I_{OL}= 10mA, VDD = 5.0V)	-	-	0.4	V
Output sink current(4)	I_{SINK}	All output pins (Active low)	-	-	10	mA
Output high leakage current	I_{LOH}		-	-	1	uA

NRST internal pull-up resister(4)	R_{PU_RST}		-	30	-	kΩ
SDA Internal Pull-up Resister(4)	R_{PU_SDA}		-	30	-	kΩ
SCL Internal Pull-up Resister(4)	R_{PU_SCL}		-	30	-	kΩ

NOTE:

(1) refer to address=14h(SEN_IDLE_TIME) and address=15h(SEN_IDLE_TIME_SUFFIX) registers

(2) SENSING_CNT=3,000cnt register configuration

address 40h=04h, address 41h=02h, address 42h=02h, address 43h=01h

address 44h=00h, address 45h=03h, address 46h=00h, address 47h=00h

(3) SENSING_CNT=2,000cnt register configuration

address 40h=02h, address 41h=01h, address 42h=01h, address 43h=00h

address 44h=02h, address 45h=03h, address 46h=00h, address 47h=02h

(4) Test condition: VDD = 3.0V, TA = 25℃ and normal operation mode under default control register value. (Unless otherwise noted)

10.3 RESET CHARACTERISTICS

(TA = -25 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
NRST input high width	t_{RST}		10	-	-	usec
POR(1) Time	t_{POR}		-	-	600	usec
POR voltage	V_{POR}		-	1.5	-	V

NOTE: (1) POR = Internal Power-On Reset

10.4 INTERRUPT OUTPUT CHARACTERISTICS

(TA = -25 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
INT low pulse width	t_{INT}		-	5	-	msec

10.5 SENSING INPUT CHARACTERISTICS

(TA = -25 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Minimum detectable input capacitance variant	ΔC_{S_MIN}		0.1	-	-	pF
Maximum input external capacitance	C_{EXT_MAX}		-	-	50	pF
Sensitivity selection steps	N_{SEN}		-	55	-	step
Sense OSC internal series resistor	R_{INT}		-	140	-	Ω
external SIN series resistor	R_{EXT_SIN}		-	560	1.5K	Ω

10.6 SYSTEM CHARACTERISTICS

(TA = -25 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Time for stable I2C communication after reset	t_{I2C}		1	-	-	msec
Time for stable Touch Operating after Reset	t_{OP}		500	-	-	msec
Touch On response time	t_{ON}	1 channel Touch at all of register default	-	80	-	msec

10.7 I2C INTERFACE TIMING CHARACTERISTICS

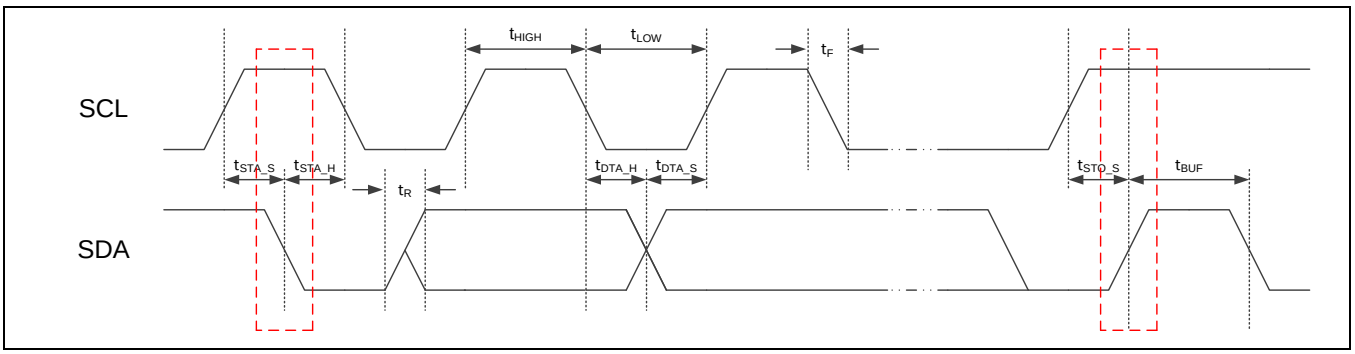
(TA = -25 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Standard-mode		Fast-mode		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}	-	100	-	400	kHz
Hold time for START condition	t_{STA_H}	4.0	-	0.6	-	usec
LOW period of the SCL clock	t_{LOW}	4.7	-	1.3	-	usec
HIGH period of the SCL clock	t_{HIGH}	4.0	-	0.7	-	usec
Set-up time for START condition	t_{STA_S}	4.7	-	0.6	-	usec
Data hold time	t_{DAT_H}	5	-	40	-	nsec
Data set-up time	t_{DAT_S}	250	-	100	-	nsec
Rise time of both SDA and SCL signals	t_R	-	1000	20 + 0.1 C_b (2)	300	nsec
Fall time of both SDA and SCL signals	t_F	-	300	20 + 0.1 C_b (2)	300	nsec
Set-up time for STOP condition	t_{STO_S}	4.0	-	0.6	-	usec
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	1.3	-	usec
Capacitive load for each bus line	Cb	-	400		400	pF

NOTE:

(1) All values referred to VIH and VIL levels (please refer to I/O ELECTRICAL CHRACTERISTICS).

(2) C_b = total capacitance of one bus line in pF.



10.8 ESD CHARACTERISTICS

Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage. During the device qualification, ESD stresses were performed for the Human Body Model (HBM), the Machine Model (MM) and the Charge Device Model (CDM).

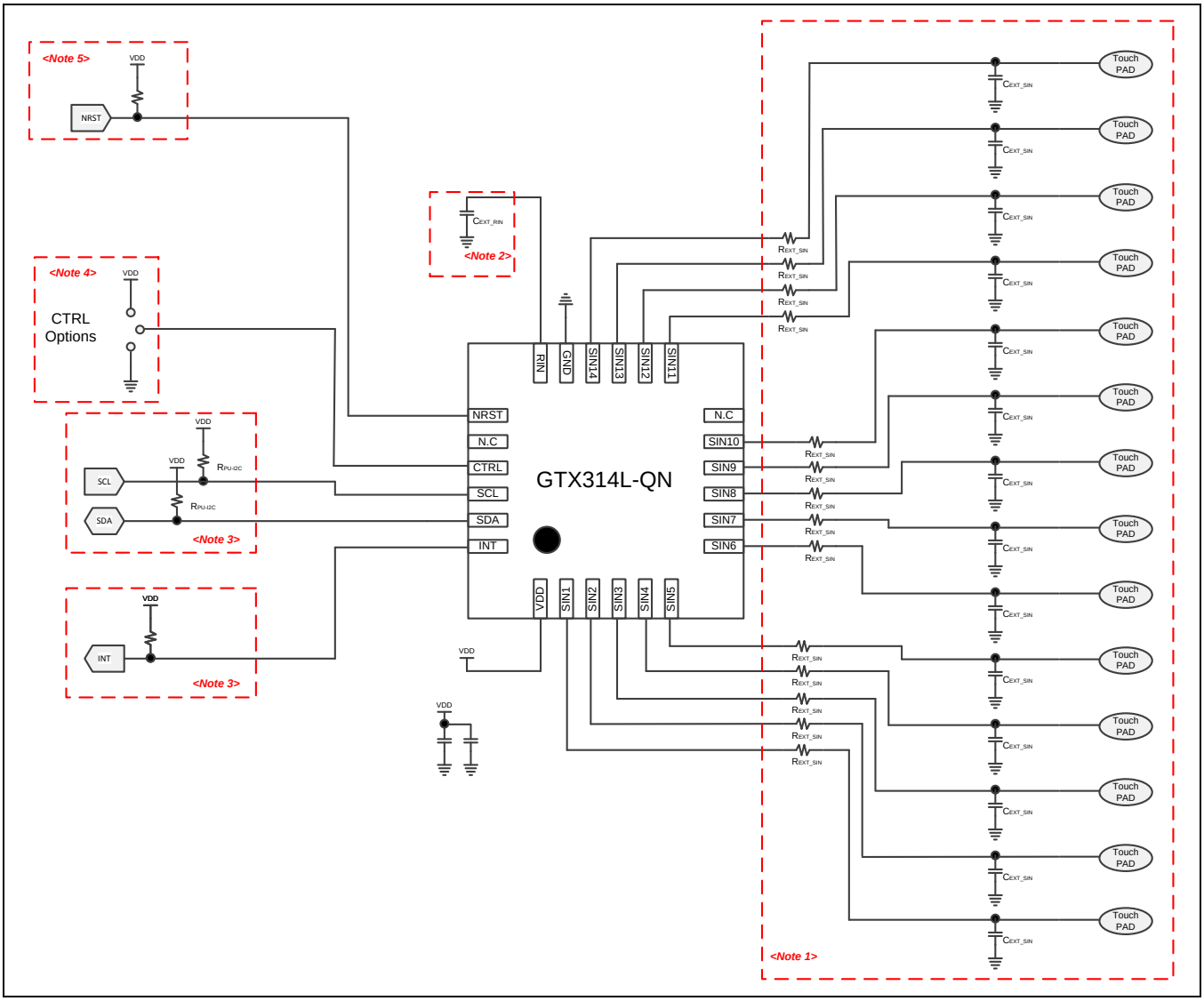
Test Mode	Symbol	Test Pin (Reference)	Max	Unit	Reference Document
Human body model (HBM)	V_{HBM}	VSS, I/O (VDD)	±8000	V	JS-001-2014
		VDD, I/O (VSS)	±8000	V	
		Every I/O (All I/O)	±8000	V	
Machine model (MM)	V_{MM}	VSS, I/O (VDD)	±600	V	JESD22-A115C :2010
		VDD, I/O (VSS)	±800	V	
		Every I/O (All I/O)	±700	V	
Charge device model (CDM)	V_{CDM}	Every Pin	±2000	V	JESD22-C101F :2013

10.9 LATCH-UP CHARACTERISTICS

Test Type	Symbol	Polarity	Max	Unit	Reference Document
I test	I_{LAT_POS}	Positive	200	mA	JESD78E :2016
	I_{LAT_NEG}	Negative	200	mA	
V_{supply} over V_{DD_MAX}	V_{LAT_POS}	Positive	8.25	V	

11. APPLICATION

11.1 EXAMPLE CIRCUIT (QFN-24L PACKAGE)



NOTE: R_{EXT_SIN} = 560Ω (recommend), R_{PU_I2C} = 10KΩ (recommend)
C_{EXT_RIN} = 4pF (recommend)

NOTE: The values of resistance and capacitance can be changed depending on the application set.

NOTE: It is recommended to make empty space on PCB artwork for install the capacitance later, currently even if the capacitance is not needed on the SIN ports.

11.2 APPLICATION NOTES

Normally a touch sensing operation is ultimately impedance variation sensing. Hence a touch sensing system is recommended to be taken care of prevention of the external sensing disturbance. Although the GTX314L has enough noise rejection algorithms and various protection circuits to prevent error touch detection caused by noise and incapable sensing, it is better to take care in noisy applications such as home appliances. There are many measurable or invisible noises in system that can affect the impedance sensing signal or distort that signal. The main principal design issues and required attentions are such as below.

- **Power Line**
  - The touch sensor power line is recommended to be split from the other power lines such as relay circuits or LED power that can make pulsation noise on power lines.
  - The big inductance that might exist in long power connection line can cause power fluctuation by other noise sources.
  - The lower frequency periodic power noise such as a few Hz ~ kHz has more baneful influence on sensitivity calibration.
  - An extra regulator for touch sensor is desirable for prevention above power line noises.
  - The V_{DD} under shooting pulse less than internal reset voltage (V_{DD_RST}) can cause system reset.
  - The capacitor connected between V_{DD} and GND is somehow obligation element for buffering above power line noises. This capacitor must be placed as near to IC as possible.

- **Sensing (Reference) Input Line for Touch Detect <Note1><Note2>**
  - The sensing lines for touch detection are desirable to be routed as short as possible and the width of routing path should be as narrow as possible.
  - The sensing line for touch detection should be formed by bottom metal, in other words, an opposite metal of a touch PAD.
  - The additional extension line pattern of RIN input on application PCB can help prevention of abnormal actions caused by radiation noise, but excessive long RIN input line can be a reason for failure of touch detect.
  - SIN capacitor is useful for sensitivity reduction adjust. A bigger capacitor of SIN makes sensitivity of corresponding channel to be lower.
  - The sensing line for touch detection is desirable to be routed as far as possible from impedance varying path such as LED drive current path.
  - An unused sensing channel is desirable to be turned off by control register. (Recommendation)

- Additional external series resistors are profitable for prevention of abnormal actions caused by radiation noise or electrical surge pulse. The location of resister is better as near as possible to the SIN and RIN pins for better stable operation.

  (Refer to IMPLEMENTATION FOR TOUCH SENSING)
- All touch sensing pads are recommended to be surrounded by GND pattern to reduce noise influence.
- It is recommended to be same the length and thickness of the SIN pins on PCB artwork.

- **I2C Interface and Interrupt Applications <Note3>**
  - The SCL is I2C clock input pin and SDA is I2C data input/output pin. SCL and SDA have internal optional pull-up resistor. So, when I2C interface is not required, SCL and SDA pins can be floating. For high speed communication, SDA pin needs small pull-up resistor connected to V_{DD} to reduce pulse rising delay.

    (Refer to I2C INTERFACE)
  - INT is for the output signal that indicates changing of sensing output data. This pin is output only pin and has active low function. Because INT pin has open drain structure, pull-up resistor is required for valid output.

    (Refer to IMPLEMENTATION FOR INTERRUPT)

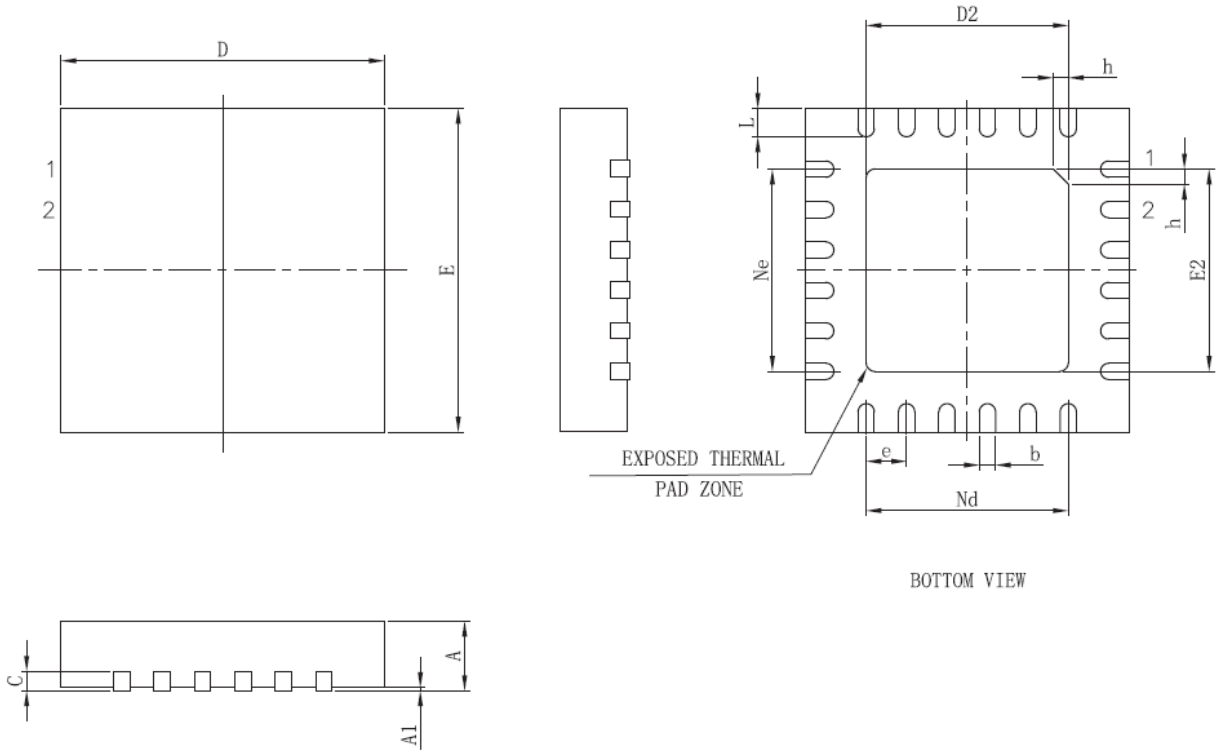
- **CTRL Option Selection <Note4>**
  - Three optional chip ID are available by CTRL pin connection.

    (Refer to CTRL OPTION SELECTION)

- **External Reset <Note5>**
  - The NRST pin is for the abrupt reset input signal. The low signal pulse can make system reset. This pin has also an internal pull-up resistor hence the NRST pin can be floating.

    (Refer to INTERNAL AND EXTERNAL RESET)

12. PACKAGE DIMENSION (QFN-24L PACKAGE)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.40	2.50	2.60
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
E	3.90	4.00	4.10
E2	2.40	2.50	2.60
L	0.35	0.40	0.45
h	0.30	0.35	0.40
L/F载体尺寸	110x110		