NTP8810A

High Performance, High Fidelity Power Driver Integrated Full Digital Audio Amplifier

Datasheet
ver. 1.6

NeoFidelity, Inc.

General Description

The NTP8810A is a single chip full digital audio amplifier including power stage for stereo amplifier system. NTP8810A is integrated with versatile digital audio signal processing functions, high-performance, high-fidelity fully digital PWM modulator and two high-power full-bridge MOSFET power stages.

The NTP8810A receives digital serial audio data with sampling frequency 96kHz, 48kHz, 44.1kHz and 32kHz. It delivers 2 x 15 watts in stereo mode.

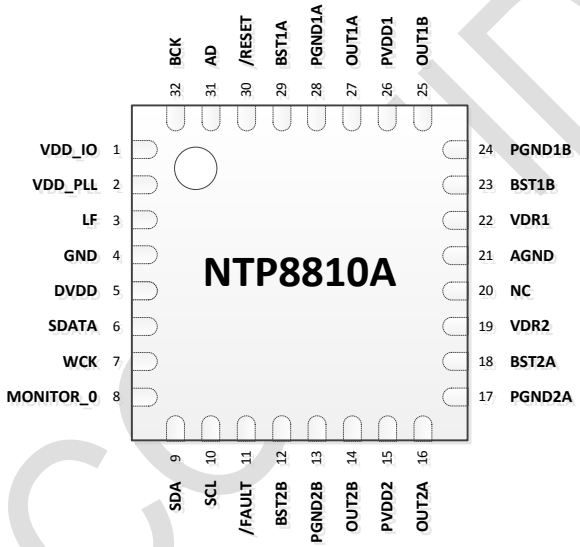
The NTP8810A has a mixer and Bi-Quad filters which can be used to implement the essential audio signal processing functions like, compensation of a loud speaker response and parametric equalization.

All the functions of the NTP8810A can be controlled by internal register values via I^2C host interface bus.

Features

- 2 CH Stereo (15W x 2 BTL @18V, 8Ω)
- SDATA Generator (I^2S output)
- Wide Operating Supply Voltage Range (4.5V to 20V)
- Floating Point Operation
- 28 Programmable Bi-Quad Filters
  - ✓ Speaker Compensation
  - ✓ LPF, HPF, DC Cut
  - ✓ Parametric Equalizer
- 100dB Dynamic Range
- 2 Band Dynamic Range Control
- Protection Circuit
  - ✓ OCP(Over Current Protection)
  - ✓ OTP(Over Temperature Protection)
  - ✓ UVP(Under Voltage Protection)
- High Efficiency
- DC protection
  - ✓ DC cut filter
  - ✓ Coefficient memory Checksum
  - ✓ Modulation Index check

Package



(32 pin SAW QFN 5mm x 5mm Package)

Applications

- LCD/LED/OLED TV or Monitor TV
- Docking Station
- Mini-Component Audio Solution

Ordering Information

Product ID	Package Type	Pin	Size
NTP8810A	SAW QFN	32	5 x 5mm

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1. BLOCK DIAGRAM

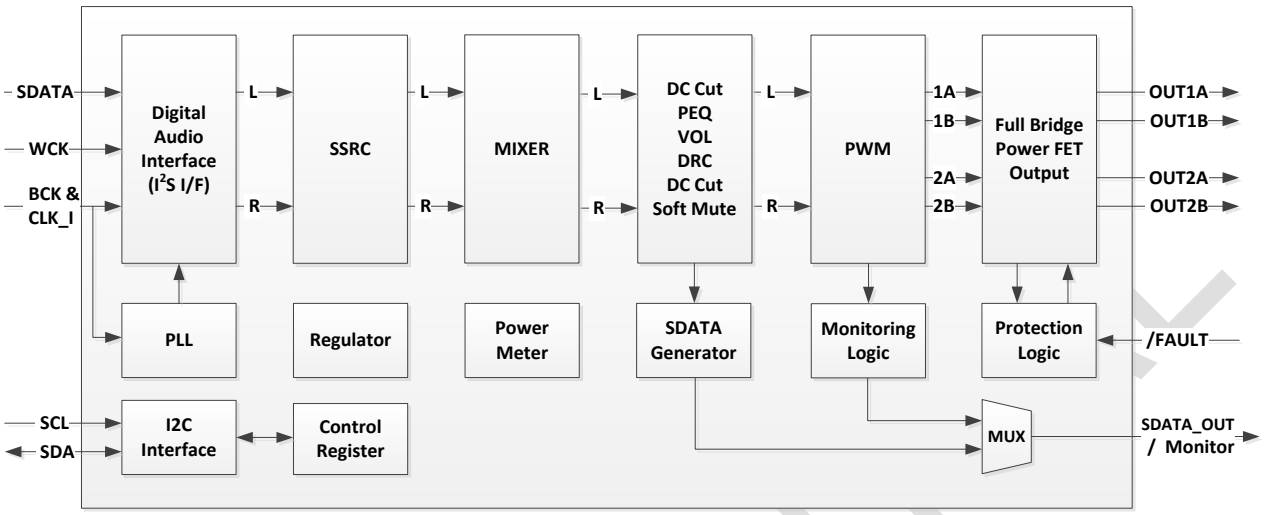


Figure 1. NTP8810A Block Diagram

2. PIN ASSIGNMENTS

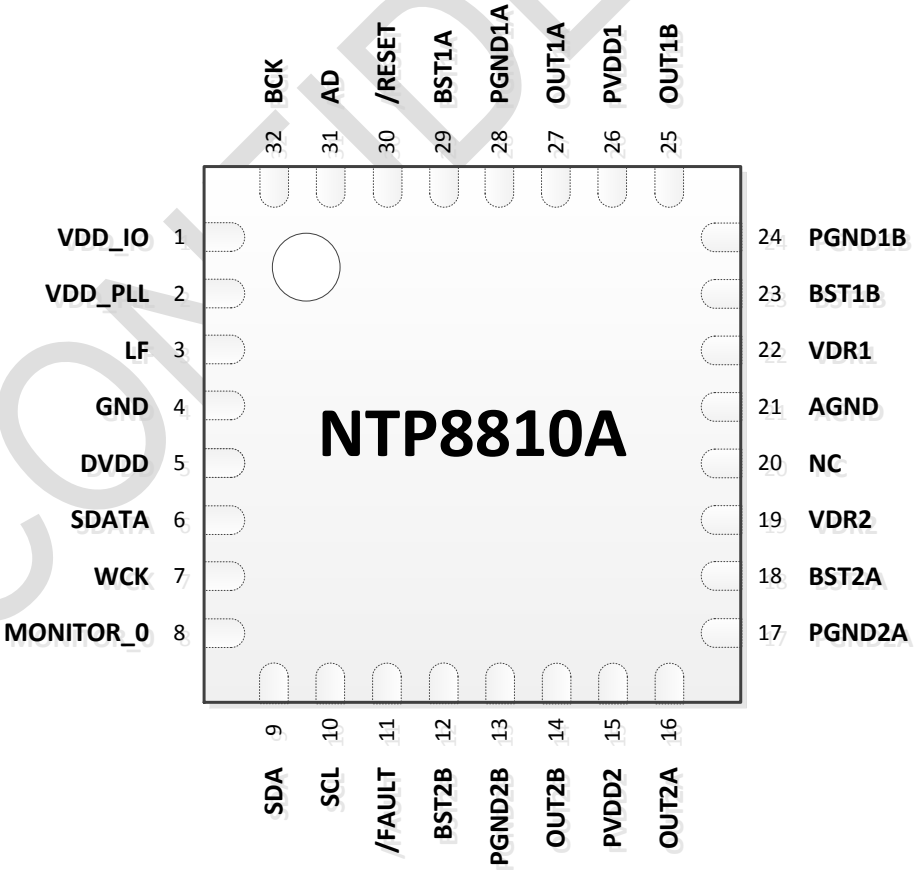


Figure 2. NTP8810A Pin Assignments

3. PIN DESCRIPTIONS

PIN	NAME	TYPE	DESCRIPTION
1	VDD_IO	P	Power supply for digital interface I/O, 3.3V
2	VDD_PLL	P	Regulator output for PLL digital block, 1.2V
3	LF	I/O	External PLL loop filter
4	GND	P	This pin should be connected to Ground
5	DVDD	P	Regulator output for Core block, 1.2V
6	SDATA	I	I^2S serial data input
7	WCK	I	I^2S word clock
8	MONITOR_0	O	No Connection, monitoring signal out from protection logic
9	SDA	I/O	I^2C data
10	SCL	I	I^2C clock
11	/FAULT	I	Active low to reset internal power stage, Pull-up
12	BST2B	P	Bootstrap supply, external capacitor to OUT2B is required
13	PGND2B	P	Ground
14	OUT2B	O	Power stage PWM output 2B
15	PVDD2	P	Power supply for PWM Power stage 2
16	OUT2A	O	Power stage PWM output 2A
17	PGND2A	P	Ground
18	BST2A	P	Bootstrap supply, external capacitor to OUT2A is required
19	VDR2	P	Gate drive voltage regulator decoupling pin, capacitor to GND is required
20	NC	-	Not connected
21	AGND	P	Ground
22	VDR1	P	Gate drive voltage regulator decoupling pin, capacitor to GND is required
23	BST1B	P	Bootstrap supply, external capacitor to OUT1B is required
24	PGND1B	P	Ground
25	OUT1B	O	Power stage PWM output 1B
26	PVDD1	P	Power supply for PWM Power stage 1
27	OUT1A	O	Power stage PWM output 1A
28	PGND1A	P	Ground
29	BST1A	P	Bootstrap supply, external capacitor to OUT1A is required
30	/RESET	I	Active low to reset NTP8810A, Schmitt trigger input
31	AD	I	I^2C device address selection
32	BCK	I	I^2S bit clock
-	Thermal Pad	P	This pad should be connected to Ground

P = Power Supply or Ground, I = Input, O = Output, I/O = Input / Output

Table 1. NTP8810A Pin Description

4. CHARACTERISTICS AND SPECIFICATIONS

4.1. Absolute Maximum Ratings

Parameter	Reference	Rating	Unit
DVDD voltage	DGND	-0.3 ~ 1.5	V
VDD_IO voltage	GND_IO	-0.3 ~ 5.25	V
Logic input voltage	GND	-0.3 ~ 5.25	V
Logic output voltage	GND	-0.3 ~ 5.25	V
PVDDXX voltage	PGNDXX	24	V
OUTXX voltage	PGNDXX	-0.3 ~ PVDDXX	V
BSTXX voltage	PGNDXX	30	V
VDRX voltage	PGNDXX	-0.3 ~ 6.0	V
Operating Ambient Temperature	T_A	-25 ~ +85	°C
Junction temperature	Tj	150	°C

4.2. Recommended Operating Conditions

Parameter	Reference	Rating			Unit
VDD_IO voltage	GND_IO	3.0 ~ 3.6			V
PVDDXX voltage	PGNDXX	4.5 ~ 20			V
VDRX voltage	PGNDXX	4.7	5.14	5.6	V
Load impedance (BTL)	Output Filter L :10uH, C : 470nF	6	8		Ω
Load impedance (PBTL)	Output Filter L :10uH, C : 470nF		4		Ω

4.3. DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Logic Block (VDD_IO=3.3V, T_A=+25°C, unless otherwise specified.)						
Input High voltage	V_{IH}	-	2.08			V
Input Low voltage	V_{IL}	-	-0.3		0.89	V
Schmitt trig. Hysteresis	ΔV	-		0.29		V
Input current	I_I	V_{IN}=V_{IL} MAX, DVDD=MIN	-50			uA
		V_{IN}=V_{IH} MIN, DVDD=MIN			50	uA
Input leakage current	I_L	V_{IN}=VSS, DVDD=MIN	-10		10	uA
Output Low voltage	V_{OL}	I_{OL} = -4mA	0		0.4	V
Output High voltage	V_{OH}	I_{OH} = 4mA	2.4		3.6	V
LDO output voltage	V_{LDO}	DVDD	1.08		1.32	V
Driver Block (PVDDXX=13V, T_A=+25°C, unless otherwise specified.)						
Current consumption		VDD_IO=3.3V, No Input, No Load		23		mA
		PVDD=13V, No Input, 8 Ω Load with 10uH inductor		30		
Peak current limit	OCP	-		4.5		A
Thermal shutdown temperature	OTP			150		°C
Under voltage lockout	UVP		3.6	3.9	4.15	V

4.4. Performance Specification

Speaker Amplifier					
Parameter	**Condition**	**Min**	**Typ**	**Max**	**Unit**
SNR	AES17, A-weighting filter		96		dB
THD+N	PS ≤ 0x7C, 20Hz~20kHz		0.3		%
Cross talk	Dolby standard		70		dB

4.5. Switching Characteristics – I²C Control

Parameter	Symbol	Condition	Min		Max	Unit
I²C Control Port						
SCL clock frequency	F_{scl}		-		400	kHz
Hold time for START condition	T_{hdsta}		600		-	ns
Low period of the SCL clock	T_{low}		1300		-	ns
High period of the SCL clock	T_{high}		600		-	ns
Rise time of SDA and SCL signals	T_{rise}		-		300	ns
Fall time of SDA and SCL signals	T_{fall}		-		300	ns
Setup time for STOP condition	T_{susto}		600		-	ns

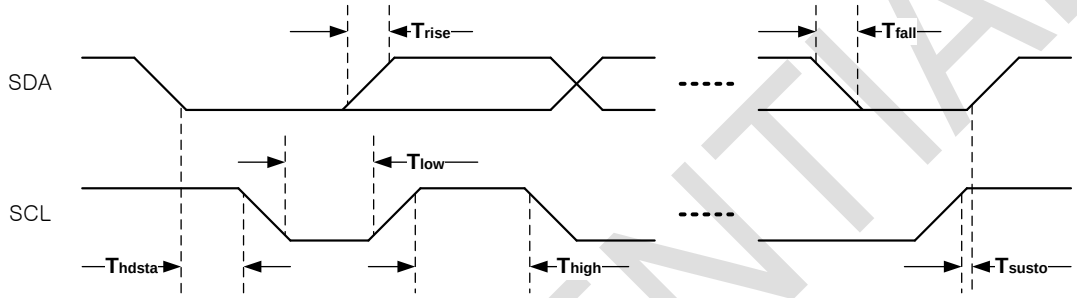


Figure 3. I²C Mode Timing

4.6. Switching Characteristics – Audio Interface

Parameters	Symbol	Min	Max	Unit
BCK high time	t_{bh}	20	-	ns
BCK low time	t_{bl}	20	-	ns
SDATA setup time before BCK rising edge	t_{ds}	10	-	ns
SDATA hold time after BCK rising edge	t_{dh}	10	-	ns
WCK setup time before BCK rising edge	t_{ws}	20	-	ns
BCK rising edge before WCK edge	t_{wh}	20	-	ns
BCK falling edge before WCK edge	t_{wl}	-20	20	ns
Rising/Falling time for BCK/WCK	$t_{br}/t_{bf}/t_{wrf}$	-	50	ns

※ Schmitt trigger characteristics (V_{SIH} Min = 1.85V, V_{SIH} Max = 0.9V)

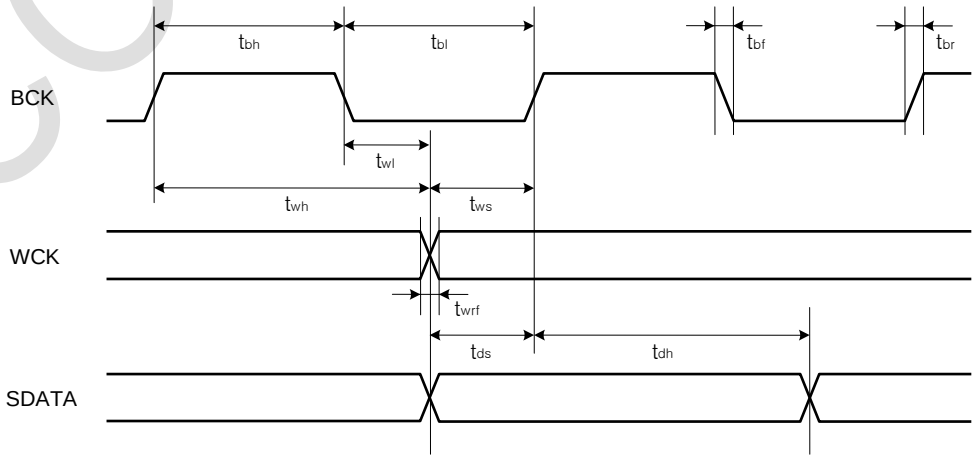


Figure 4. Audio Interface Timing

5. I2C BUS OF NTP8810A

The NTP8810A uses an industry standard Inter IC Control (I^2C) bus to communicate with host IC. A host IC can write or read internal registers of the NTP8810A via the I^2C bus.

5.1. General Description of I^2C Bus

The I^2C bus uses two signal lines – a serial clock line (SCL) and a serial data line (SDA). Because the SDA line is open-drain type port, both the NTP8810A and a host IC can only drive these pins low or leave them open.

In I^2C bus, a master device means the device which generates serial clock on the SCL. A slave device means the device which receives serial clock. There can be many master and slave devices on an I^2C bus. But, when one master device works on the bus, the other master devices should not generate signal on the lines. These unexpected interrupts can make other slave devices to fail to communicate with the mater device.

The NTP8810A supports only slave mode of I^2C bus. So, the NTP8810A always receives serial clock from a host IC. The slave mode is enough to write/read data to/from the NTP8810A.

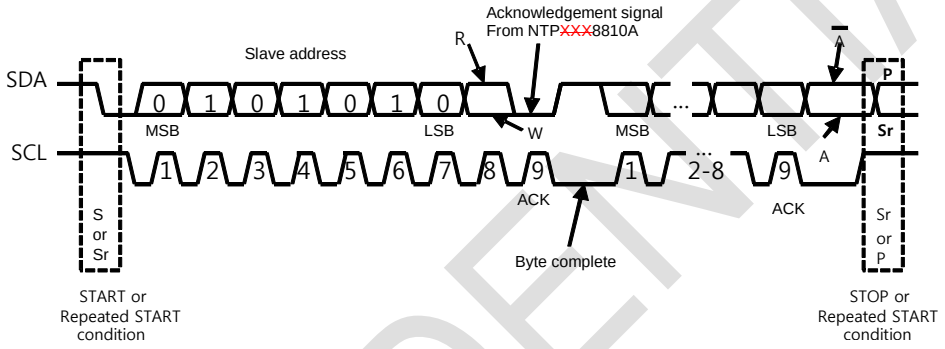


Figure 5. Basic Signaling Elements of I^2C Bus

If there are no communication on I^2C bus, lines must keep in high state. I^2C bus begins communication with the start condition and ends communication with the stop condition. The start condition can be generated by changing the SDA state high to low, during the SCL state remains in high. The stop condition can be generated by changing the SDA state low to high during the SCL remains in high state. Be aware that the stop condition always reset the internal status of I^2C bus control logic. Except these two conditions, the SDA may not change during the SCL in high state. Otherwise, abnormal start or stop condition will be generated.

I^2C bus transfers the MSB of a byte on 1st data slot and the LSB of a byte on 8th data slot. I^2C bus checks success or fail of transfer on every 1 byte transfer. The device which found an expected data on SDA must generate acknowledgement (keep low on SDA) on 9th clock. If there is no acknowledgement on 9th clock, the device which generated a data on SDA may stop transfer. The NTP8810A will generate acknowledgement for every successful data transfer of 1 byte in write mode. But, in read mode, because data is generated by the NTP8810A, the NTP8810A will not generate an acknowledgement. In this case, on the contrary, the NTP8810A will check SDA state on 9th clock that the master device received a read data properly.

Last 8th bit of the 1st byte is used to indicate whether the master device want to write or read data.

5.1.1. Writing Operation

When last 8th bit of the 1st byte is set to low state, the writing operation of I^2C bus begins. The NTP8810A supports 3 kind of writing operations which presented on **Figure 6**.

The type presented on **Figure 6-(a)** is single byte write operation. “Sub address” on 2nd byte means the internal register address of the NTP8810A. The “Data” on 3rd byte will be written into the internal register address on “Sub address”. If stop condition is not generated, writing “data” on specific “sub address” can be repeated like **Figure 6-(b)**. “Data #n” will be written on “sub address #n”.

The type presented on **Figure 6-(c)** is single byte write operation under address auto increment mode. The AIF on 1st bit of 2nd byte is the address auto increment flag. If SDA is set to high state on AIF slots, the NTP8810A write data continuously with register addresses which increased from initial “sub

address" for every byte; "Data #n" will be written on "sub address" + n – 1. The internal address will cycle automatically.

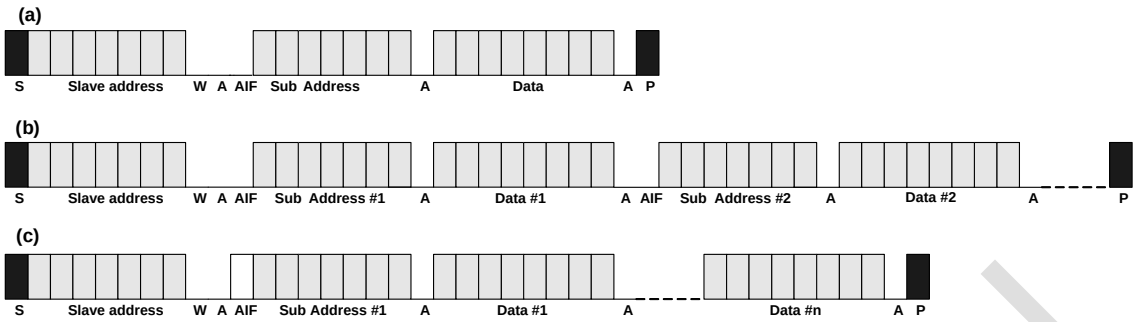


Figure 6. Single Byte Write Mode Sequence

Figure 7-(a), Figure 7-(b), and **Figure 7-(c)** represent 4 byte writing operations. Coefficient Mode Register address 0x00~0x62 are used to configure Bi-Quad filter coefficients, those are BQ, power meter gain and PEQ/DRC check. The data size of these coefficients and gains is 4 byte for each. The difference between 4byte writing operation and single byte writing operation is only the size of transferring data. So, after sending "Sub address", 4 sequential bytes must be transferred from the MSB(most significant byte) to the LSB(least significant byte) sequence.
The type presented on **Figure 7-(c)** is quad byte write operation under address auto increment mode, AIF function. Please compare the data transfer size between **Figure 6** and **Figure 7.**

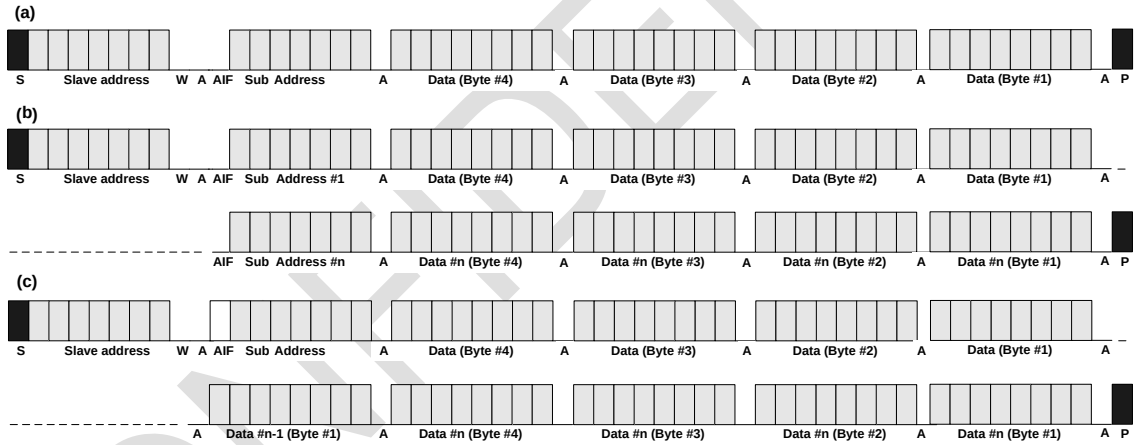


Figure 7. Quad Byte Write Mode Sequence

The coefficient mode register address from 0x00 to 0x62 are used for the Bi-Quad filter coefficients in the coefficient mode. Each Bi-Quad filter uses 5 coefficients. Any unexpected coefficient value changes on any part of 5 coefficients can generate unstable Bi-Quad filter response. For example, if only one of 5 coefficients for a Bi-quad filter is changed and downloaded, its combined 5-coefficient set can have unstable operation while old and new coefficients are mixed together. Therefore to prevent this kind of problem, the NTP8810A writes coefficients to coefficient registers only when the last 5th coefficients of each Bi-quad filter are downloaded, which means all of 5 coefficients are fully ready. Please refer to 9.1 for more detailed operation.

5.1.2. Reading Operation

Figure 8-(a) represents single byte reading operation from the NTP8810A. To read data from the NTP8810A, generate start condition to start transfer. After then, send “slave address” with write mode flag and send the register address(sub address). By regenerating start condition (Sr) again and transferring “slave address” with read mode flag, reading operation begins. The NTP8810A will generate data on SDA signal synchronizing with serial clocks on the SCL. Because the SDA signal generated from the NTP8810A, the master device must generate ACK on 9th slot to confirm that the master received read 1 byte successfully. However, if this is just one byte reading operation, NAK (not acknowledged) signal must be generated. Then stop condition must be generated to end transfer.
When AIF set to high on sub address like **Figure 8-(b)**, data will be read continuously with register addresses which are increased from initial “sub address” for every byte. To continue reading operation in this case, the master must generate ACK signal on every 9th slot to confirm that master received 1 byte successfully. Otherwise, reading operation will be terminated. To end address auto incrementing reading operation, generate NAK on 9th slot and generate stop condition.

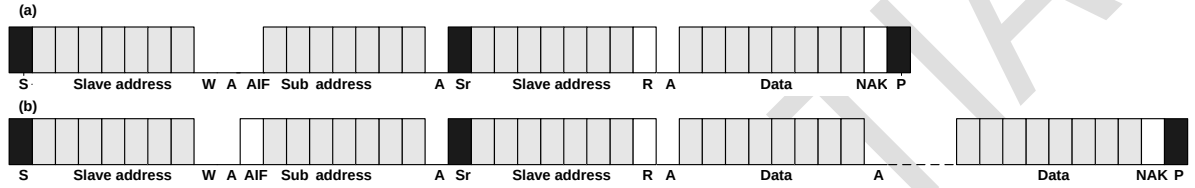


Figure 8. Single Byte Read Mode Sequence

Figure 9 represents quad byte reading operation. The difference between quad byte reading operation and single byte reading operation is only the size of receiving data. So, after sending “Sub address”, 4 sequential bytes must be received from the MSB to the LSB sequence.
The type presented on **Figure 9-(b)** is quad byte read operation under address auto increment mode, AIF function. Please compare the data receive size between **Figure 8** and **Figure 9.**

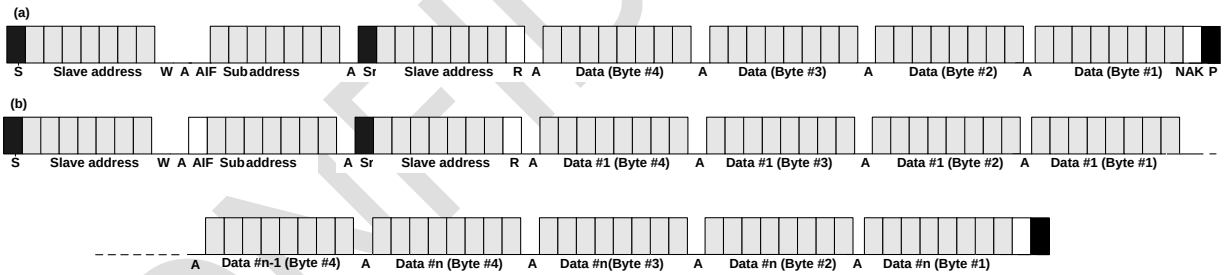


Figure 9. Quad Byte Read Mode Sequence

5.1.3. I²C Glitch Filter

To clean out the threats of noise in today’s high-speed-board system, the NTP8810A has a glitch elimination filter on the I^2C ports. Glitches in the transmission lines of the I^2C port can be safely removed with this function. Please refer to the register 0x3B.

5.1.4. I²C Slave Address

The NTP8810A supports up to four slave address. So, four NTP8810A can be connected to the same MCU at the same time. For multi-chip operation, use the proper I2C slave address according to AD pin and the initial state of Monitor_0 pin as shown in **Table 2**.

		Monitor_0		
Pin name	Value	Pull-down (‘L’)	Pull-up (‘H’)	No pd / pu (default: ‘L’)
AD	0	Addr : 0x54	Addr : 0x58	Addr : 0x54
	1	Addr : 0x56	Addr : 0x5A	Addr : 0x56

Table 2. I^2C Slave Address

6. CLOCK, RESET & CONTROL

6.1. System Clock

The internal system clock of the NTP8810A is generated from an external master clock by the on-chip PLL. The NTP8810A supports external master clock frequency from 2.048 MHz to 24.576MHz. For proper operation, the registers for the PLL should be set correctly according to master clock frequency (Address 0x00).

6.2. Timing Sequence 1 (recommend)

For proper power up, initialization and power down of NTP8810A, it is recommend to use the following sequence as shown in **Figure 10**.

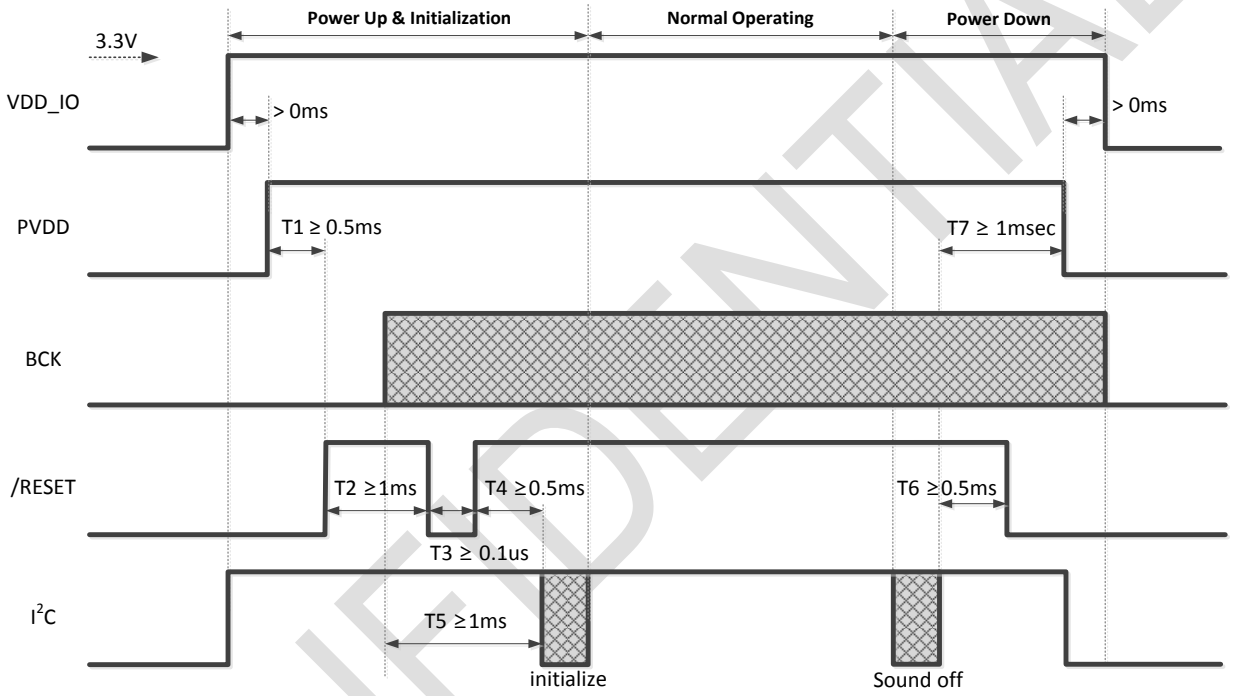


Figure 10. Timing Sequence 1

6.2.1. Power-Up & Initialization Sequence

1) Ramp up VDD_IO to at least 3.3V.
2) Ramp up PVDD.
3) After 0.5msec (T1≥0.5msec), drive /RESET = High, and then wait for at least 1msec (T2≥1msec).
4) Hold /RESET Low for at least 0.1usec (T3≥1usec)
5) Drive /RESET = High, and then wait for at least 0.5msec for I^2C communication (T4≥0.5msec).
6) BCK signal should arrive at least 1msec before I^2C initialization sequence (T5≥1msec).
7) Execute both amp initialization sequence (e.g. clock, volume, DRC, PEQ setup) and Sound on (Address: 0x04, Data: 0xFF) sequence.

6.2.2. Power-Down Sequence

1) When both DC and AC power are off, make sure to execute sound off sequence (Address: 0x04, Data: 0x00).
2) Switch /RESET to Low after sound off sequence (T6≥0.5msec).
3) BCK and I^2C should be Low after sound off sequence (T7≥0.5msec).
4) After I^2C is Low, ramp down VDD_IO.

6.3. Timing Sequence 2 (reference)

Following figure illustrates another timing sequence, which is conforming to the legacy reset timing.

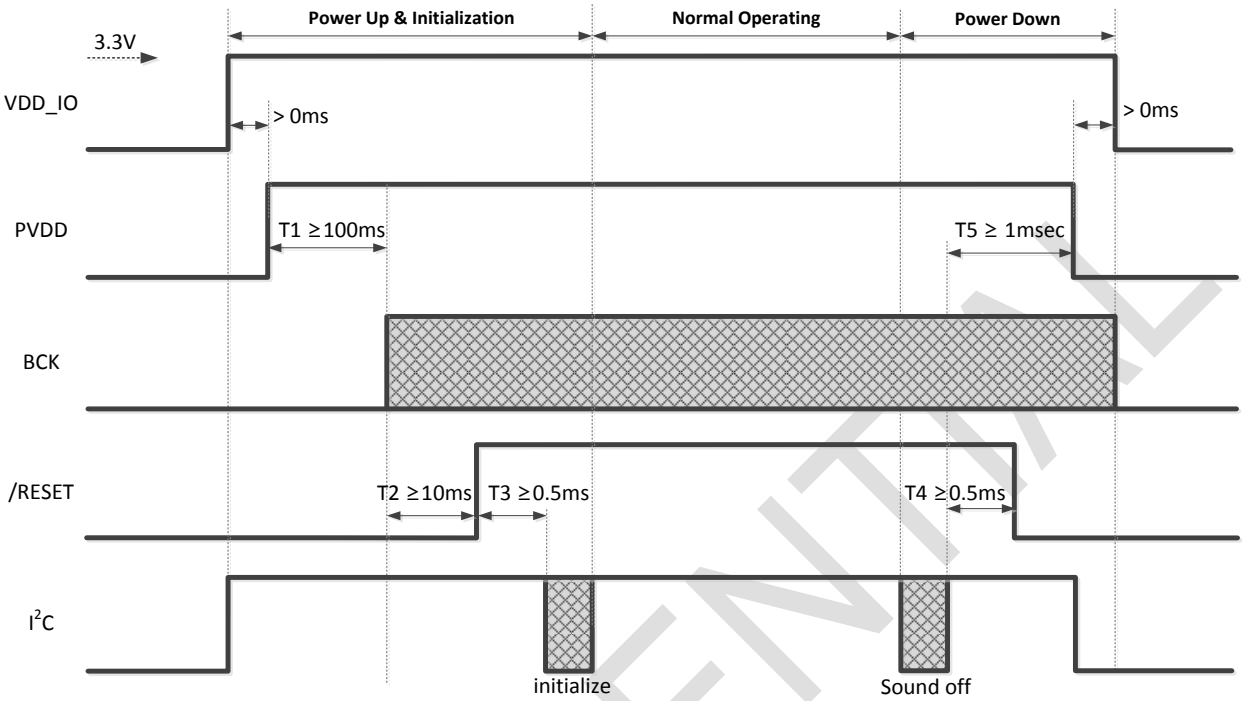


Figure 11. Timing Sequence 2

6.3.1. Power-Up & Initialization Sequence

1) Ramp up VDD_IO to at least 3.3V.
2) Ramp up PVDD.
3) Drive BCK signal at least 100ms after PVDD (T1≥100msec).
4) At least 10ms after BCK, Drive /RESET = High(T2≥10msec).
5) Wait for at least 0.5msec for I^2C communication (T3≥0.5msec) and keep the status.
6) Execute both amp initialization sequence (e.g. clock, volume, DRC, PEQ setup) and Sound on sequence.

6.3.2. Power-Down Sequence

1) When both DC and AC power are off, make sure to execute sound off sequence.
2) Switch /RESET to Low at least 0.5 msec after sound off sequence (T4≥0.5msec).
3) Ramp down PVDD at least 1 msec after sound off sequence (T5≥1msec).
4) After I^2C is Low, ramp down VDD_IO.

7. AUDIO INTERFACE

7.1. I^2S

NTP8810A receives audio data through digital audio interface. There is a standard digital audio interface - the Inter-IC Sound (I^2S) Interface.

These interfaces use 2 clock lines and 1 data line to receive the audio data. One of these clock lines is the WCK. A period of the WCK is same with sampling period of audio data i.e. 64bits (32bits for each channel). One of the main function of WCK to define the channels, the low state of WCK indicates the 1^{st} channel i.e. left channel and the high state indicate the 2^{nd} channel i.e. right channel. This feature enable the clock receiving device to synchronize the data word-wise for transmitting or receiving from clock generating device.

The other clock line is BCK. This clock line used to synchronize the bit-wise data. The number of clock for one WCK period is 64 clock of BCK. The name of data transfer line is SDATA. The data being synchronized with the BCK must be loaded on this line. NTP8810A receive data on rising edge of the BCK. The bit range for I^2S is predefined.

NTP8810A can only work as a slave on bus. In slave mode, NTP8810A receives WCK and BCK from external source. Please refer to the following **Figure 12**.

7.1.1. I^2S Glitch Filter

To clean out the threats of noise in today's high-speed-board system, the NTP8810A has a glitch elimination filter on the I^2S ports. Glitches in the transmission lines of the I^2S port can be safely removed with this function. Please refer to the register 0x72.

7.2. SDATA Generator

The SDATA generator of NTP8810A sends out I2S out signal. In order for SDATA out process to function stably, the falling of BCK should either synchronize or occur ahead of falling or rising of WCK. Refer to the register Address 0x5F in the **Appendix A** and refer to the **4.6. Switching Characteristics – Audio Interface**.

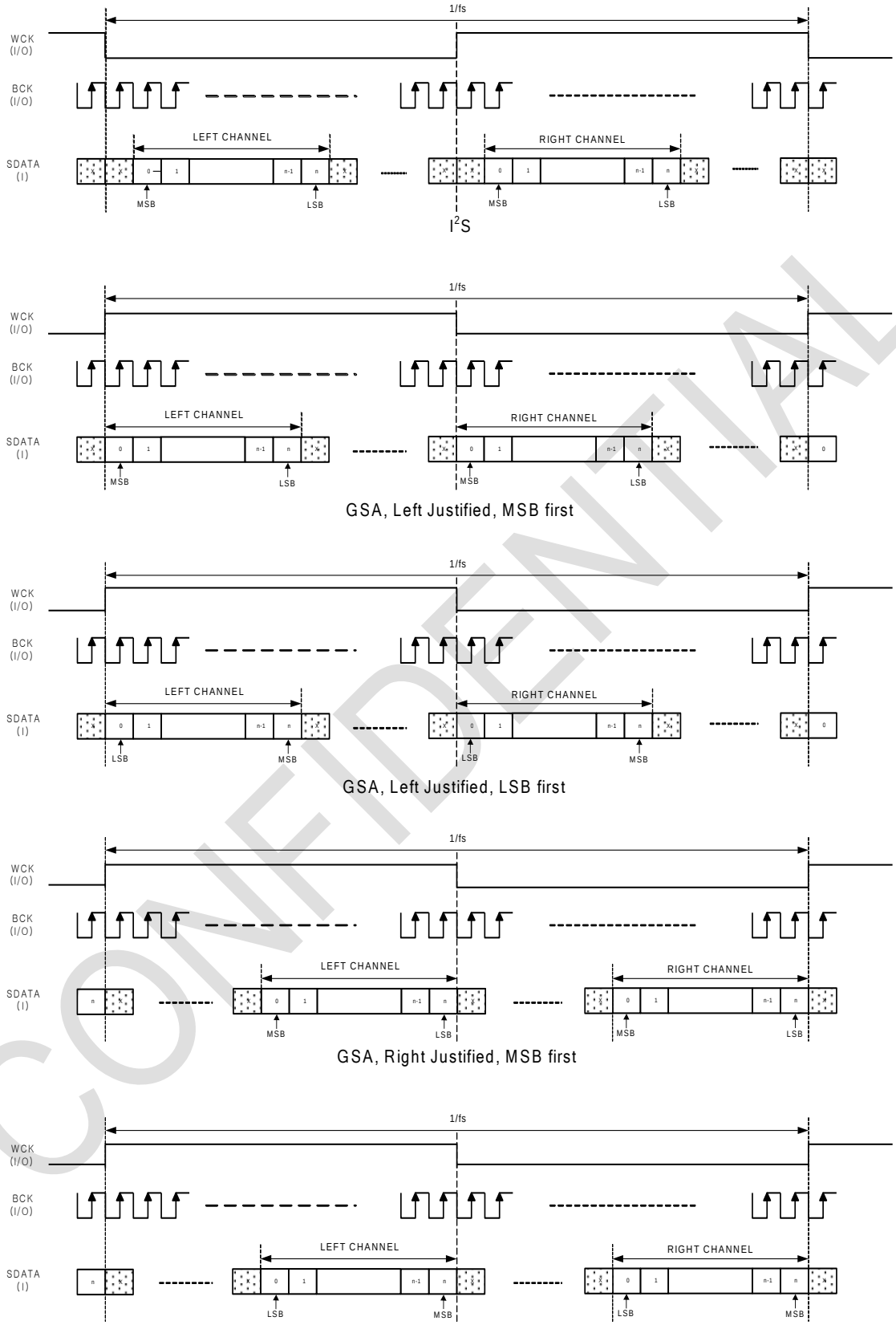


Figure 12. I²S Audio Interface Format

8. MIXER

Channel mixer can be used in lots of application needs like pseudo stereo and etc. User can mix input channels into each output channels with designated gains and polarity. Step size of mixer gain is variable according to the gain level as shown below.

Volume Range (dB)	Step (dB)
+18 ~ +6	1
+5.5 ~ -5.5	0.5
-6 ~ -32	1
≤ 32	-∞

Table 3. Variable Step Mixing Gain

In total, 4 mixing gain coefficients denoted as M00, M01, M10 and M11 are defined as shown in the equation below. Each Mxx stores volume value in dB scale, and the number values versus gain in dB are shown in the **Appendix B**. By default, each input channel connected to each output channel directly; M00 and M11 are set as 0 dB in plus polarity, M01 and M10 are set as -∞ dB.

[Output Channels] = [Mixer Matrix] x [Input Channels]

$$\begin{bmatrix} CH1\ OUT \\ CH2\ OUT \end{bmatrix} = \begin{bmatrix} M00 & M01 \\ M10 & M11 \end{bmatrix} \cdot \begin{bmatrix} CH1\ IN \\ CH2\ IN \end{bmatrix}$$

Figure 13. Serial Mixer Matrix

In order to load mixer coefficients into internal memory, send the index value in the gain value table to the register address 0x09, 0x21~0x24. Each address matched to M00, M01, M10 and M11 sequentially.

9. PRE-PROCESSING

9.1. Bi-Quad Filter Chain

The Bi-Quad filter means 2nd order IIR filter. NTP8810A implemented a serial chain of Bi-Quad filters with proprietary floating point operation schemes. The Bi-Quad filter chains can be used in various purposes; parametric EQ, loud-speaker EQ, DC cut and etc. The Bi-Quad filter structure is shown in **Figure 14**.

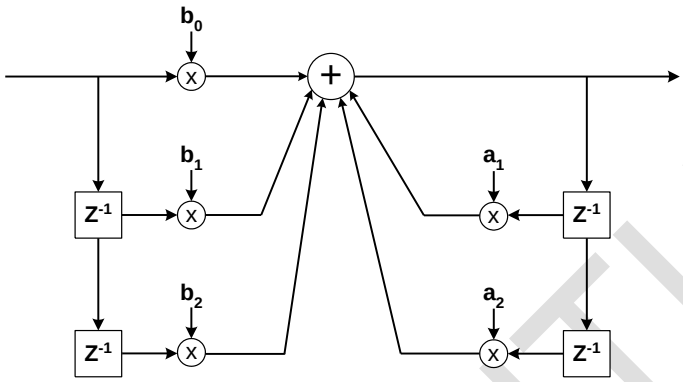


Figure 14. Bi-Quad Filter Structure

Fourteen Bi-Quad filters are linked serially for one channel. The Bi-Quad filters can be configured differently for each filter.

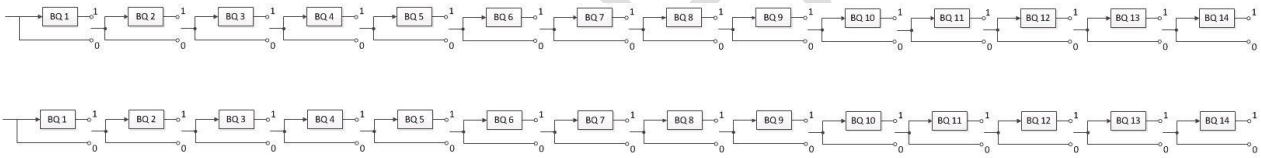


Figure 15. Bi-Quad Filter Chain

Filter coefficients are 32-bit floating point numbers and can be downloaded thru I^2C interface. To download Bi-Quad filter coefficients to NTP8810A, select download channel by using CH flag in register Address 0x7E first. Then, write actual coefficient values to register addresses, from 0x00 to 0x62 in the coefficient register addresses.

The coefficient mode register addresses from 0x00 through 0x04 designate the five coefficients of the first Bi-Quad (BQ1) and represent coefficients b0, b1, b2, a1, a2 respectively. The coefficient mode register addresses from 0x05 through 0x09 designate coefficients of the 2nd Bi-Quad (BQ2) filter, and so on. The enable/disable operation of these Bi-Quad filters can be made by using BQF flag in register addresses of 0x3C~0x3F and 0x18~0x19.

Coefficient Mode register	0x00 ~ 0x04	0x05 ~ 0x09	0x0A ~ 0x0E	0x0F ~ 0x13	0x14 ~ 0x18	0x19 ~ 0x1D	0x1E ~ 0x22
When system address 0x7E = 0x01	BQ1 of CH1/2	BQ2 of CH1/2	BQ3 of CH1/2	BQ4 of CH1/2	BQ5 of CH1/2	BQ7 of CH1/2	BQ8 of CH1/2
Coefficient Mode register	0x23 ~ 0x27	0x45 ~ 0x49	0x4A ~ 0x4F	0x4F ~ 0x53	0x54 ~ 0x58	0x59 ~ 0x5D	0x5E ~ 0x62
When system address 0x7E = 0x01	BQ9 of CH1/2	BQ10 of CH1/2	BQ11 of CH1/2	BQ6 of CH1/2	BQ12 of CH1/2	BQ13 of CH1/2	BQ14 of CH1/2

Table 4. Address of Coefficients for Bi-Quad Filter Chain

10. VOLUME & DYNAMIC RANGE CONTROL

Master and channel volumes of the NTP8810A are independently controlled and softly changed. The system register address 0x04 is the master volume control that affects both channels simultaneously and the address 0x06 and 0x07 correspond to the channel volume control register for channel 1 and 2 respectively.
The possible Maximum Gain is +48.375dB with using master volume fine control, master volume and channel volume because the master volume applies the gain to an input signal independent from a channel volume. However, in such a case, a clipping might occur to prevent a signal overflow error if the magnitude of the input signal is large enough to exceed 0dB under the combined volume setting.

10.1. Master Volume Control

By setting volume control register (address 0x04), master volume is controlled from negative infinity through 0dB with selectable step size as follows. For details on the master volume setting, see the register value table shown in **Appendix B**.

Step	Range
0.5 dB	0 ~ -125 dB

Table 5. Level Dependent Master Volume Steps

10.2. Channel Volume Control

By setting volume control registers (address 0x06 and 0x07), channel volumes are independently controlled from negative infinity through +48dB with two selectable step sizes as described below, and in the **Appendix B**, exact values for channel volume setting are described.

Step	Range
0.5 dB	+48 ~ -79 dB

Table 6. Level Dependent Channel Volume Steps

10.3. Master Volume Fine Control

Fine control for master volume is possible (+0.125dB step up to maximum +0.375dB boost). Refer to the system register Address 0x05 in the **Appendix A**.

10.4. Mute and Soft Volume Change

The NTP8810A enters mute state by setting soft mute flag of register Address 0x30. Soft mute is implemented so that the volume gradually increases or decreases when mute is turned off or on respectively. Also the soft mute speed and soft volume change speed rates are programmable. Designers can minimize the pop noise by controlling the soft mute speed and volume change intervals. Refer SM flag of register Address 0x30 and SVI flag of register Address 0x37.

10.5. Auto Mute

The NTP8810A can mute the sound automatically when the level of input audio signal is lower than the register-controlled threshold value. The mute can be done by PWM switching with 50 % duty ratio.
Auto mute is supported for internal channels 1~2 after 2x2 mixer block. Refer register Address 0x38.

10.6. Dynamic Range Control

NTP8810A has a 2-band scheme for dynamic range control, which comprises a high band DRC and a low band DRC. The input data is separated into two bands by HPF and LPF, and then those two bands are processed by H-DRC and L-DRC respectively. Finally, two processed bands are merged, to produce the output data with the fully controlled dynamic range. For detailed setting of the DRC registers, please refer to the system register addresses in **Table 8**. and refer to the coefficient mode register addresses in **Table 7**.

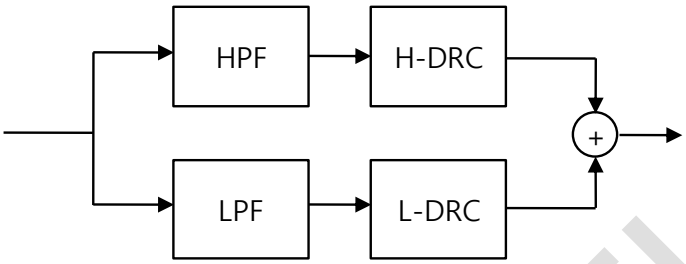


Figure 16. Block Diagram of Dynamic Range Control

2B' DRC Coefficient mode register	0x28 ~ 0x2C	0x2D ~ 0x31	0x32 ~ 0x36	0x37 ~ 0x3B
When System Address 0x7E = 0x01	BQ1_Low	BQ2_Low	BQ3_High	BQ4_High

Table 7. DRC Coefficient Mode Register Map for Dynamic Range Control

2B' DRC System Address	0x2B	0x2D	0x2A	0x2C
When system address 0x7E = 0x00	Attack/ Release time control of L-DRC	Attack/ Release Time control of H-DRC	Threshold for L-DRC	Threshold for H-DRC

Table 8. System Register Map for Dynamic Range Control

10.7. Power Meter

The power meter measures signal's energy of internal, send value of energy through register address 0x54 and always operates without on/off control.

Because audio signals swing very rapidly in process of time, user can use power meter gain to get stable value of energy. The more power meter gain approaches to maximum value, the more value of energy changes slowly.

Power meter gain is 32-bit floating point numbers and can be downloaded thru I^2C interface. To download power meter gain, page flag register 0x7E should be set 0x01. And then write gain value to coefficient mode register address 0x41.

11.OUTPUT INTERFACE

11.1. Output Configuration

The output of NTP8810A has various options. To produce proper output signal, register 0x08, 0x31, 0x39, and 0x3A should be set to appropriate values.

11.2. AM Interference Relief Mode

The NTP8810A has AM interference reduction mode. In this mode SNR performance of NTP8810A can be degrade down to 90 dB and the PWM switching frequency is spread from 384kHz through 768kHz.

11.3. PWM Output Mapper

Any internal channel that produces a PWM output can be assigned to any PWM output hardware port (or pin) by mapping output port register. This feature is very helpful for the hardware designer because it can relieve difficulties in the power stage signal routing and channel assignment if the output channel order is fixed. See the system register address 0x39 in the **Appendix A**.

11.4. Switching Output Mode

There are two selectable switching output modes in NTP8810A. The difference between two output modes lies in the relationship of the relative signal pattern between PWM OUTxA and PWM OUTxB for a channel x. The first one is called as AD mode. This AD mode can be applied to both half bridge and full bridge output stage.

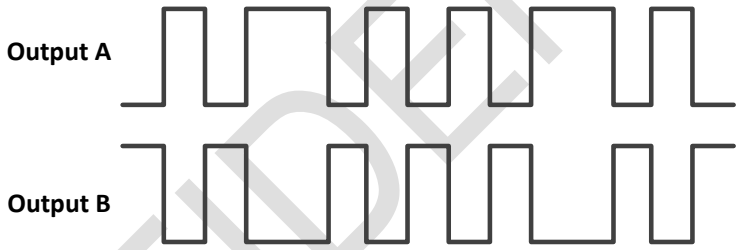


Figure 17. PWM Output Signals in AD Mode

AD asynchronous pair means the normal AD mode PWM output. In other words, A output and B output of each PWM output pair are mutually complementary. In the case of AD synchronous pair, A output and B output is perfectly identical, and its relation is not complementary. This is useful in some special case including single-ended power stage design.
The other one is called as NTX (Neo Trinity Amplification), which is D-BTL mode. This mode is applied only for BTL, and its operation is dynamically-biased BTL, compared to the normal BTL. An example of output signals in D-BTL mode is shown in Figure 18**.**

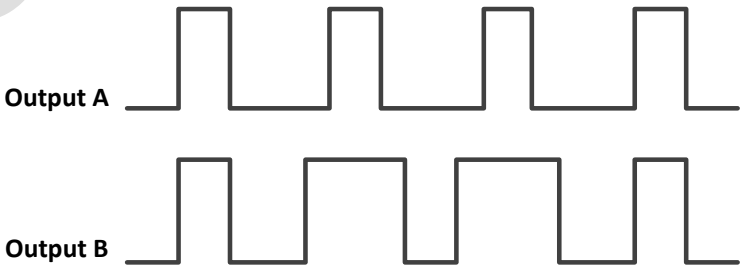


Figure 18. PWM Output Signals in D-BTL Mode

For D-BTL mode, there are two additional parameters, which is MLP (Minimum Linear Pulse Length). MLP defines the minimum pulse length that can guarantee a linear relationship between the input and output pulse length. Generally, the width of the output pulse is proportional to that of the input pulse. However, as the width of input pulse becomes narrower, such linear relation is not maintained due to the characteristic of a power device. The minimum MLP value is preferred as long as linear relationship between the input and the output pulse is satisfied. In addition, in terms of power consumption, a minimal MLP value is preferred.
This compensation is illustrated in **Figure 19**.

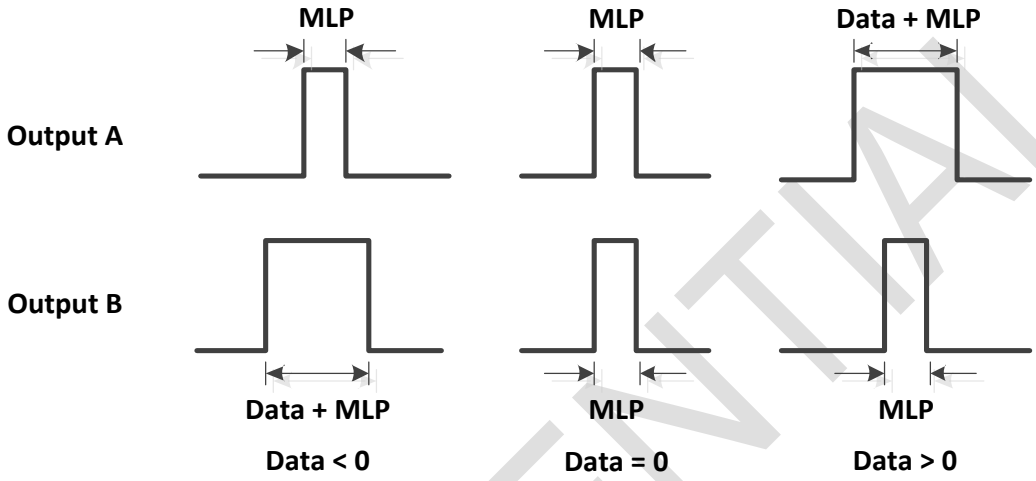


Figure 19. Compensation by MLP

11.5. Soft Start

The soft_start reduces pop noise by controlling rapidly increased energy of PWM.
To begin soft_start operation, PWM soft start enable register (0x44: PSE) should be set to high, and then PWM switching on/off register (0x31: POF) should be set to low. The duty ratio of PWM output increases from 127:1 (Low:High) to 50:50 (Low:High). Step repeat time register (0x44: SRT) means repeat number of PWM output in one duty sector. Soft_start operation with 17 repetitions is shown in the **Figure 20**.

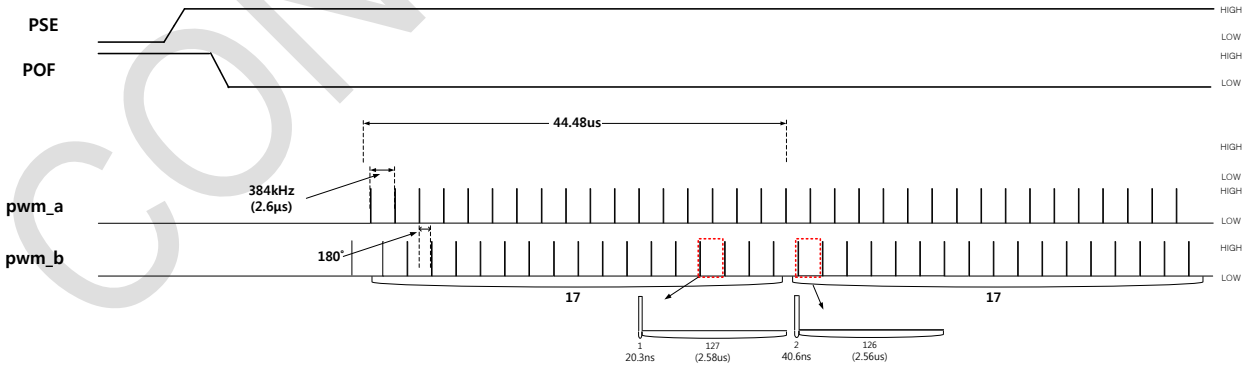


Figure 20. Soft Start Operation Timing

12. DC PROTECTION

This DC protection block prevents the system from outputting DC signal, which can cause a speaker unit burnt. Three sub functions are employed to prevent DC output, which are monitoring a memory checksum, observing a modulation index, and cutting DC output via hard-wired filters. Except for the hard-wired DC cut filter, the other two blocks only reports the error status, and external MCU may reset the amplifier chip by setting the DC soft reset register to high.

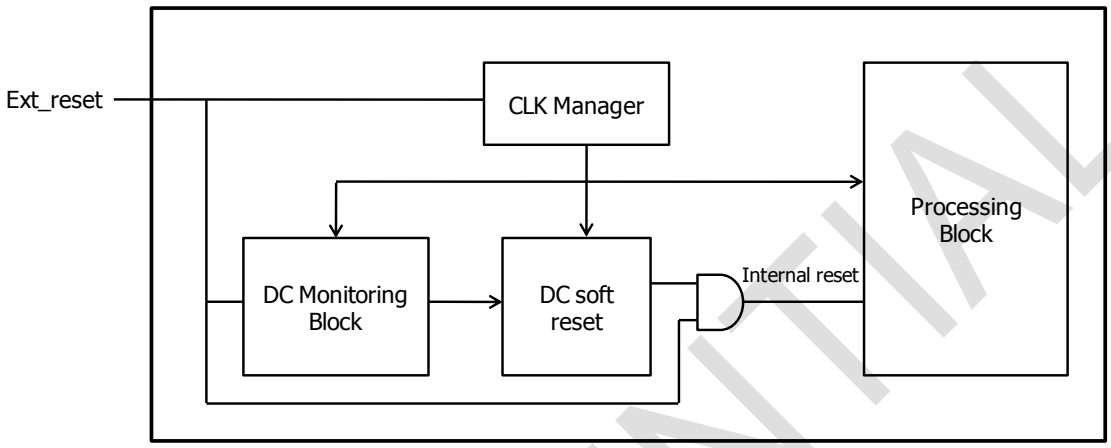


Figure 21. Block Diagram for DC PROTECTION

12.1 Memory Checksum

While initializing the system, the checksum data of coefficients are downloaded from the external MCU from the address 0x63 through 0x66. This memory checksum block compares the checksum data of current memory block and the checksum data at the initial time. If there happens a discrepancy between two values due to some memory fault, the error flag of address 0x6B is set to high. The external MCU can monitor this error flag and reset the chip by setting the DC soft reset to high at address 0x02. This DC soft reset will initialize the whole chip, and initialization process of the memory should be done thereafter.

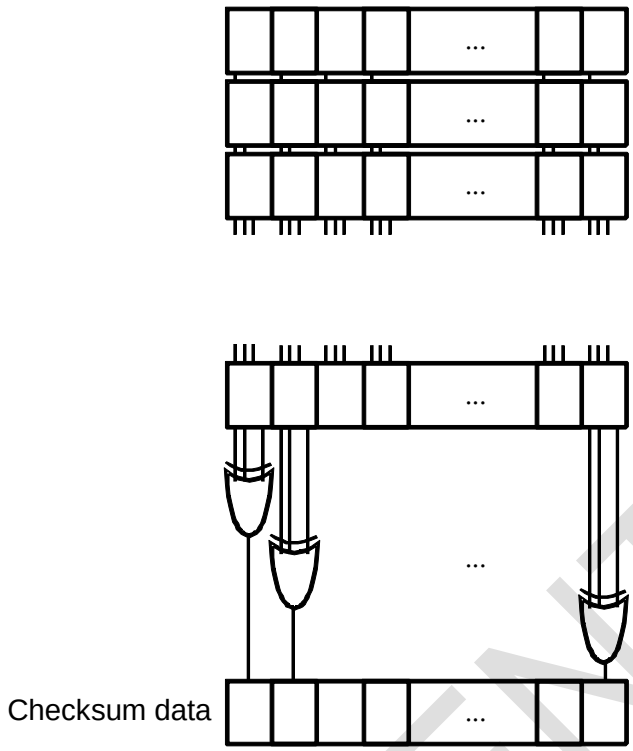


Figure 22. Structure of Memory Checksum

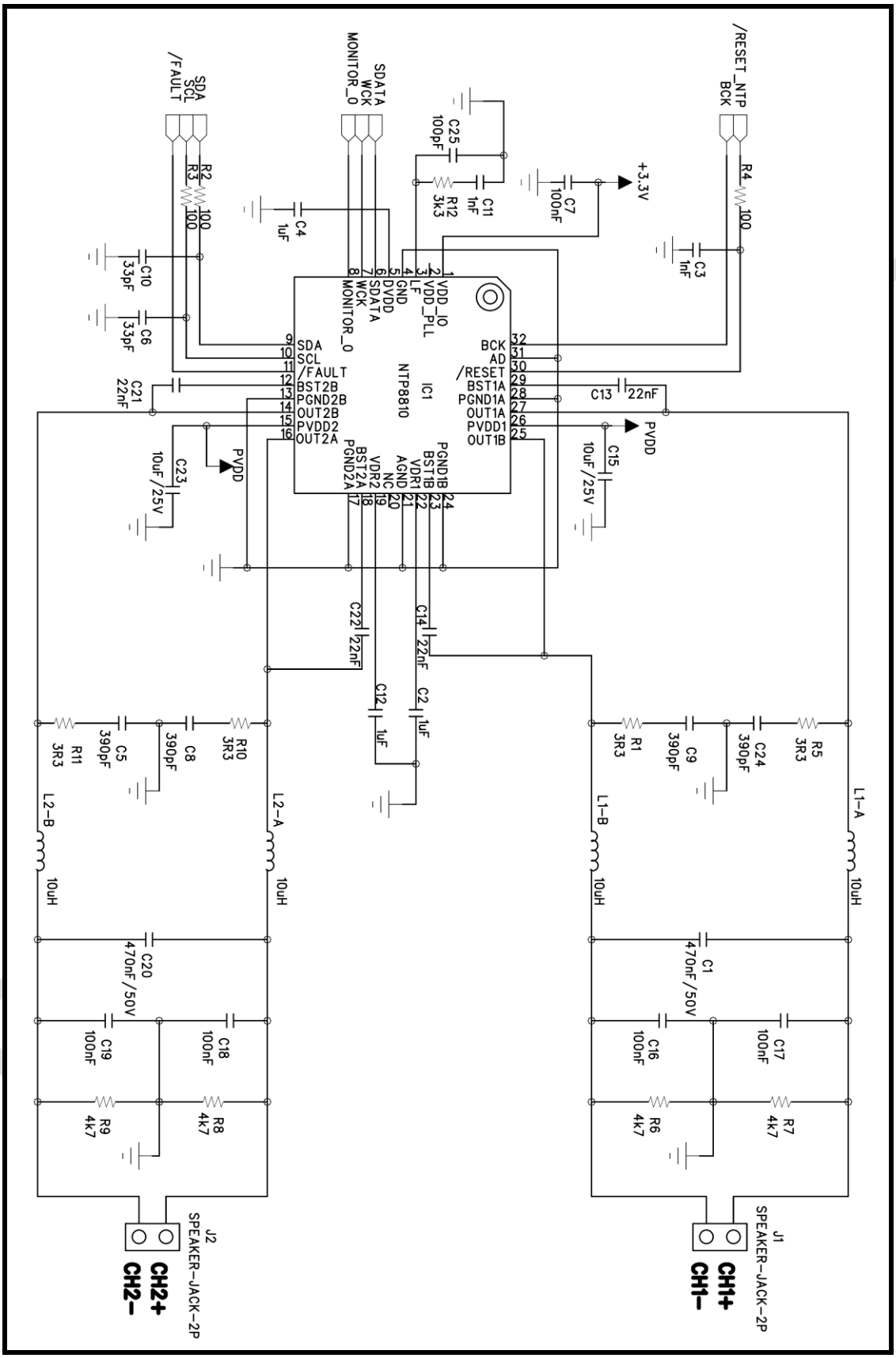
12.2 Modulation Index Check

When there is a DC component in the output, the modulation index tends to stay over or under certain value. The modulation index check block constantly monitors the PWM modulation index, and if the index value continues to stay over or under certain period of time, it sets modulation index error flag of address 0x6B to high. The external MCU can monitor this error flag and reset the chip by setting the DC soft reset the register value of address 0x02 to high. The PWM modulation duty at address 0x60 and 0x61 can be set to decide the level of DC monitoring for AD and D-BTL mode respectively.

12.3 Hard-Wired DC Cut

The hard-wired DC cut filters prevent the system from outputting the signal of less than 1Hz frequency. The two hard-wired DC cut filters exist in the Bi-quad filter chain. One is located forefront, while the other is at the end of filter chain.

13.TYPICAL APPLICATION SCHEMATICS



14. APPENDIX

A. Configuration Register Summary

Addr 0x00: Audio Input Format & Master Clock Frequency Control

Bit	7	6	5	4	3	2	1	0
Name	X	MCF			X	X	X	INS

Name	Description	Value	Meaning	Ref.
INS		**b'0**	I2S, slave mode	
		b'1	General serial audio, slave mode	
MCF	Master Clock Frequency	**b'000**	3.072 MHz (WCK 48 kHz) / 2.8224 MHz (WCK 44.1 kHz)	
		b'001	2.048 MHz (WCK 32 kHz)	
		b'010	6.144 MHz (WCK 96 kHz)	

Addr 0x01: System Status (read-only)

Bit	7	6	5	4	3	2	1	0
Name	X	DRCCHK	PEQCHK	DC	Current	TEMP	X	ULCK

Name	Description	Value	Meaning	Ref.
ULCK	Sampled PLL Unlock Error	**b'0**	PLL is locked state	
		b'1	PLL is Unlocked state	
TEMP	Temperature Protection Error	**b'0**	Temperature Protection Normal state	
		b'1	Temperature Protection Error state	
Current	Current protection Error	**b'0**	Current protection Normal state	
		b'1	Current protection Error state	
DC	Modulation Index Error	**b'0**	Modulation Index Normal state	
		b'1	Modulation Index Error state	
PEQCHK	PEQ Coefficient Checksum Error	**b'0**	PEQ1-12 Coefficient Normal state	
		b'1	PEQ1-12 Coefficient Error state	
DRCCHK	DRC Coefficient Checksum Error	**b'0**	DRC Coefficient Normal state	
		b'1	DRC Coefficient Error state	

Addr 0x02: Modulation Reset Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	X	Rst

Name	Description	Value	Meaning	Ref.
Rst	DC soft reset Flag	**b'0**		
		b'1	DC soft Reset start in Modulation	

Addr 0x03: Soft Mute Speed Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	SMC	

Name	Description	Value	Meaning	Ref.
SMC	Soft mute speed control	**b'00**	50msec (at 96 / 88.2kHz)	
		b'01	100msec	
		b'10	200msec	
		b'11	0msec (Hard change)	

Addr 0x04: Master Volume & SPK PWM Switching On/Off Control

Bit	7	6	5	4	3	2	1	0
Name	MVOL						SPOF	

Name	Description	Value	Meaning	Ref.
SPOF	Smart Switching Output on/off control	**b'00000000**	PWM off (softmute on → pwm off → pwm_mask low)	
		b'00000001	PWM off (softmute on → pwm off→ pwm_mask high)	
		b'00000010	PWM on (softmute on → pwm_mask high → pwm on)	
		b'00000011	PWM on (pwm_mask high → pwm on → softmute off)	
MVOL	Volume control	b'00000000 ~ b'11111111	See volume control register table. Reset default is 0 (**0x00**) (= −∞dB) 0xFF (= 0dB), 0.5dB Step	

Addr 0x05: Master Volume Fine Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	MVFC	

Name	Description	Value	Meaning	Ref.
MVFC	Master volume fine control	**b'00** ~ b'11	0dB ~ 0.375dB with 0.125dB step	

Addr 0x06~0x07: CH 1/2 Volume

Bit	7	6	5	4	3	2	1	0
Name	CH VOL							

Name	Description	Value	Meaning	Ref.
CHVOL	Volume control	b'00000000 ~ b'11111111	See channel volume table. Reset default is 0 (**0x9F**) (=0dB) 0xFFmeans 48dB with 0.5dB step.	

Addr 0x08: SPK Prescaler Value Control

Bit	7	6	5	4	3	2	1	0
Name	PS							

Name	Description	Value	Meaning	Ref.
PS	Prescaler value	b'00000000 ~ b'11111111	default = **0x68**	

Addr 0x09: SPK Operation Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	IMD		X	X	OPM	

Name	Description	Value	Meaning	Ref.
OPM	PWM output port	**b'00**	Normal BTL	
		b'01	PBTL(1A →1A,2A , 1B →1B,2B)	
IMD	Input Mode	**b'00**	Stereo	
		b'01	(L+R)/2 (In Mixer)	
		b'10/b'11	Follows Register setting (addr0x21~0x24)	

Addr 0x0A: Function Control

Bit	7	6	5	4	3	2	1	0
Name	X	CHK	X	PUD	X	AMDRC	MDRC	DRC

Name	Description	Value	Meaning	Ref.
DRC	1band DRC Enable	**b'0**	1band DRC Disable	
		b'1	1band DRC Enable	
MDRC	2band DRC Enable	**b'0**	2band DRC Disable	
		b'1	2band DRC Enable	
AMDRC	Advance 2band DRC Enable	**b'0**	Advance 2band DRC Disable	
		b'1	Advance 2band DRC Enable	
PUD	PEQ User mode	**b'0**	Disable individual BQ setting (addr 0x18~0x19, 0x3C~0x3F)	
		b'1	Enable individual BQ setting (addr 0x18~0x19, 0x3C~0x3F)	
CHK	Checksum Enable	**b'0**	Checksum Disable	
		b'1	Checksum Enable	

Reserved Addr 0x0B ~ 0x17

Addr 0x18~0x19: PEQ Filter Control 1 for Ch1 and Ch2 respectively

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	BQ14	X	BQ13	X	BQ12

Name	Description	Value	Meaning	Ref.
BQ12	On/off Bi_Quad 12 of ch. n (n = 1,2)	**b'0**	Bypass Bi-Quad 12 of channel n	
		b'1	Enable Bi-Quad 12 of channel n	
BQ13	On/off Bi_Quad 13 of ch. n (n = 1,2)	**b'0**	Bypass Bi-Quad 13 of channel n	
		b'1	Enable Bi-Quad 13 of channel n	
BQ14	On/off Bi_Quad 14 of ch. n (n = 1,2)	**b'0**	Bypass Bi-Quad 14 of channel n	
		b'1	Enable Bi-Quad 14 of channel n	

Addr 0x20: General Serial Audio Format

Bit	7	6	5	4	3	2	1	0
Name	X	X	BCKS		BS		MLF	LRJ

Name	Description	Value	Meaning	Ref.
LRJ	Serial data justify	**b'0**	Left justify	
		b'1	Right justify	
MLF	Serial bit order	**b'0**	MSB first	
		b'1	LSB first	
BS	Serial bit size	**b'00**	24 bit	
		b'01	20 bit	
		b'10	18 bit	
		b'11	16 bit	
BCKS	Bit clock size select	**b'00**	64 BCK/WCK	
		b'01	48 BCK/WCK	
		b'10	32 BCK/WCK	

Addr 0x21~0x24: Mixer Gain

Bit	7	6	5	4	3	2	1	0
Name	X	MG						

Name	Description	Value	Meaning	Ref.
MG	Mixer gain	b'0000000 ~ b'1111111	Mixer gain (refer to mixer gain table)	

$$\begin{bmatrix} mixer\_ch1\_output \\ mixer\_ch2\_output \end{bmatrix} = \begin{bmatrix} 0x21 & 0x22 \\ 0x23 & 0x24 \end{bmatrix} \bullet \begin{bmatrix} I2S\_ch1\_input \\ I2S\_ch2\_input \end{bmatrix}$$

Mixer equation

$$\begin{bmatrix} mixer\_ch1\_output \\ mixer\_ch2\_output \end{bmatrix} = \begin{bmatrix} 0dB(0x4E) & -\infty dB(0x00) \\ -\infty dB(0x00) & 0dB(0x4E) \end{bmatrix} \bullet \begin{bmatrix} I2S\_ch1\_input \\ I2S\_ch2\_input \end{bmatrix}$$

Reset default

Reserved Addr 0x25 ~ 0x29

Addr 0x2A: DRC Control 0

Bit	7	6	5	4	3	2	1	0
Name	CPR_L	CTS_L						

Name	Description	Value	Meaning	Ref.
CTS_L	DRC threshold for Low band	**b'0000000** ~ b'1111111	-57 ~ 12dB unsigned 7-bit DRC threshold for 1 band mode. In 2 band mode, It will control the threshold of low band. Refer to DRC threshold table for threshold values.	
CPR_L	DRC enable for Low band	**b'0**	Dynamic Range Compression off	
		b'1	Dynamic Range Compression on	

Addr 0x2B: DRC Control 1

Bit	7	6	5	4	3	2	1	0
Name	X	C1C_L			A1C_L			

Name	Description	Value	Meaning	Ref.
A1C_L	DRC attack time (Low band)	b'0000 ~ b'1010	Attack time control for 1 band mode. In 2 band mode, it will control the attack time of low band. (See DRC attack time table below.) default = **b'0001**	
C1C_L	DRC release time (Low band)	**b'000** ~ b'111	Release time control for 1 band mode. In 2 band mode, it will control the release time of low band. (See DRC release time table below.)	

Value of Register	Attack time 6dB, fs = 96,000
0011	30msec
0010	15msec
0001	8msec
0000	4msec
0111	2msec
0110	1msec
0101	0.5msec
0100	0.25msec
1000	5msec
1001	6msec
1010	7msec

Table 9. DRC Attack Time Table

Value of Register	Release time 6dB, fs = 96,000
011	5.0sec
010	2.0sec
001	1.0sec
000	0.5sec
111	0.2sec
110	0.1sec
101	0.05sec
100	0.025sec

Table 10. DRC Release Time Table

Addr 0x2C: DRC Control 2

Bit	7	6	5	4	3	2	1	0
Name	CPR_H	CTS_H						

Name	Description	Value	Meaning	Ref.
CTS_H	DRC threshold for High band	**b'0000000** ~ b'1111111	-57 ~ 12dB unsigned 7-bit DRC threshold for high band. It has effect only in 2 band mode. Refer to DRC threshold table for threshold values.	
CPR_H	DRC enable for High band	**b'0**	Dynamic Range Compression off	
		b'1	Dynamic Range Compression on	

Addr 0x2D: DRC Control 3

Bit	7	6	5	4	3	2	1	0
Name	X	C1C_H			A1C_H			

Name	Description	Value	Meaning	Ref.
A1C_H	DRC attack time (High band)	b'0000 ~ b'1010	Attack time control for high band mode. It has effect only in 2 band mode. (See DRC attack time table in Addr 0x2B.) default = **b'0001**	
C1C_H	DRC release time (High band)	**b'000** ~ b'111	Release time control for high band mode. It has effect only in 2 band mode. (See DRC release time table in Addr 0x2B.)	

Addr 0x2E: DRC Control 4

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	DLL				

Name	Description	Value	Meaning	Ref.
DLL	Delay line length	b'00000~ **b'10100**	Delay line length. 0~20(decimal)	

Addr 0x2F: DRC Control 5

Bit	7	6	5	4	3	2	1	0
Name	X	X	RSB	ASB	X	DTS	2BM	CAS

Name	Description	Value	Meaning	Ref.
CAS	Coupled All pass Structure enable	**b'0**	Enable coupled all pass structure	
		b'1	Disable coupled all pass structure	
2BM	2band mode enable	**b'0**	1 band DRC	
		b'1	2 band DRC	
DTS	LH-DRC type select	**b'0**	LH-DRC old mode	
		b'1	LH-DRC new mode	
ASB	Attack parameter select bit	**b'0**	Attack parameters in table	
		b'1	Attack parameters from external loading	
RSB	Release parameter Select bit	**b'0**	Release parameters in table	
		b'1	Release parameters from external loading	

Addr 0x30: Soft Mute On/Off Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	SM2	SM1

Name	Description	Value	Meaning	Ref.
SMn	Soft mute	b'0	increase for channel n	
		b'1	decrease for channel n	

Addr 0x31: PWM Switching On/Off Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	POF2	POF1

Name	Description	Value	Meaning	Ref.
POFn	Switching output On/off control	b'0	Channel n PWM switching on	
		b'1	Channel n PWM switching off	

Addr 0x32: PWM_MASK Control 0

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	SRD	FPMLD	PWMM	

Name	Description	Value	Meaning	Ref.
PWMM	PWM MASK register	**b'10**	PWM MASK output is low. (reset default)	
		otherwise	PWM MASK output is high.	
FPMLD	Permanent PWMMASK Low disable flag	**b'0**	No effect	
		b'1	Reset the auto PWMMASK restore counter to 0	
SRD	FAULT disable	**b'0**	FAULT is effect for PROTECT	
		b'1	FAULT is ineffective for PROTECT	

Addr 0x33: PWM_MASK Control 1

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	APM	POF

Name	Description	Value	Meaning	Ref.
POF	PWM off flag	b'0	Even if Auto PWM_MASK(PMSKn) condition is met, the PWM output of all channels is not affected.	
		b'1	When Auto PWM_MASK(PMSKn) condition is met, the PWM output of all channels goes to the defined state which is set by the PWM off state control register (Addr 0x34).	
APM	PWM_MASK flag	b'0	Even if Auto PWM_MASK(VMSKn) condition is met, the PWM_MASK output of all channels is not affected.	
		b'1	When Auto PWM_MASK(VMSKn) condition is met, the PWM_MASK output goes to Low state.	

Addr 0x34: PWM_MASK Control 2

Bit	7	6	5	4	3	2	1	0
Name	VMSK3	X	VMSK1	VMSK0	PMSK3	X	PMSK1	PMSK0

Name	Description	Value	Meaning	Ref.
PMSKn	Masking bit of PWM off control	b'0	Mask bit indicating the validity of n-th bit of Addr 0x70 system register: If the n-th bit of this register is zero, the n-th bit of Addr 0x70 system register is invalid. The n-th bit of Addr 0x70 is valid only when the n-th mask bit is one. (**Default : b'1x10**)	
		b'1		
VMSKn	Masking bit of PWM_MASK signal	b'0		
		b'1		

Addr 0x35: PWM_MASK Control 3

Bit	7	6	5	4	3	2	1	0
Name	IRC		AVRCT			PHT		

Name	Description	Value	Meaning	Ref.
PHT	PWM_MASK Low Hold Time	b'000	0.5 msec Hold Time	
		b'001	1 msec Hold Time (Default)	
		b'010	2 msec Hold Time	
		b'011	4 msec Hold Time	
		b'100	8 msec Hold Time	
		b'101	16msec Hold Time	
AVRCT	Auto PWM_MASK Restore Counter Threshold	**b'000**	2 (Default)	
		b'001	5	
		b'010	10	
		b'011	15	
		b'100	20	
		b'101	25	
		b'110	30	
		b'111	Infinity	
IRC	Auto PWM_MASK Restore Interval Ratio Control	**b'00**	2 (Default)	
		b'01	4	

Addr 0x36: PWM_MASK Control 4

Bit	7	6	5	4	3	2	1	*0*
Name	SHE	POE	X	X	X	HT2		

Name	Description	Value	Meaning	*Ref.*
HT2	Hold Time 2 apply start point (restore counter)	b'000	100msec Hold Time	
		b'001	200msec Hold Time	
		b'010	400msec Hold Time	
		b'011	600msec Hold Time	
		b'100	800msec Hold Time	
		b'101	1 sec Hold Time (Default)	
		b'110	2 sec Hold Time	
		b'111	4 sec Hold Time	
POE	PWM off when Fault detected and PWM on when PWMMASK recover	**b'0**	Disable (Default)	
		b'1	Enable	
SHE	Second Hold time Enable	b'0	Disable	
		b'1	Enable (Default)	

Addr 0x37: Soft Volume Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	SVI	

Name	Description	Value	Meaning	Ref.
SVI	Soft volume change	b'00	Medium speed	
		b'01	High speed	
		b'10	Low speed	
		b'11	soft volume change disable	

Addr 0x38: Auto-Mute Control

Bit	7	6	5	4	3	2	1	0
Name	X	EAMC	II		AT			

Name	Description	Value	Meaning	Ref.
AT	Auto-mute detection threshold	**b'0000** ~ b'1111	Unsigned integer between 0 and 15	
II	Auto-mute response time	**b'00**	5msec	
		b'01	50msec	
		b'10	500msec	
		b'11	2 sec	
EAMC	Effect of Auto-mute condition	**b'0**	Auto mute disable(No-Effect)	
		b'1	Continue switching if auto-mute	

Addr 0x39: PWM Output Port Control for PWM 1A&1B, 2A&2B

Bit	7	6	5	4	3	2	1	0
Name	OPM2B		OPM2A		OPM1B		OPM1A	

Name	Description	Value	Meaning	Ref.
OPM1A	Select source channel for PWM output port 1A	**b'00**	PWM1A is connected to PWM port 1A	
		b'01	PWM1B is connected to PWM port 1A	
		b'10	PWM2A is connected to PWM port 1A	
		b'11	PWM2B is connected to PWM port 1A	
OPM1B	Select source channel for PWM output port 1B	b'00	PWM1A is connected to PWM port 1B	
		b'01	PWM1B is connected to PWM port 1B	
		b'10	PWM2A is connected to PWM port 1B	
		b'11	PWM2B is connected to PWM port 1B	
OPM2A	Select source Channel for PWM output port 2A	b'00	PWM1A is connected to PWM port 2A	
		b'01	PWM1B is connected to PWM port 2A	
		b'10	PWM2A is connected to PWM port 2A	
		b'11	PWM2B is connected to PWM port 2A	
OPM2B	Select source channel for PWM output port 2B	b'00	PWM1A is connected to PWM port 2B	
		b'01	PWM1B is connected to PWM port 2B	
		b'10	PWM2A is connected to PWM port 2B	
		b'11	PWM2B is connected to PWM port 2B	

Addr 0x3A: Miscellaneous PWM Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	BHL	AHL	MD	

Name	Description	Value	Meaning	Ref.
MD	PWM output mode	b'00	AD mode with asynchronous signal pair	
		b'01	AD mode with synchronous signal pair	
		b'10	PWM D-BTL mode	
		b'11	AM Interference mode	
AHL	A-out state When switching off	**b'0**	Low	
		b'1	High	
BHL	B-out state when switching off	**b'0**	Low	
		b'1	High	

Addr 0x3B: I²C Glitch filter

Bit	7	6	5	4	3	2	1	0
Name	GFO	DUR						

Name	Description	Value	Meaning	Ref.
DUR	glitch width	b'0000000 ~ b'1111111	minimum pulse width = (DUR+2) * 20 ns reset default = (15+2) * 20 ns (DUR default = **0x0F,** means 17)	
GFO	Glitch filter enable/disable	**b'0**	Glitch filter on	
		b'1	Bypass	

Addr 0x3C~0x3D: PEQ Filter Control for Ch1 and Ch2 respectively

Bit	7	6	5	4	3	2	1	0
Name	X	X	BQ6	BQ5	BQ4	BQ3	BQ2	BQ1

Name	Description	Value	Meaning	Ref.
BQ1	On/off Bi-Quad 1 of ch. n (= ch. 1,2)	**b'0**	Bypass Bi-Quad 1 of channel n	
		b'1	Enable Bi-Quad 1 of channel n	
BQ2	On/off Bi-Quad 2 of ch. n (= ch. 1,2)	**b'0**	Bypass Bi-Quad 2 of channel n	
		b'1	Enable Bi-Quad 2 of channel n	
BQ3	On/off Bi-Quad 3 of ch. n (= ch. 1,2)	**b'0**	Bypass Bi-Quad 3 of channel n	
		b'1	Enable Bi-Quad 3 of channel n	
BQ4	On/off Bi-Quad 4 of ch. n (= ch. 1,2)	**b'0**	Bypass Bi-Quad 4 of channel n	
		b'1	Enable Bi-Quad 4 of channel n	
BQ5	On/off Bi-Quad 5 of ch. n (= ch. 1,2)	**b'0**	Bypass Bi-Quad 5 of channel n	
		b'1	Enable Bi-Quad 5 of channel n	
BQ6	On/off Bi-Quad 6 of ch. n (= ch. 1,2)	**b'0**	Bypass Bi-Quad 6 of channel n	
		b'1	Enable Bi-Quad 6 of channel n	

Addr 0x3E~0x3F: PEQ Filter Control 0 for Ch1 and Ch2 respectively

Bit	7	6	5	4	3	2	1	0
Name	BQ11	BQ10	X	BQ9	X	BQ8	X	BQ7

Name	Description	Value	Meaning	Ref.
BQ7	On/off Bi-Quad 7 of ch. n (= ch. 1,2)	**b'0**	Bypass Bi-Quad 7 of channel n	
		b'1	Enable Bi-Quad 7 of channel n	
BQ8	On/off Bi-Quad 8 of ch. n (= ch. 1,2)	**b'0**	Bypass Bi-Quad 8 of channel n	
		b'1	Enable Bi-Quad 8 of channel n	
BQ9	On/off Bi-Quad 9 of ch. n (= ch. 1,2)	**b'0**	Bypass Bi-Quad 9 of channel n	
		b'1	Enable Bi-Quad 9 of channel n	
BQ10	On/off Bi-Quad 10 of ch. n (= ch. 1,2)	**b'0**	Bypass Bi-Quad 10 of channel n	
		b'1	Enable Bi-Quad 10 of channel n	
BQ11	On/off Bi-Quad 11 of ch. n (= ch. 1,2)	**b'0**	Bypass Bi-Quad 11 of channel n	
		b'1	Enable Bi-Quad 11 of channel n	

Addr 0x40: PWM D-BTL Mode Control 0

Bit	7	6	5	4	3	2	1	0
Name	X	MLP						

Name	Description	Value	Meaning	Ref.
MLP	Minimum Linear pulse length	**b'0001000**	Unsigned 0~127	

Reserved Addr 0x41

Addr 0x42: PWM D-BTL Mode Control 1

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	NSS	

Name	Description	Value	Meaning	Ref.
NSS	NS Select	b'00/01	7bit NS	
		b'10	7 bit NS* 2 8bit NS	
		b'11	New 8bit NS	

Addr 0x43: PWM Phase Control

Bit	7	6	5	4	3	2	1	0
Name	PPC				PFC			

Name	Description	Value	Meaning	Ref.
PFC	PWM phase Fine Control	**b'0000** ~ b'1001	Range is 0°~14.94° with 1.66° step	In Single ended mode, fixed as PFC = b'0000, and PPC = b' 0110 (90°)
PPC	PWM Phase Control	b'0000 ~ b'1100	Range is 0°~180° with 15° step. default = **b'0110** (90°)	

Addr 0x44: PWM Soft Start Control

Bit	7	6	5	4	3	2	1	0
Name	PSE	SRT						

Name	Description	Value	Meaning	Ref.
PSE	PWM soft start Enable	**b'0**	Disable (Default)	
		b'1	Enable (only under AD mode)	
SRT	Step Repeat Time	b'000000 ~ b'111111	The repeat time of each step (default = **16** : means repeat 17 times)	

Addr 0x45: Modulation Index & NS-Type Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	FB	M0		NTF_Ord	MD12	

Name	Description	Value	Meaning	Ref.
MD12	Modulation index control by Minimum pulse width for Ch 1&2	**b'11**	Minimum pulse width = 2	
		b'10	Minimum pulse width = 4	
		b'01	Minimum pulse width = 6	
		b'00	Minimum pulse width = 8	
NTF_Ord	Select NTF Order	**b'0**	NTF Coeff. = 4th Order at WCK 48kHz	
		b'1	NTF Coeff. = 4th Order at WCK 96kHz (possible to configure any 5 coefficients of NTF through external loading)	
M0	Dither Position Selector	**b'00**	No left shift on dither value = Dither off	
		b'01	1bit left shift on dither value	
		b'10	2bit left shift on dither value	
		b'11	3bit left shift on dither value	
FB	Feed Back on/off	b'0	NS Feed Back off	
		b'1	NS Feed Back on	

Addr 0x46: NS Feedback Limit Control

Bit	7	6	5	4	3	2	1	0
Name	X	FBMAX						

Name	Description	Value	Meaning	Ref.
FBMAX	Feedback on/off	b'0000000 ~b'1111111	Feedback limit, default = **0x04**	

Addr 0x47: SSRC Control 0

Bit	7	6	5	4	3	2	1	0
Name	X	X	DCESW	X	FSFHM	FSFSM	X	X

Name	Description	Value	Meaning	Ref.
FSFSM	frequency stable effect on soft mute flag	**b'0**	no effect on soft mute flag	
		b'1	soft mute flag = 1 when unstable state	
FSFHM	frequency stable effect on hard mute flag	**b'0**	no effect on hard mute flag	
		b'1	hard mute flag = 1 when unstable state	
DCESW	DC Check Enable of SRC WCK	b'0	DC Check Disable in SRC WCK	
		b'1	DC Check Enable in SRC WCK	

Addr 0x48: SSRC Control 1

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	FVT			

Name	Description	Value	Meaning	Ref.
FVT	Frequency variation threshold	b'0000 ~ b'1111	Threshold value for Frequency stable check (unsigned integer) default = **b'0111**	

Addr 0x49: NS Soft Mute Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	Time_Lim	Enable	CNT_THR			

Name	Description	Value	Meaning	Ref.
CNT_THR	Minimum counting value	b'0000 ~ b'1111	Minimum counting value of continuous zeros for forcing NS_OUT as 0. default = **b'0110**	
Enable	Enable NS soft mute	**b'0**	Disable	
		b'1	Enable	
Time_Lim	Time limit on finding continuous zeros	**b'0**	Time Limit = 200ms	
		b'1	Time Limit = 400ms	

Reserved Addr 0x4A

Addr 0x4B: I^2S WCK Max Ratio

Bit	7	6	5	4	3	2	1	0
Name	I^2S MAX							

Name	Description	Value	Meaning	Ref.
I^2S MAX	I^2S MAX Value	**h'47**	Maximum limit value for I^2S Ratio	

Addr 0x4C: I^2S WCK Min Ratio

Bit	7	6	5	4	3	2	1	0
Name	I^2S MIN							

Name	Description	Value	Meaning	Ref.
I^2S MIN	I^2S MIN Value	**h'3A**	Minimum limit value for I^2S Ratio	

Addr 0x4D: I^2S BCK Max Ratio

Bit	7	6	5	4	3	2	1	0
Name	I^2S MAX							

Name	Description	Value	Meaning	Ref.
I^2S MAX	I^2S MAX Value	**h'12**	Maximum limit value for I^2S Ratio	

Addr 0x4E: I^2S BCK Min Ratio

Bit	7	6	5	4	3	2	1	0
Name	I^2S MIN							

Name	Description	Value	Meaning	Ref.
I^2S MIN	I^2S MIN Value	**h'0D**	Minimum limit value for I^2S Ratio	

Addr 0x4F: PWM_MASK Control 5

Bit	7	6	5	4	3	2	1	0
Name	X	VMSK2	VMSK1	VMSK0	X	PMSK2	PMSK1	PMSK0

Name	Description	Value	Meaning	Ref.
PMSK	Masking bit of PWM off control	b'0 b'1	Mask bit indicating the validity of n-th bit of Addr 0x50 system register: If the n-th bit of this register is zero, the n-th bit of Addr 0x50 system register is invalid. The n-th bit of Addr 0x50 is valid only when the n-th mask bit is one. (**Default :b'x001**)	
VMSK	Masking bit of PWM_MASK signal	b'0 b'1		

Addr 0x50: Watch Dog Error System Status (read-only)

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	INF	X	IWK	IBK	WDE

Name	Description	Value	Meaning	Ref.
WDE	Watch Dog Ratio Error	b'0		
		b'1	Watch Dog Error	
IBK	IIS BCK Ratio Error	b'0		
		b'1	IIS BCK Ratio Error	
IWK	IIS WCK Ratio Error	b'0		
		b'1	IIS WCK Ratio Error	
INF	Inferno(BCK Error) Flag	b'0		
		b'1	Inferno(BCK Error) Flag. Set modulator reset(Addr 0x02) active to clear this flag.	

Addr 0x51: Monitoring Range Control of Abnomal Reference Clock

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	DIS		

Name	Description	Value	Meaning	Ref.
DIS	Deviation for inferno state	b'000 ~ b'111	default = **b'100** (detect 40% increase of BCK)	

Reserved Addr 0x52

Addr 0x53: Power Meter Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	PDPOS	X	X	PDCH	

Name	Description	Value	Meaning	Ref.
PDCH	Power meter Detect Channel	**b'00**	L+R/2 (default)	
		b'01	L channel	
		b'10	R channel	
		b'11	reserved	
PDPOS	Power meter Detect Position	**b'0**	After volume (default)	
		b'1	Before volume	

Addr 0x54: Power Meter (read-only)

Bit	7	6	5	4	3	2	1	0
Name	POWERMETER							

Name	Description	Value	Meaning	Ref.
POWER METER	POWERMETER	0x00		

Reserved Addr 0x55 ~ 0x5A

Addr 0x5B: System Status Register (0x01) Holding Control 0

Bit	7	6	5	4	3	2	1	0
Name	X	HDRCCHK	HPEQCHK	X	HCurrent	HTEMP	X	HULCK

Name	Description	Value	Meaning	Ref.
HULCK	Enable bit of Holding the ULCK status	**b'0**	Update the new value without holding the ULCK status bit of 0x01	
		b'1	Hold the first different value	
HTEMP	Enable bit of Holding the TEMP status	**b'0**	Update the new value without holding the TEMP status bit of 0x01	
		b'1	Hold the first different value	
HCurrent	Enable bit of Holding the Current status	**b'0**	Update the new value without holding the Current status bit of 0x01	
		b'1	Hold the first different value	
HPEQCHK	Enable bit of Holding the PEQCHK status	**b'0**	Update the new value without holding the PEQCHK status bit of 0x01	
		b'1	Hold the first different value	
HDRCCHK	Enable bit of Holding the DRCCHK status	**b'0**	Update the new value without holding the DRCCHK status bit of 0x01	
		b'1	Hold the first different value	

Addr 0x5C: System Status Register (0x50, 0x70) Holding Control 1

Bit	7	6	5	4	3	2	1	0
Name	X	HIWK	HIBK	HWDE	HMPW	X	HULCK	X

Name	Description	Value	Meaning	Ref.
HULCK	Enable bit of Holding the ULCK status	**b'0**	Update the new value without holding the ULCK status bit of 0x70	
		b'1	Hold the first different value	
HMPW	Enable bit of Holding the MPW status	**b'0**	Update the new value without holding the MPW status bit of 0x70	
		b'1	Hold the first different value	
HWDE	Enable bit of Holding the WDE status	**b'0**	Update the new value without holding the WDE status bit of 0x50	
		b'1	Hold the first different value	
HIBK	Enable bit of Holding the IBK status	**b'0**	Update the new value without holding the IBK status bit of 0x50	
		b'1	Hold the first different value	
HIWK	Enable bit of Holding the IWK status	**b'0**	Update the new value without holding the IWK status bit of 0x50	
		b'1	Hold the first different value	

Addr 0x5D: Checksum Download Type Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	X	CDT

Name	Description	Value	Meaning	Ref.
CDT	Checksum download type	**b'0**	1byte * 4 (addr 0x56~0x59,0x63~0x66 0x67~0x6A)	
		b'1	4byte (Coefficient mode)	

Addr 0x5E: Shut Down Reset Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	SDR_EN	SDR_CON	

Name	Description	Value	Meaning	*Ref.*
SDR_EN	SDR Enable	**b'0**	Disable	
		b'1	Enable	
SDR_CON	Voltage detect level	b'00	2.4V	
		b'01	2.5V	
		b'10	2.6V	
		b'11	2.7V	

Addr 0x5F: Monitor

Bit	7	6	5	4	3	2	1	*0*
Name	X				Monitor0			

Name	Description	Value	Meaning	*Ref.*
Monitor0		b'0000	SOFT_RESET => Monitor0 pin	
		b'0001	PWM1A => Monitor0 pin	
		b'0010	PWM1B => Monitor0 pin	
		b'0011	PWM2A => Monitor0 pin	
		b'0100	PWM2B => Monitor0 pin	
		b'0101	PWM_MASK => Monitor0 pin	
		b'0111	IIS GEN SDATAOUT => Monitor 0 pin	

Addr 0x60: AD DC Protection Control 0

Bit	7	6	5	4	3	2	1	0
Name	PDH				PDL			

Name	Description	Value	Meaning	Ref.
PDL	PWM Duty Low	b'0000	40%	
		b'0001	35%	
		b'0010	30%	
		b'0011	25%	
		b'0100	20%	
		b'0101	15%	
		b'0110	10%	
		b'0111	5%	
		b'1000	45%	
PDH	PWM Duty High	b'0000	60%	
		b'0001	65%	
		b'0010	70%	
		b'0011	75%	
		b'0100	80%	
		b'0101	85%	
		b'0110	90%	
		b'0111	95%	
		b'1000	55%	

Addr 0x61: D-BTL DC Protection Control 1

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	MLPA			

Name	Description	Value	Meaning	Ref.
MLPA	D-BTL Duty MLP	**b'0000**	5%	
		b'0001	10%	
		b'0010	15%	
		b'0011	20%	
		b'0100	25%	
		b'0101	30%	
		b'0110	35%	
		b'0111	40%	
		b'1000	45%	
		b'1001	50%	

Addr 0x62: DC Protection Control 2

Bit	7	6	5	4	3	2	1	0
Name	SRE	SRF	X	X	X	PFE	DFE	MFE

Name	Description	Value	Meaning	Ref.
MFE	Modulation Index Error Enable	**b'0**	Modulation Index Error Disable	
		b'1	Modulation Index Error Enable	
DFE	MDRC Coefficient Error Enable	**b'0**	MDRC Coefficient Error Disable	
		b'1	MDRC Coefficient Error Enable	
PFE	PEQ1-12 Coefficient Error Enable	**b'0**	PEQ1-12 Coefficient Error Disable	
		b'1	PEQ1-12 Coefficient Error Enable	
SRF	DC Soft Reset Flag	**b'0**		
		b'1	DC Soft Reset start in Modulation	
SRE	DC Soft Reset Enable	**b'0**	DC Soft Reset Flag Disable	
		b'1	DC Soft Reset Flag Enable	

Addr 0x63: DC Protection Control 3

Bit	7	6	5	4	3	2	1	0
Name	X	X	PCS3					

Name	Description	Value	Meaning	Ref.
PCS3	PEQ1-12 RX Checksum(29:24)		**default = 0x00**	

Addr 0x64: DC Protection Control 4

Bit	7	6	5	4	3	2	1	0
Name	PCS2							

Name	Description	Value	Meaning	Ref.
PCS2	PEQ1-12 RX Checksum (23:16)		**default = 0x00**	

Addr 0x65: DC Protection Control 5

Bit	7	6	5	4	3	2	1	0
Name	PCS1							

Name	Description	Value	Meaning	Ref.
PCS1	PEQ1-12 RX Checksum (15:8)		**default = 0x00**	

Addr 0x66: DC Protection Control 6

Bit	7	6	5	4	3	2	1	0
Name	PCS0							

Name	Description	Value	Meaning	Ref.
PCS0	PEQ1-12 RX Checksum (7:0)		**default = 0x00**	

Addr 0x67: DC Protection Control 7

Bit	7	6	5	4	3	2	1	0
Name	X	X	DCS3					

Name	Description	Value	Meaning	Ref.
DCS3	MDRC RX Checksum (29:24)		**default = 0x1D**	

Addr 0x68: DC Protection Control 8

Bit	7	6	5	4	3	2	1	0
Name	DCS2							

Name	Description	Value	Meaning	Ref.
DCS2	MDRC RX Checksum (23:16)		**default = 0x42**	

Addr 0x69: DC Protection Control 9

Bit	7	6	5	4	3	2	1	0
Name	DCS1							

Name	Description	Value	Meaning	Ref.
DCS1	MDRC RX Checksum (15:8)		**default = 0xF0**	

Addr 0x6A: DC Protection Control 10

Bit	7	6	5	4	3	2	1	0
Name	DCS0							

Name	Description	Value	Meaning	Ref.
DCS0	MDRC RX Checksum (7:0)		**default = 0x70**	

Addr 0x6B: DC Protection Control 11 (read-only)

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	PEF	DEF	MEF

Name	Description	Value	Meaning	Ref.
MEF	Modulation Index Error Flag	**b'0**		
		b'1	Modulation Index Error	
DEF	MDRC Coefficient Error Flag	**b'0**		
		b'1	MDRC Coefficient Error	
PEF	PEQ Coefficient Error Flag	**b'0**		
		b'1	PEQ Coefficient Error	

Addr 0x6C: POP Control 0

Bit	7	6	5	4	3	2	1	0
Name	RST							

Name	Description	Value	Meaning	Ref.
RST	Release Time	**unsigned 0x10**	CLK error should not occur during RST Unit in 10msec	

Addr 0x6D: POP Control 1

Bit	7	6	5	4	3	2	1	0
Name	ULM[15:8]							

Name	Description	Value	Meaning	Ref.
ULM		**unsigned 0x00**	Upper limit on ratio of BCK to CLK_FR_4	

Addr 0x6E: POP Control 2

Bit	7	6	5	4	3	2	1	0
Name	ULM[7:0]							

Name	Description	Value	Meaning	Ref.
ULM	Upper Limit	**unsigned 0x20**	Upper limit on ratio of BCK to CLK_FR_4	

Addr 0x6F: POP Control 3

Bit	7	6	5	4	3	2	1	0
Name	LLM[3:0]				0	0	0	WON

Name	Description	Value	Meaning	Ref.
LLM	Lower Limit	**unsigned b'1001**	Lower limit on ratio of BCK to CLK_FR_4	
WON	Watch-dog On	b'0	OFF	
		b'1	ON	

Addr 0x70 System Error Status (read-only)

Bit	7	6	5	4	3	2	1	0
Name	FSI		X	X	MPW	X	ULCK	PPM

Name	Description	Value	Meaning	Ref.
PPM	Permanent PWMMASK Indication flag	b'0		
		b'1	Indicated that PWM_MASK is in Permanent LOW state	
ULCK	Sampled PLL Unlock error	b'0	PLL is locked state.	
		b'1	PLL is unlocked state.	
MPW	MCK/WCK Ratio error	b'0	Ratio is incorrect.	
		b'1	Ratio is correct.	
FSI	Sampling Frequency Information	b'00	48 kHz (44.1kHz)	
		b'01	96 kHz	
		b'10	32 kHz	

Reserve Addr 0x71

Addr 0x72: I^2S Glitch Filter

Bit	7	6	5	4	3	2	1	0
Name	GFE	WTH						

Name	Description	Value	Meaning	Ref.
WTH	glitch width	b'0000000 ~ b'1111111	minimum pulse width =(WTH+2) * 10 ns reset default = (1+2) * 10 ns (WTH default =**0x01,** means 3)	
GFE	Glitch filter enable/disable	b'0	Glitch filter on	
		b'1	Bypass	

Reserve Addr 0x73 ~ 0x7B

Addr 0x7C: IIS Sdata_Out Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	X	OUT_SEL

Name	Description	Value	Meaning	Ref.
OUT_SEL	Select data for IIS OUT	**b'0**	Data after soft mute stage is selected	
		b'1	Data before EQ stage is selected	

Reserve Addr 0x7D

Addr 0x7E: Bi-Quad Filter Control 3

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	X	WR_EN

Name	Description	Value	Meaning	Ref.
WR_EN	Coefficient write Enable	**b'0**	Disable coefficient write for ch1/ch2	
		b'1	Enable coefficient write for ch1/ch2	

Coefficient Register Mode:

0x00 ~ 0x27 :	BQ1 ~ 5, BQ7 ~ 9
0x28 ~ 0x3B :	QMF_BQ1 ~ 4
0x41 :	Power Meter Gain
0x42 ~ 0X43 :	PEQ Checksum, DRC Checksum
0x45 ~ 0x4E :	BQ10 ~ 11
0x4F ~ 0x53 :	BQ6
0x54 ~ 0x62 :	BQ12 ~ 14

B. Configuration Register Value Reference

Table 11. Master Volume

Index	dB	Index	dB	Index	dB	Index	dB	Index	dB	Index	dB
0xFF	0.0	0xD4	-21.5	0xA9	-43.0	0x7E	-64.5	0x53	-86.0	0x28	-107.5
0xFE	-0.5	0xD3	-22.0	0xA8	-43.5	0x7D	-65.0	0x52	-86.5	0x27	-108.0
0xFD	-1.0	0xD2	-22.5	0xA7	-44.0	0x7C	-65.5	0x51	-87.0	0x26	-108.5
0xFC	-1.5	0xD1	-23.0	0xA6	-44.5	0x7B	-66.0	0x50	-87.5	0x25	-109.0
0xFB	-2.0	0xD0	-23.5	0xA5	-45.0	0x7A	-66.5	0x4F	-88.0	0x24	-109.5
0xFA	-2.5	0xCF	-24.0	0xA4	-45.5	0x79	-67.0	0x4E	-88.5	0x23	-110.0
0xF9	-3.0	0xCE	-24.5	0xA3	-46.0	0x78	-67.5	0x4D	-89.0	0x22	-110.5
0xF8	-3.5	0xCD	-25.0	0xA2	-46.5	0x77	-68.0	0x4C	-89.5	0x21	-111.0
0xF7	-4.0	0xCC	-25.5	0xA1	-47.0	0x76	-68.5	0x4B	-90.0	0x20	-111.5
0xF6	-4.5	0xCB	-26.0	0xA0	-47.5	0x75	-69.0	0x4A	-90.5	0x1F	-112.0
0xF5	-5.0	0xCA	-26.5	0x9F	-48.0	0x74	-69.5	0x49	-91.0	0x1E	-112.5
0xF4	-5.5	0xC9	-27.0	0x9E	-48.5	0x73	-70.0	0x48	-91.5	0x1D	-113.0
0xF3	-6.0	0xC8	-27.5	0x9D	-49.0	0x72	-70.5	0x47	-92.0	0x1C	-113.5
0xF2	-6.5	0xC7	-28.0	0x9C	-49.5	0x71	-71.0	0x46	-92.5	0x1B	-114.0
0xF1	-7.0	0xC6	-28.5	0x9B	-50.0	0x70	-71.5	0x45	-93.0	0x1A	-114.5
0xF0	-7.5	0xC5	-29.0	0x9A	-50.5	0x6F	-72.0	0x44	-93.5	0x19	-115.0
0xEF	-8.0	0xC4	-29.5	0x99	-51.0	0x6E	-72.5	0x43	-94.0	0x18	-115.5
0xEE	-8.5	0xC3	-30.0	0x98	-51.5	0x6D	-73.0	0x42	-94.5	0x17	-116.0
0xED	-9.0	0xC2	-30.5	0x97	-52.0	0x6C	-73.5	0x41	-95.0	0x16	-116.5
0xEC	-9.5	0xC1	-31.0	0x96	-52.5	0x6B	-74.0	0x40	-95.5	0x15	-117.0
0xEB	-10.0	0xC0	-31.5	0x95	-53.0	0x6A	-74.5	0X3F	-96.0	0x14	-117.5
0xEA	-10.5	0xBF	-32.0	0x94	-53.5	0x69	-75.0	0X3E	-96.5	0x13	-118.0
0xE9	-11.0	0xBE	-32.5	0x93	-54.0	0x68	-75.5	0X3D	-97.0	0x12	-118.5
0xE8	-11.5	0xBD	-33.0	0x92	-54.5	0x67	-76.0	0X3C	-97.5	0x11	-119.0
0xE7	-12.0	0xBC	-33.5	0x91	-55.0	0x66	-76.5	0X3B	-98.0	0x10	-119.5
0xE6	-12.5	0xBB	-34.0	0x90	-55.5	0x65	-77.0	0X3A	-98.5	0x0F	-120.0
0xE5	-13.0	0xBA	-34.5	0x8F	-56.0	0x64	-77.5	0X39	-99.0	0x0E	-120.5
0xE4	-13.5	0xB9	-35.0	0x8E	-56.5	0x63	-78.0	0X38	-99.5	0x0D	-121.0
0xE3	-14.0	0xB8	-35.5	0x8D	-57.0	0x62	-78.5	0X37	-100.0	0x0C	-121.5
0xE2	-14.5	0xB7	-36.0	0x8C	-57.5	0x61	-79.0	0X36	-100.5	0x0B	-122.0
0xE1	-15.0	0xB6	-36.5	0x8B	-58.0	0x60	-79.5	0X35	-101.0	0x0A	-122.5
0xE0	-15.5	0xB5	-37.0	0x8A	-58.5	0x5F	-80.0	0X34	-101.5	0x09	-123.0
0xDF	-16.0	0xB4	-37.5	0x89	-59.0	0x5E	-80.5	0X33	-102.0	0x08	-123.5
0xDE	-16.5	0xB3	-38.0	0x88	-59.5	0x5D	-81.0	0X32	-102.5	0x07	-124.0
0xDD	-17.0	0xB2	-38.5	0x87	-60.0	0x5C	-81.5	0X31	-103.0	0x06	-124.5
0xDC	-17.5	0xB1	-39.0	0x86	-60.5	0x5B	-82.0	0X30	-103.5	0x05	-125.0
0xDB	-18.0	0xB0	-39.5	0x85	-61.0	0x5A	-82.5	0x2F	-104.0	0x04	-125.5
0xDA	-18.5	0xAF	-40.0	0x84	-61.5	0x59	-83.0	0x2E	-104.5	0x03	NA
0xD9	-19.0	0xAE	-40.5	0x83	-62.0	0x58	-83.5	0x2D	-105.0	0x02	NA
0xD8	-19.5	0xAD	-41.0	0x82	-62.5	0x57	-84.0	0x2C	-105.5	0x01	NA
0xD7	-20.0	0xAC	-41.5	0x81	-63.0	0x56	-84.5	0x2B	-106.0	0x00	NA
0xD6	-20.5	0xAB	-42.0	0x80	-63.5	0x55	-85.0	0x2A	-106.5		
0xD5	-21.0	0xAA	-42.5	0x7F	-64.0	0x54	-85.5	0x29	-107.0		

Table 12. Channel Volume

Index	dB	Index	dB	Index	dB	Index	dB	Index	dB	Index	dB
0xFF	48.0	0xD4	26.5	0xA9	5.0	0x7E	-16.5	0x53	-38.0	0x28	-59.5
0xFE	47.5	0xD3	26.0	0xA8	4.5	0x7D	-17.0	0x52	-38.5	0x27	-60.0
0xFD	47.0	0xD2	25.5	0xA7	4.0	0x7C	-17.5	0x51	-39.0	0x26	-60.5
0xFC	46.5	0xD1	25.0	0xA6	3.5	0x7B	-18.0	0x50	-39.5	0x25	-61.0
0xFB	46.0	0xD0	24.5	0xA5	3.0	0x7A	-18.5	0x4F	-40.0	0x24	-61.5
0xFA	45.5	0xCF	24.0	0xA4	2.5	0x79	-19.0	0x4E	-40.5	0x23	-62.0
0xF9	45.0	0xCE	23.5	0xA3	2.0	0x78	-19.5	0x4D	-41.0	0x22	-62.5
0xF8	44.5	0xCD	23.0	0xA2	1.5	0x77	-20.0	0x4C	-41.5	0x21	-63.0
0xF7	44.0	0xCC	22.5	0xA1	1.0	0x76	-20.5	0x4B	-42.0	0x20	-63.5
0xF6	43.5	0xCB	22.0	0xA0	0.5	0x75	-21.0	0x4A	-42.5	0x1F	-64.0
0xF5	43.0	0xCA	21.5	0x9F	0.0	0x74	-21.5	0x49	-43.0	0x1E	-64.5
0xF4	42.5	0xC9	21.0	0x9E	-0.5	0x73	-22.0	0x48	-43.5	0x1D	-65.0
0xF3	42.0	0xC8	20.5	0x9D	-1.0	0x72	-22.5	0x47	-44.0	0x1C	-65.5
0xF2	41.5	0xC7	20.0	0x9C	-1.5	0x71	-23.0	0x46	-44.5	0x1B	-66.0
0xF1	41.0	0xC6	19.5	0x9B	-2.0	0x70	-23.5	0x45	-45.0	0x1A	-66.5
0xF0	40.5	0xC5	19.0	0x9A	-2.5	0x6F	-24.0	0x44	-45.5	0x19	-67.0
0xEF	40.0	0xC4	18.5	0x99	-3.0	0x6E	-24.5	0x43	-46.0	0x18	-67.5
0xEE	39.5	0xC3	18.0	0x98	-3.5	0x6D	-25.0	0x42	-46.5	0x17	-68.0
0xED	39.0	0xC2	17.5	0x97	-4.0	0x6C	-25.5	0x41	-47.0	0x16	-68.5
0xEC	38.5	0xC1	17.0	0x96	-4.5	0x6B	-26.0	0x40	-47.5	0x15	-69.0
0xEB	38.0	0xC0	16.5	0x95	-5.0	0x6A	-26.5	0X3F	-48.0	0x14	-69.5
0xEA	37.5	0xBF	16.0	0x94	-5.5	0x69	-27.0	0X3E	-48.5	0x13	-70.0
0xE9	37.0	0xBE	15.5	0x93	-6.0	0x68	-27.5	0X3D	-49.0	0x12	-70.5
0xE8	36.5	0xBD	15.0	0x92	-6.5	0x67	-28.0	0X3C	-49.5	0x11	-71.0
0xE7	36.0	0xBC	14.5	0x91	-7.0	0x66	-28.5	0X3B	-50.0	0x10	-71.5
0xE6	35.5	0xBB	14.0	0x90	-7.5	0x65	-29.0	0X3A	-50.5	0x0F	-72.0
0xE5	35.0	0xBA	13.5	0x8F	-8.0	0x64	-29.5	0X39	-51.0	0x0E	-72.5
0xE4	34.5	0xB9	13.0	0x8E	-8.5	0x63	-30.0	0X38	-51.5	0x0D	-73.0
0xE3	34.0	0xB8	12.5	0x8D	-9.0	0x62	-30.5	0X37	-52.0	0x0C	-73.5
0xE2	33.5	0xB7	12.0	0x8C	-9.5	0x61	-31.0	0X36	-52.5	0x0B	-74.0
0xE1	33.0	0xB6	11.5	0x8B	-10.0	0x60	-31.5	0X35	-53.0	0x0A	-74.5
0xE0	32.5	0xB5	11.0	0x8A	-10.5	0x5F	-32.0	0X34	-53.5	0x09	-75.0
0xDF	32.0	0xB4	10.5	0x89	-11.0	0x5E	-32.5	0X33	-54.0	0x08	-75.5
0xDE	31.5	0xB3	10.0	0x88	-11.5	0x5D	-33.0	0X32	-54.5	0x07	-76.0
0xDD	31.0	0xB2	9.5	0x87	-12.0	0x5C	-33.5	0X31	-55.0	0x06	-76.5
0xDC	30.5	0xB1	9.0	0x86	-12.5	0x5B	-34.0	0X30	-55.5	0x05	-77.0
0xDB	30.0	0xB0	8.5	0x85	-13.0	0x5A	-34.5	0x2F	-56.0	0x04	-77.5
0xDA	29.5	0xAF	8.0	0x84	-13.5	0x59	-35.0	0x2E	-56.5	0x03	-78.0
0xD9	29.0	0xAE	7.5	0x83	-14.0	0x58	-35.5	0x2D	-57.0	0x02	-78.5
0xD8	28.5	0xAD	7.0	0x82	-14.5	0x57	-36.0	0x2C	-57.5	0x01	-79.0
0xD7	28.0	0xAC	6.5	0x81	-15.0	0x56	-36.5	0x2B	-58.0	0x00	-295.0
0xD6	27.5	0xAB	6.0	0x80	-15.5	0x55	-37.0	0x2A	-58.5		
0xD5	27.0	0xAA	5.5	0x7F	-16.0	0x54	-37.5	0x29	-59.0		

Table 13. Mixer Gain & Polarity

Index	Polarity	dB	Index	Polarity	dB	Index	Polarity	dB	Index	Polarity	dB
7E	+	18	7D	-	18	3E	+	-4	3D	-	-4
7C	+	17	7B	-	17	3C	+	-4.5	3B	-	-4.5
7A	+	16	79	-	16	3A	+	-5	39	-	-5
78	+	15	77	-	15	38	+	-5.5	37	-	-5.5
76	+	14	75	-	14	36	+	-6	35	-	-6
74	+	13	73	-	13	34	+	-7	33	-	-7
72	+	12	71	-	12	32	+	-8	31	-	-8
70	+	11	6F	-	11	30	+	-9	2F	-	-9
6E	+	10	6D	-	10	2E	+	-10	2D	-	-10
6C	+	9	6B	-	9	2C	+	-11	2B	-	-11
6A	+	8	69	-	8	2A	+	-12	29	-	-12
68	+	7	67	-	7	28	+	-13	27	-	-13
66	+	6	65	-	6	26	+	-14	25	-	-14
64	+	5.5	63	-	5.5	24	+	-15	23	-	-15
62	+	5	61	-	5	22	+	-16	21	-	-16
60	+	4.5	5F	-	4.5	20	+	-17	1F	-	-17
5E	+	4	5D	-	4	1E	+	-18	1D	-	-18
5C	+	3.5	5B	-	3.5	1C	+	-19	1B	-	-19
5A	+	3	59	-	3	1A	+	-20	19	-	-20
58	+	2.5	57	-	2.5	18	+	-21	17	-	-21
56	+	2	55	-	2	16	+	-22	15	-	-22
54	+	1.5	53	-	1.5	14	+	-23	13	-	-23
52	+	1	51	-	1	12	+	-24	11	-	-24
50	+	0.5	4F	-	0.5	10	+	-25	0F	-	-25
4E	+	0	4D	-	0	0E	+	-26	0D	-	-26
4C	+	-0.5	4B	-	-0.5	0C	+	-27	0B	-	-27
4A	+	-1	49	-	-1	0A	+	-28	09	-	-28
48	+	-1.5	47	-	-1.5	08	+	-29	07	-	-29
46	+	-2	45	-	-2	06	+	-30	05	-	-30
44	+	-2.5	43	-	-2.5	04	+	-31	03	-	-31
42	+	-3	41	-	-3	02	+	-32	01	-	-32
40	+	-3.5	3F	-	-3.5	00	+	-150			

Table 14. Dynamic Range Control Threshold

dB	Value	dB	Value	dB	Value	dB	Value
-57	FF	-5.5	DF	-2.3	BF	0.9	9F
-54	FE	-5.4	DE	-2.2	BE	1	9E
-51	FD	-5.3	DD	-2.1	BD	1.25	9D
-48	FC	-5.2	DC	-2	BC	1.5	9C
-45	FB	-5.1	DB	-1.9	BB	1.75	9B
-42	FA	-5	DA	-1.8	BA	2	9A
-39	F9	-4.9	D9	-1.7	B9	2.25	99
-36	F8	-4.8	D8	-1.6	B8	2.5	98
-33	F7	-4.7	D7	-1.5	B7	2.75	97
-30	F6	-4.6	D6	-1.4	B6	3	96
-27	F5	-4.5	D5	-1.3	B5	3.25	95
-24	F4	-4.4	D4	-1.2	B4	3.5	94
-21	F3	-4.3	D3	-1.1	B3	3.75	93
-18	F2	-4.2	D2	-1	B2	4	92
-15	F1	-4.1	D1	-0.9	B1	4.25	91
-12	F0	-4	D0	-0.8	B0	4.5	90
-11.5	EF	-3.9	CF	-0.7	AF	4.75	8F
-11	EE	-3.8	CE	-0.6	AE	5	8E
-10.5	ED	-3.7	CD	-0.5	AD	5.5	8D
-10	EC	-3.6	CC	-0.4	AC	6	8C
-9.5	EB	-3.5	CB	-0.3	AB	6.5	8B
-9	EA	-3.4	CA	-0.2	AA	7	8A
-8.5	E9	-3.3	C9	-0.1	A9	7.5	89
-8	E8	-3.2	C8	0	A8	8	88
-7.5	E7	-3.1	C7	0.1	A7	8.5	87
-7	E6	-3	C6	0.2	A6	9	86
-6.5	E5	-2.9	C5	0.3	A5	9.5	85
-6	E4	-2.8	C4	0.4	A4	10	84
-5.9	E3	-2.7	C3	0.5	A3	10.5	83
-5.8	E2	-2.6	C2	0.6	A2	11	82
-5.7	E1	-2.5	C1	0.7	A1	11.5	81
-5.6	E0	-2.4	C0	0.8	A0	12	80

※ CPR bit(MSB) = 1

Table 15. Auto Mute Detection Threshold Table

Name	Description	Value	dB
AT	Auto-mute Detection threshold	0000	-120
		0001	-114
		0010	-108
		0011	-102
		0100	-96
		0101	-90
		0110	-84
		0111	-78
		1000	-72
		1001	-66
		1010	-60
		1011	-54
		1100	-48
		1101	-42
		1110	-36
		1111	**Auto-mute**

※ Do not use value 1111.

Table 16. Power Meter Reading Table

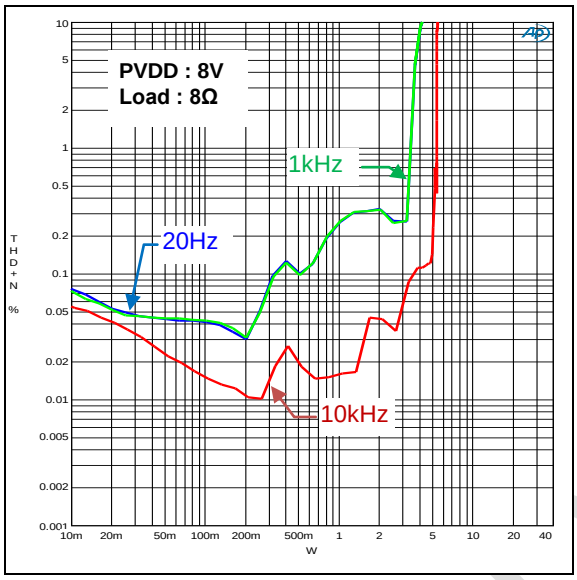
addr 0x54 (Decimal)	addr 0x54 (Hex)	dB	addr 0x54 (Decimal)	addr 0x54 (Hex)	dB	addr 0x54 (Decimal)	addr 0x54 (Hex)	dB	addr 0x54 (Decimal)	addr 0x54 (Hex)	dB
0	0x00	-48.2 under	64	0x40	-12.0	128	0x80	-6.0	192	0xC0	-2.5
1	0x01	-48.2	65	0x41	-11.9	129	0x81	-6.0	193	0xC1	-2.5
2	0x02	-42.1	66	0x42	-11.8	130	0x82	-5.9	194	0xC2	-2.4
3	0x03	-38.6	67	0x43	-11.6	131	0x83	-5.8	195	0xC3	-2.4
4	0x04	-36.1	68	0x44	-11.5	132	0x84	-5.8	196	0xC4	-2.3
5	0x05	-34.2	69	0x45	-11.4	133	0x85	-5.7	197	0xC5	-2.3
6	0x06	-32.6	70	0x46	-11.3	134	0x86	-5.6	198	0xC6	-2.2
7	0x07	-31.3	71	0x47	-11.1	135	0x87	-5.6	199	0xC7	-2.2
8	0x08	-30.1	72	0x48	-11.0	136	0x88	-5.5	200	0xC8	-2.1
9	0x09	-29.1	73	0x49	-10.9	137	0x89	-5.4	201	0xC9	-2.1
10	0x0A	-28.2	74	0x4A	-10.8	138	0x8A	-5.4	202	0xCA	-2.1
11	0x0B	-27.3	75	0x4B	-10.7	139	0x8B	-5.3	203	0xCB	-2.0
12	0x0C	-26.6	76	0x4C	-10.5	140	0x8C	-5.2	204	0xCC	-2.0
13	0x0D	-25.9	77	0x4D	-10.4	141	0x8D	-5.2	205	0xCD	-1.9
14	0x0E	-25.2	78	0x4E	-10.3	142	0x8E	-5.1	206	0xCE	-1.9
15	0x0F	-24.6	79	0x4F	-10.2	143	0x8F	-5.1	207	0xCF	-1.8
16	0x10	-24.1	80	0x50	-10.1	144	0x90	-5.0	208	0xD0	-1.8
17	0x11	-23.6	81	0x51	-10.0	145	0x91	-4.9	209	0xD1	-1.8
18	0x12	-23.1	82	0x52	-9.9	146	0x92	-4.9	210	0xD2	-1.7
19	0x13	-22.6	83	0x53	-9.8	147	0x93	-4.8	211	0xD3	-1.7
20	0x14	-22.1	84	0x54	-9.7	148	0x94	-4.8	212	0xD4	-1.6
21	0x15	-21.7	85	0x55	-9.6	149	0x95	-4.7	213	0xD5	-1.6
22	0x16	-21.3	86	0x56	-9.5	150	0x96	-4.6	214	0xD6	-1.6
23	0x17	-20.9	87	0x57	-9.4	151	0x97	-4.6	215	0xD7	-1.5
24	0x18	-20.6	88	0x58	-9.3	152	0x98	-4.5	216	0xD8	-1.5
25	0x19	-20.2	89	0x59	-9.2	153	0x99	-4.5	217	0xD9	-1.4
26	0x1A	-19.9	90	0x5A	-9.1	154	0x9A	-4.4	218	0xDA	-1.4
27	0x1B	-19.5	91	0x5B	-9.0	155	0x9B	-4.4	219	0xDB	-1.4
28	0x1C	-19.2	92	0x5C	-8.9	156	0x9C	-4.3	220	0xDC	-1.3
29	0x1D	-18.9	93	0x5D	-8.8	157	0x9D	-4.2	221	0xDD	-1.3
30	0x1E	-18.6	94	0x5E	-8.7	158	0x9E	-4.2	222	0xDE	-1.2
31	0x1F	-18.3	95	0x5F	-8.6	159	0x9F	-4.1	223	0xDF	-1.2
32	0x20	-18.1	96	0x60	-8.5	160	0xA0	-4.1	224	0xE0	-1.2
33	0x21	-17.8	97	0x61	-8.4	161	0xA1	-4.0	225	0xE1	-1.1
34	0x22	-17.5	98	0x62	-8.3	162	0xA2	-4.0	226	0xE2	-1.1
35	0x23	-17.3	99	0x63	-8.3	163	0xA3	-3.9	227	0xE3	-1.0
36	0x24	-17.0	100	0x64	-8.2	164	0xA4	-3.9	228	0xE4	-1.0
37	0x25	-16.8	101	0x65	-8.1	165	0xA5	-3.8	229	0xE5	-1.0
38	0x26	-16.6	102	0x66	-8.0	166	0xA6	-3.8	230	0xE6	-0.9
39	0x27	-16.3	103	0x67	-7.9	167	0xA7	-3.7	231	0xE7	-0.9
40	0x28	-16.1	104	0x68	-7.8	168	0xA8	-3.7	232	0xE8	-0.9
41	0x29	-15.9	105	0x69	-7.7	169	0xA9	-3.6	233	0xE9	-0.8
42	0x2A	-15.7	106	0x6A	-7.7	170	0xAA	-3.6	234	0xEA	-0.8
43	0x2B	-15.5	107	0x6B	-7.6	171	0xAB	-3.5	235	0xEB	-0.7
44	0x2C	-15.3	108	0x6C	-7.5	172	0xAC	-3.5	236	0xEC	-0.7
45	0x2D	-15.1	109	0x6D	-7.4	173	0xAD	-3.4	237	0xED	-0.7
46	0x2E	-14.9	110	0x6E	-7.3	174	0xAE	-3.4	238	0xEE	-0.6
47	0x2F	-14.7	111	0x6F	-7.3	175	0xAF	-3.3	239	0xEF	-0.6
48	0x30	-14.5	112	0x70	-7.2	176	0xB0	-3.3	240	0xF0	-0.6
49	0x31	-14.4	113	0x71	-7.1	177	0xB1	-3.2	241	0xF1	-0.5
50	0x32	-14.2	114	0x72	-7.0	178	0xB2	-3.2	242	0xF2	-0.5
51	0x33	-14.0	115	0x73	-7.0	179	0xB3	-3.1	243	0xF3	-0.5
52	0x34	-13.8	116	0x74	-6.9	180	0xB4	-3.1	244	0xF4	-0.4
53	0x35	-13.7	117	0x75	-6.8	181	0xB5	-3.0	245	0xF5	-0.4
54	0x36	-13.5	118	0x76	-6.7	182	0xB6	-3.0	246	0xF6	-0.3
55	0x37	-13.4	119	0x77	-6.7	183	0xB7	-2.9	247	0xF7	-0.3
56	0x38	-13.2	120	0x78	-6.6	184	0xB8	-2.9	248	0xF8	-0.3
57	0x39	-13.0	121	0x79	-6.5	185	0xB9	-2.8	249	0xF9	-0.2
58	0x3A	-12.9	122	0x7A	-6.4	186	0xBA	-2.8	250	0xFA	-0.2
59	0x3B	-12.7	123	0x7B	-6.4	187	0xBB	-2.7	251	0xFB	-0.2
60	0x3C	-12.6	124	0x7C	-6.3	188	0xBC	-2.7	252	0xFC	-0.1
61	0x3D	-12.5	125	0x7D	-6.2	189	0xBD	-2.6	253	0xFD	-0.1
62	0x3E	-12.3	126	0x7E	-6.2	190	0xBE	-2.6	254	0xFE	-0.1
63	0x3F	-12.2	127	0x7F	-6.1	191	0xBF	-2.5	255	0xFF	0.0

※ Output 8bit value : (-dB * 2), n dB = output 8bit *0.5

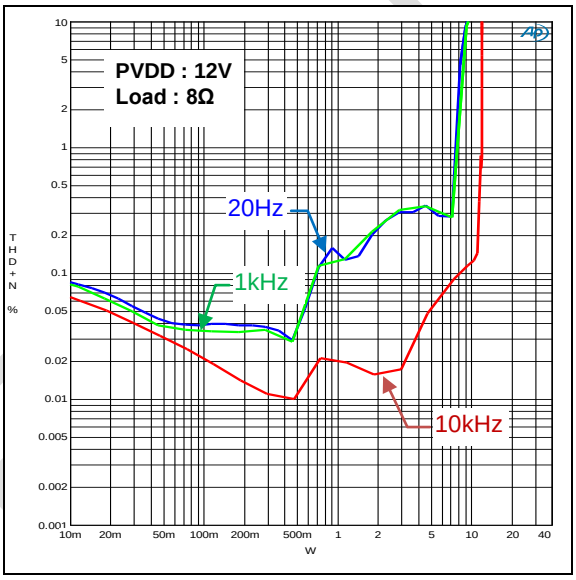
C. Typical Characteristics Graph

Total Harmonic Distortion + Noise vs. Power, BTL Configuration, 8Ω

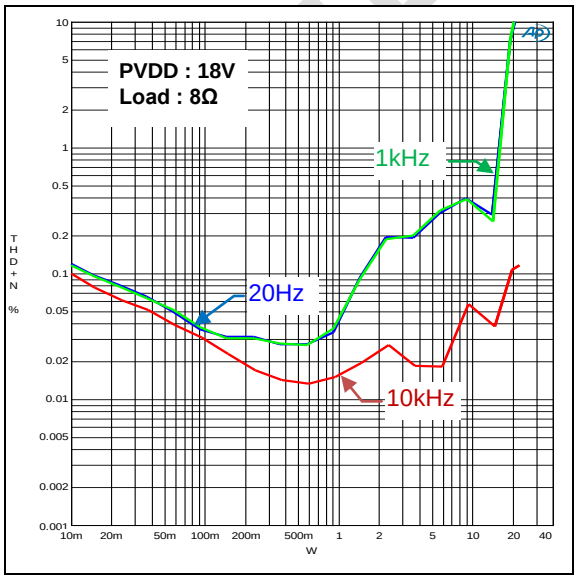
THD+N vs. Power



THD+N vs. Power

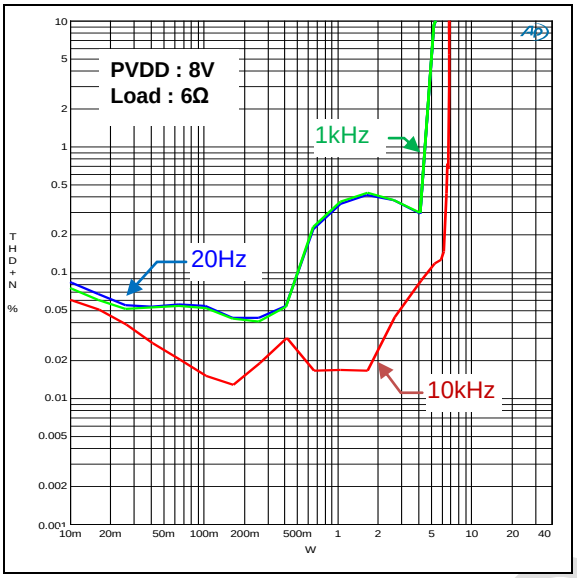


THD+N vs. Power

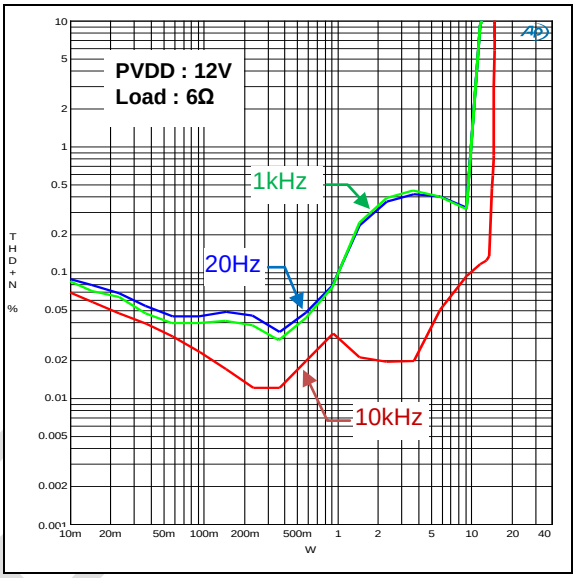


Total Harmonic Distortion + Noise vs. Power, BTL Configuration, 6Ω

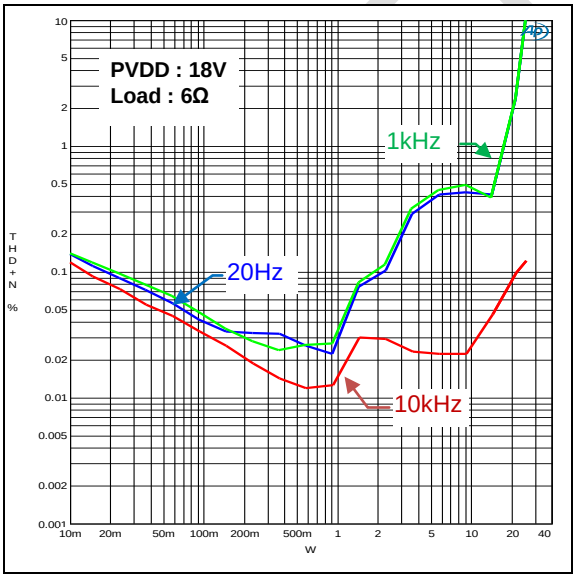
THD+N vs. Power



THD+N vs. Power

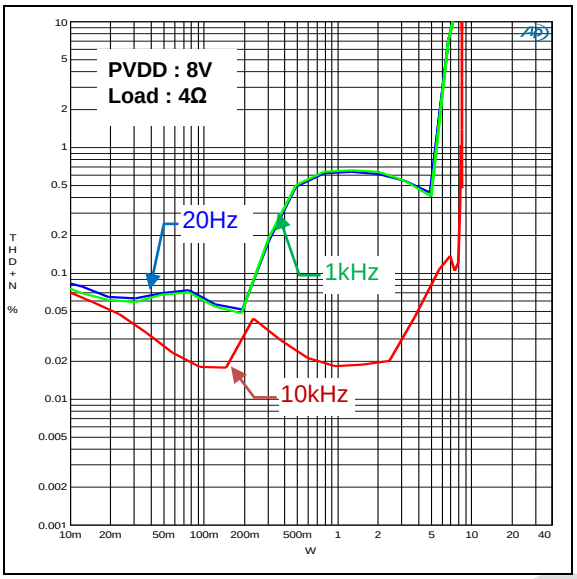


THD+N vs. Power

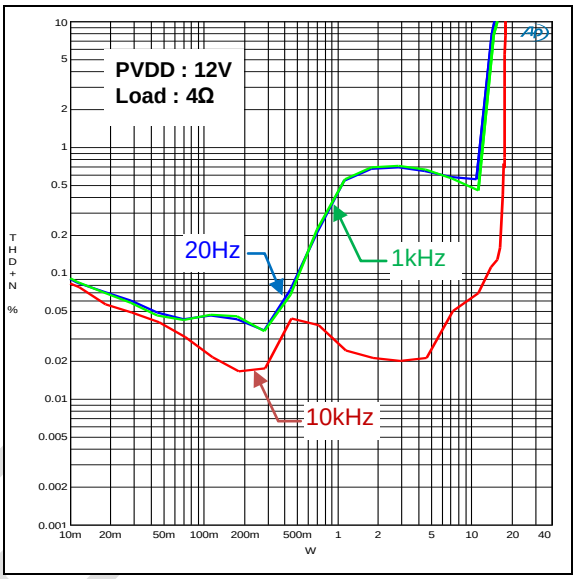


Total Harmonic Distortion + Noise vs. Power, BTL Configuration, 4Ω

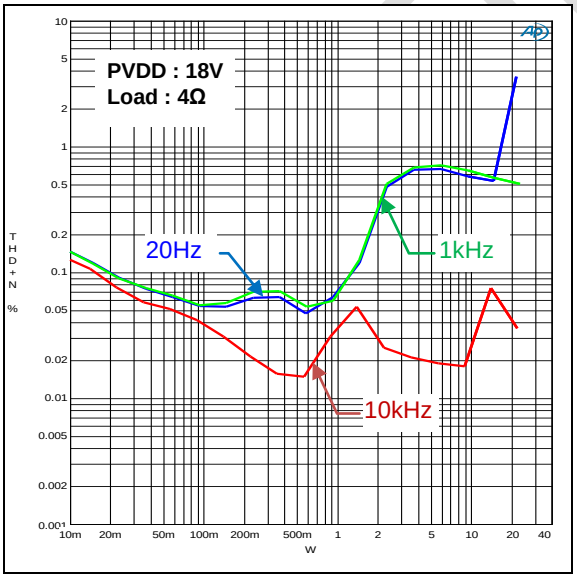
THD+N vs. Power



THD+N vs. Power

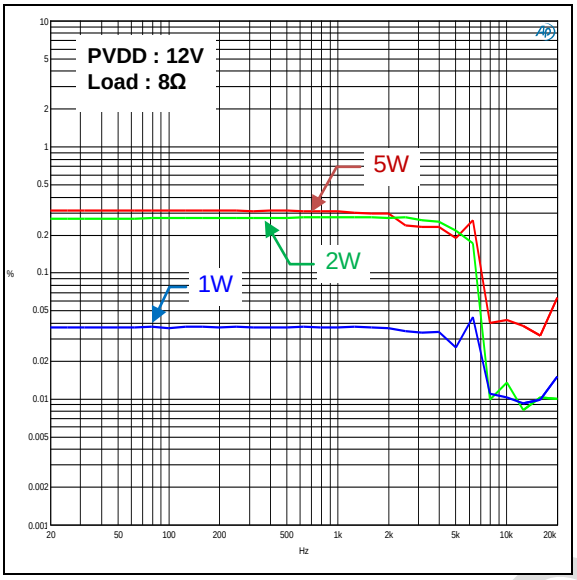


THD+N vs. Power

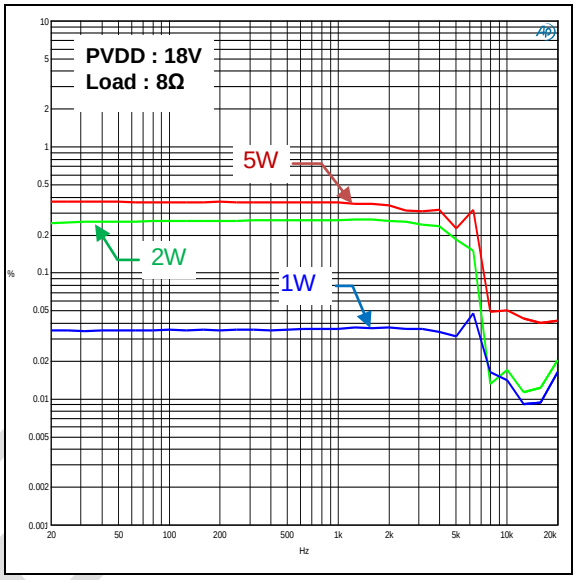


Total Harmonic Distortion + Noise vs. Frequency, BTL Configuration

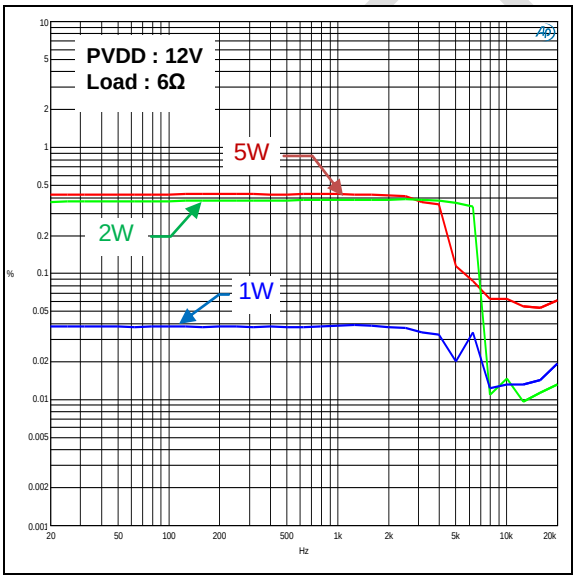
THD+N vs. Frequency



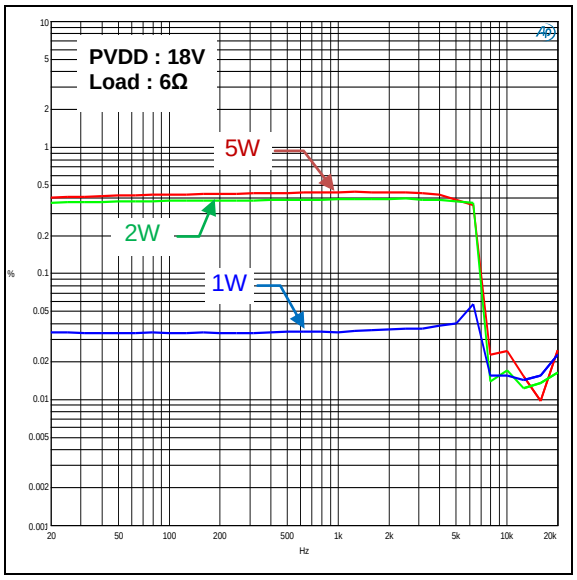
THD+N vs. Frequency



THD+N vs. Frequency

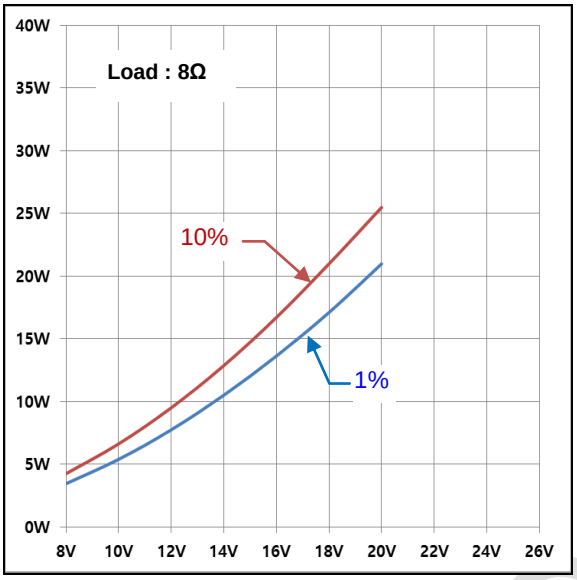


THD+N vs. Frequency

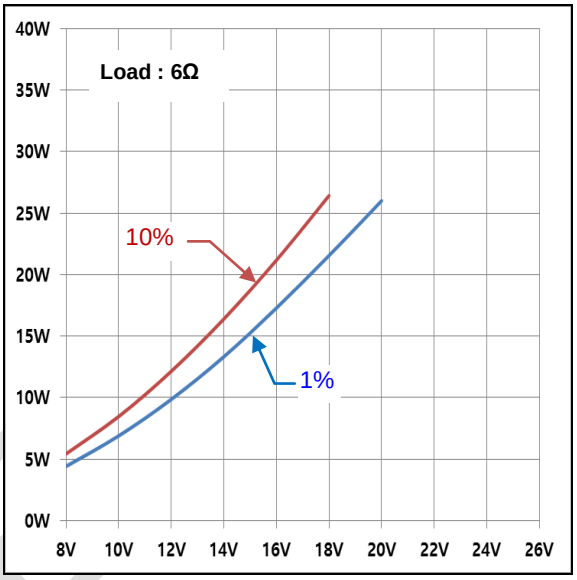


Output Power vs. PVDD, BTL Configuration

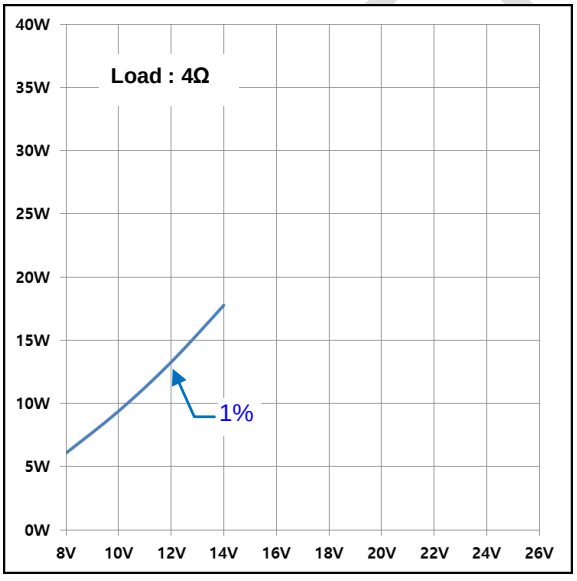
Output Power vs. PVDD



Output Power vs. PVDD

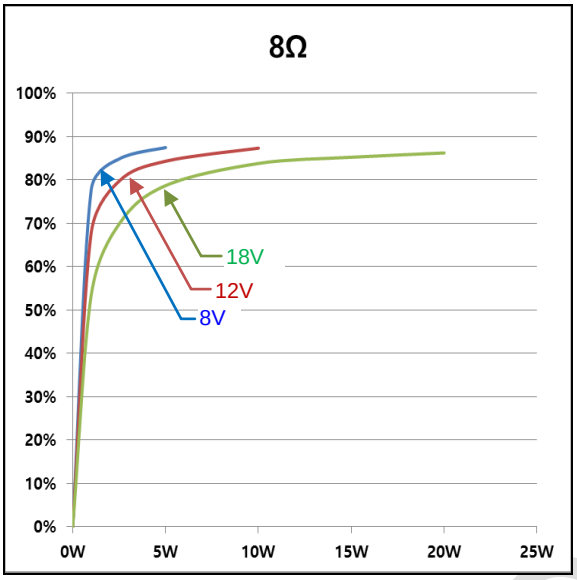


Output Power vs. PVDD

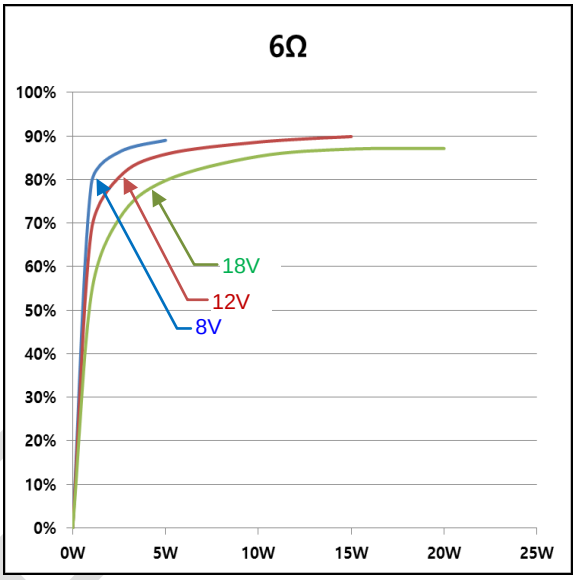


Efficiency vs. Total Power, BTL Configuration

Efficiency vs. Output Power

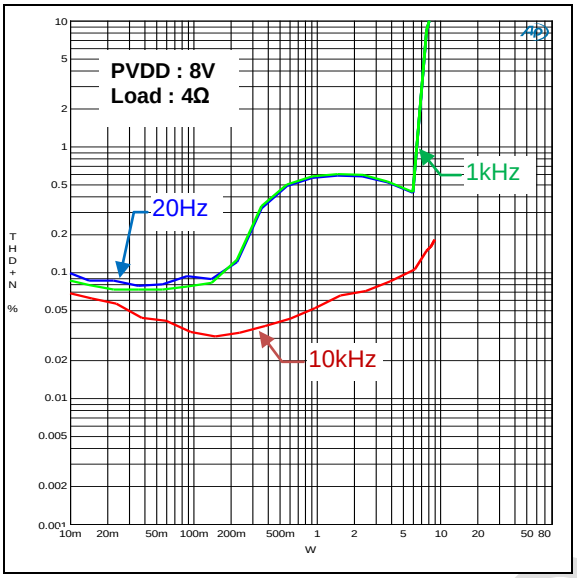


Efficiency vs. Output Power

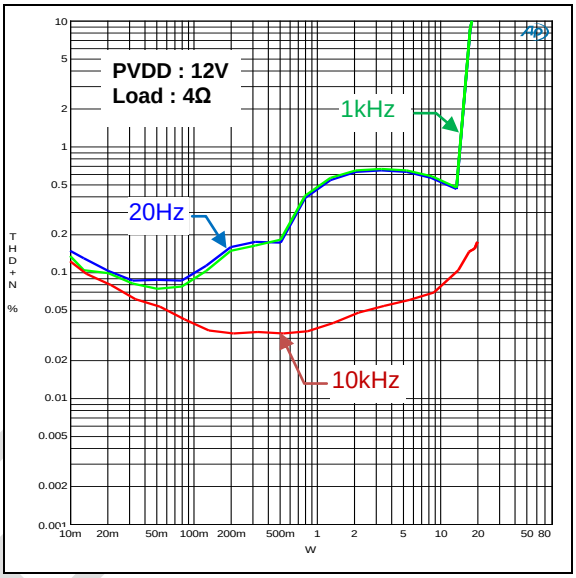


Total Harmonic Distortion + Noise vs. Power, PBTL Configuration, 4Ω

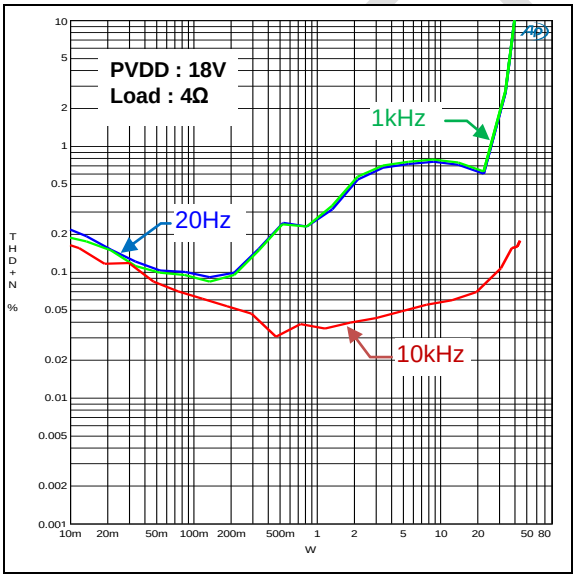
THD+N vs. Power



THD+N vs. Power

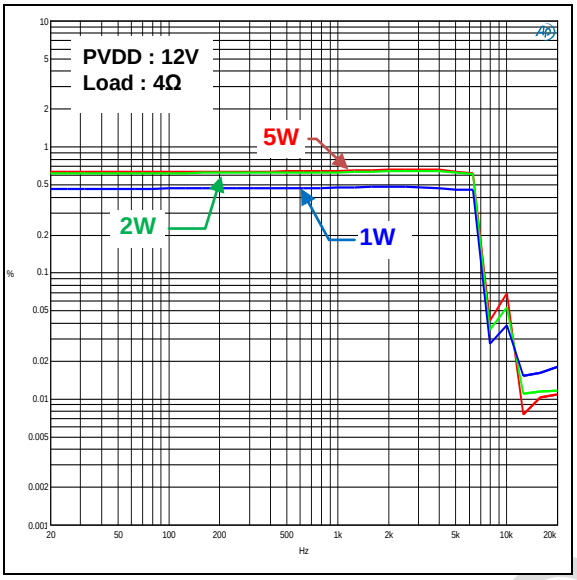


THD+N vs. Power

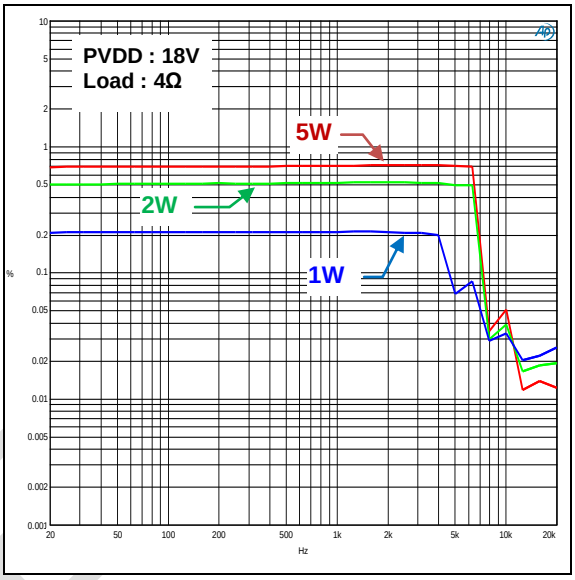


Total Harmonic Distortion + Noise vs. Frequency, PBTL Configuration, 4Ω

THD+N vs. Frequency

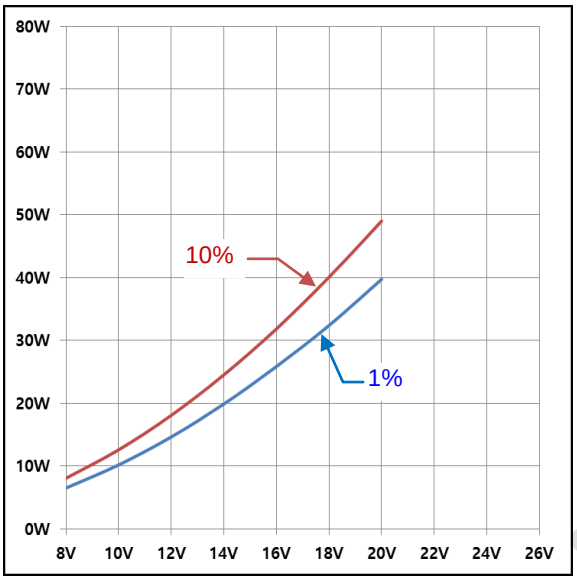


THD+N vs. Frequency



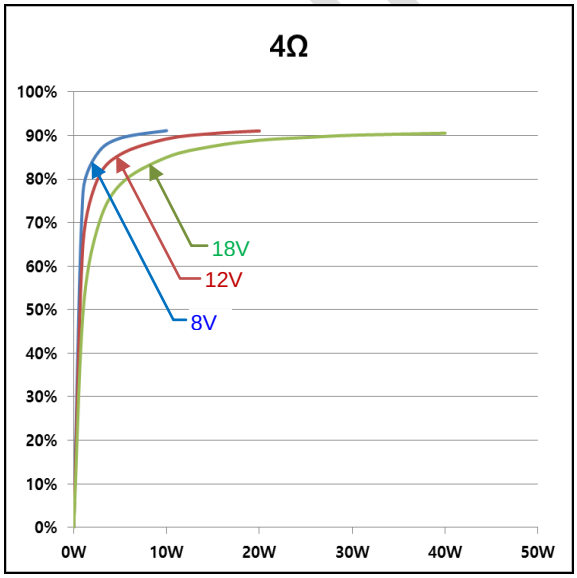
Output Power vs. PVDD, PBTL Configuration

Output Power vs. PVDD

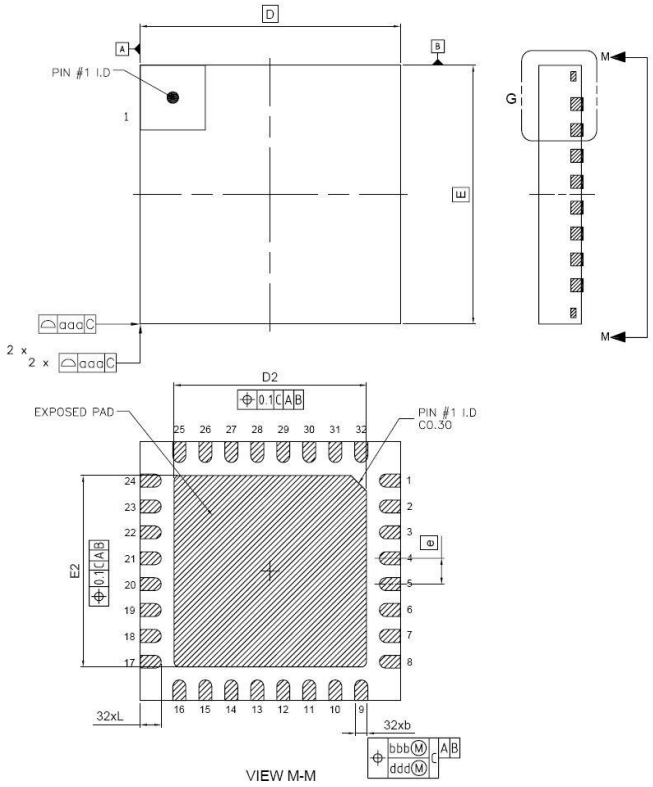


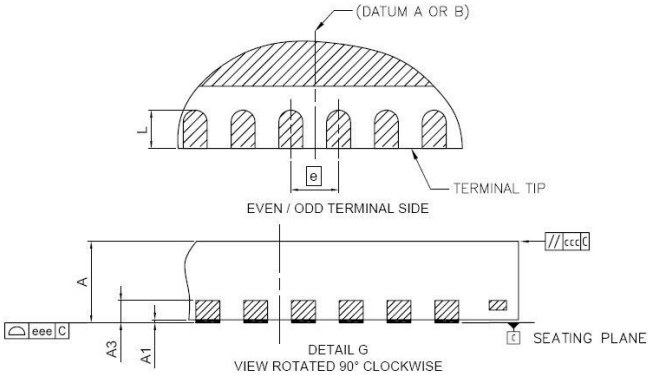
Efficiency vs. Total Power, PBTL Configuration

Efficiency vs. Output Power



D. Outline and Mechanical Data





DIM	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00		0.05
A3		0.203 REF	
b	0.20	0.25	0.30
D		5.00 BSC	
E		5.00 BSC	
D2	3.60	3.70	3.80
E2	3.60	3.70	3.80
e		0.50 BSC	
L	0.35	0.40	0.45
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

NOTES

1.0 DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.

2.0 ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

3.0 DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP. DIMENSION L1 REPRESENTS TERMINAL FULL BACK FROM PACKAGE EDGE UP TO 0.1mm IS ACCEPTABLE.

4.0 COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.

UNIT	DIMENSION AND TOLERANCE	REFERENCE DOCUMENT
Millimeter(mm)	ASME Y14.5M	JEDEC MO-220