NTP8212G

High Performance, High Fidelity Power Driver Integrated Full Digital Audio Amplifier

Datasheet
Preliminary ver. 0.8

NEOFIDELITY, INC.

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General Description

The NTP8212G is a single chip full digital audio amplifier including power stage for stereo amplifier system. NTP8212G is integrated with versatile digital audio signal processing functions, high-performance, high-fidelity fully digital PWM modulator and two high-power full-bridge MOSFET power stages.

The NTP8212G receives digital serial audio data with sampling frequency from 8kHz through 192kHz. It delivers 2 x 20 watts in stereo mode.

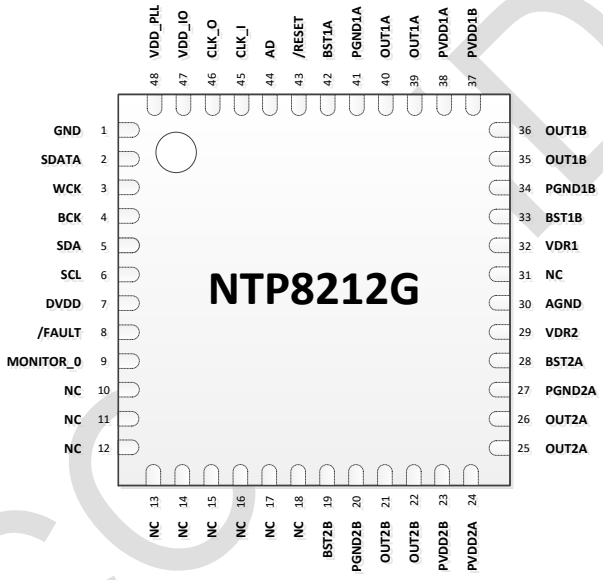
The NTP8212G has a mixer and Bi-Quad filters which can be used to implement the essential audio signal processing functions like loudness control, compensation of a loud speaker response and parametric equalization.

All the functions of the NTP8212G can be controlled by internal register values via I^2C host interface bus.

Features

- 2 CH Stereo (20W x 2 @24V, 8Ω)
- Wide Operating Supply Voltage Range (4.5V to 28V)
- Floating Point Operation
- 20 Programmable Bi-Quad Filters
  - ✓ Speaker Compensation
  - ✓ LPF, HPF
  - ✓ Parametric Equalizer
  - ✓ Loudness Control
- 100dB Dynamic Range
- 2 Band Dynamic Range Control
- 5 Band Graphic Equalizer
  - ✓ 10 PEQ in User Mode for LR
- 3D Surround
- Protection Circuit
  - ✓ OCP(Over Current Protection)
  - ✓ OTP(Over Temperature Protection)
  - ✓ UVP(Under Voltage Protection)
- Asynchronous Sample Rate Conversion
- High Efficiency
- DC cut filter

Package



(48 pin SAW QFN 7mm x 7mm Package)

Applications

- PDP TV or LCD TV
- Docking Station
- Mini-Component Audio Solution

Ordering Information

Product ID	Package Type	Pin	Size
NTP8212G	SAW QFN	48	7 x 7mm

NeoFidelity, Inc. 9F, Silicon Park A, 35, Pangyo-ro 255beon-gil, Bundang-gu, Seongnam-si, Gyeonggi-do, 463-400, Korea
Phone +82-31-8038-4810, Fax +82-31-8038-4885, Email info@neofidelity.com, Web www.neofidelity.com

Table of Contents

1. BLOCK DIAGRAM

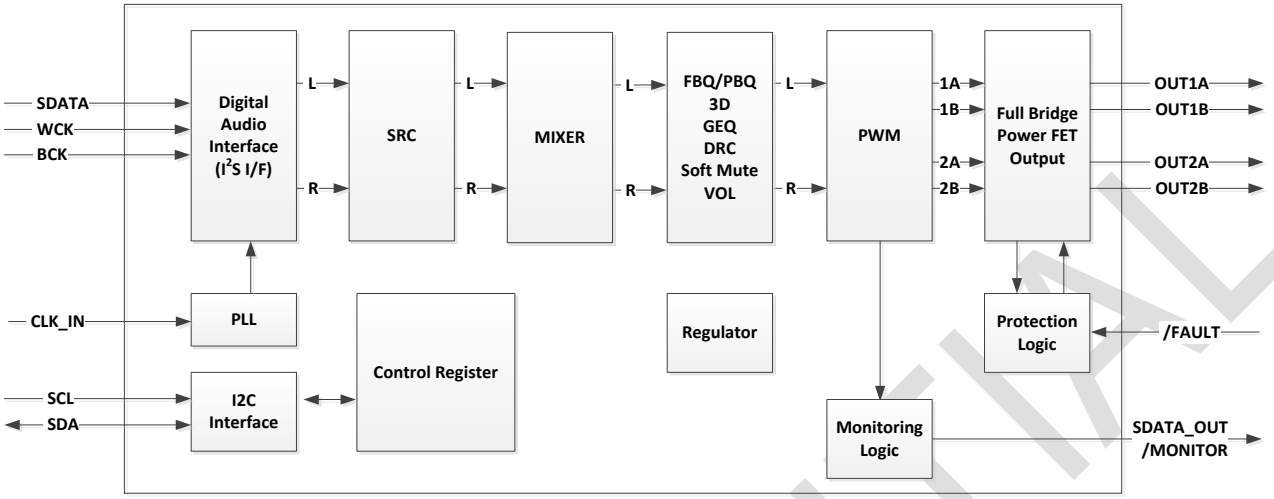


Figure 1. NTP8212G Block Diagram

2. PIN ASSIGNMENTS

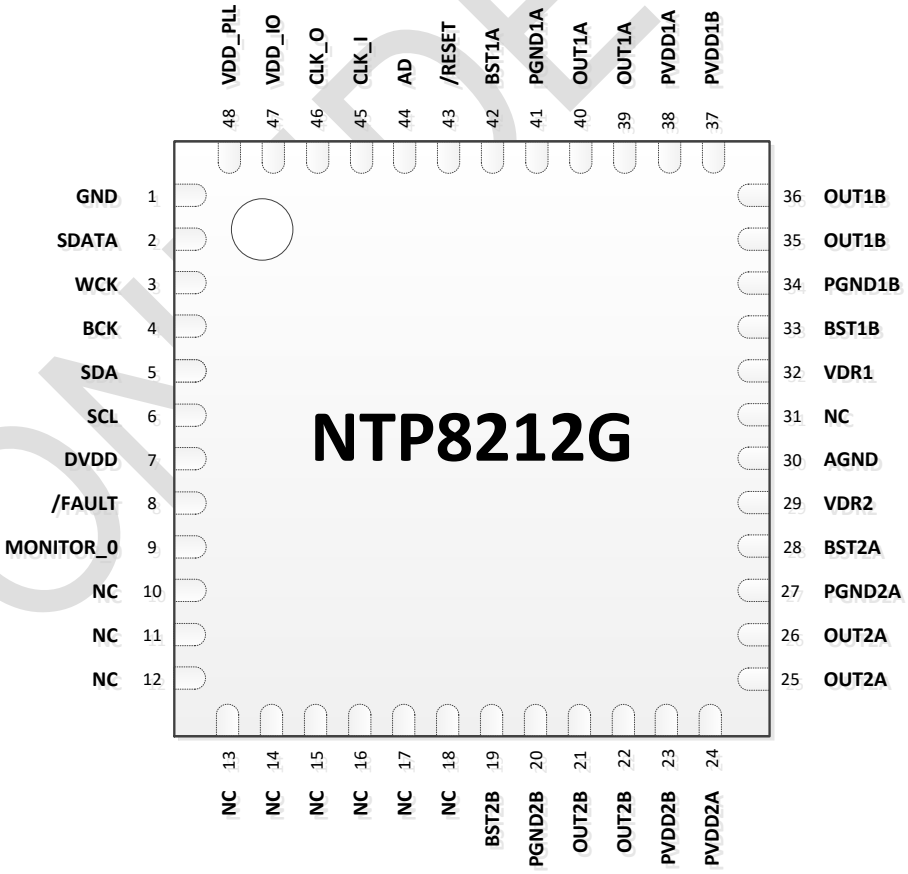


Figure 2. NTP8212G Pin Assignments

3. PIN DESCRIPTIONS

PIN	NAME	TYPE	DESCRIPTION
1	GND	P	This pin should be connected to Ground
2	SDATA	I	I^2S serial data input
3	WCK	I/O	I^2S word clock
4	BCK	I/O	I^2S bit clock
5	SDA	I/O	I^2C data
6	SCL	I	I^2C clock
7	DVDD	P	Regulator output for Core block, 1.2V
8	/FAULT	I	Input from external power device
9	MONITOR_0	O	Monitoring signal (SDATA word) / I^2S slave addr2 <refer to 5.3>
10	NC	-	Not Connected
11	NC	-	Not Connected
12	NC	-	Not Connected
13	NC	-	Not Connected
14	NC	-	Not Connected
15	NC	-	Not Connected
16	NC	-	Not Connected
17	NC	-	Not Connected
18	NC	-	Not Connected
19	BST2B	P	Bootstrap supply, external capacitor to OUT2B is required
20	PGND2B	P	Ground
21	OUT2B	O	Power stage PWM output 2B
22	OUT2B	O	Power stage PWM output 2B
23	PVDD2B	P	Power supply for PWM Power stage 2A, 2B
24	PVDD2A	P	Power supply for PWM Power stage 2A, 2B
25	OUT2A	O	Power stage PWM output 2A
26	OUT2A	O	Power stage PWM output 2A
27	PGND2A	P	Ground
28	BST2A	P	Bootstrap supply, external capacitor to OUT2A is required
29	VDR2	P	Gate drive voltage regulator decoupling pin, capacitor to GND is required
30	AGND	P	Ground
31	NC	-	Not Connected
32	VDR1	P	Gate drive voltage regulator decoupling pin, capacitor to GND is required
33	BST1B	P	Bootstrap supply, external capacitor to OUT1B is required
34	PGND1B	P	Ground
35	OUT1B	O	Power stage PWM output 1B
36	OUT1B	O	Power stage PWM output 1B
37	PVDD1B	P	Power supply for PWM Power stage 1A, 1B
38	PVDD1A	P	Power supply for PWM Power stage 1A, 1B
39	OUT1A	O	Power stage PWM output 1A
40	OUT1A	O	Power stage PWM output 1A
41	PGND1A	P	Ground
42	BST1A	P	Bootstrap supply, external capacitor to OUT1A is required
43	/RESET	I	Active low to reset, Schmitt trigger input
44	AD	I	I^2C Device address selection
45	CLK_I	I	System master clock, Schmitt trigger input
46	CLK_O	O	System master clock, Schmitt trigger output
47	VDD_IO	P	Power supply for digital interface I/O, 3.3V
48	VDD_PLL	P	Regulator output for PLL digital block, 1.2V
-	Thermal Pad	P	This pad should be connected to Ground

P = Power Supply or Ground, I = Input, O = Output, I/O = Input/Output

Table 1. NTP8212G Pin Description

4. CHARACTERISTICS AND SPECIFICATIONS

4.1. Absolute Maximum Ratings

Parameter	Reference	Rating	Unit
DVDD voltage	DGND	-0.3 ~ 1.5	V
VDD_IO voltage	GND_IO	-0.3 ~ 5.25	V
Logic input voltage	GND	-0.3 ~ 5.25	V
Logic output voltage	GND	-0.3 ~ 5.25	V
PVDDXX voltage	PGNDXX	30	V
OUTXX voltage	PGNDXX	-0.3 ~ PVDDXX	V
BSTXX voltage	PGNDXX	36	V
VDRX voltage	PGNDXX	6.0	V
Junction temperature	Tj	150	°C

4.2. Recommended Operating Conditions

Parameter	Reference	Min	Typ	Max	Unit
VDD_IO voltage	GND_IO	3.0	3.3	3.6	V
PVDDXX voltage	PGNDXX	4.5		28	V
VDRX voltage	PGNDXX	4.7	5.1	5.6	V
Ambient operating temperature	T_{AMB}	-10		85	°C

4.3. DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Logic Block (VDD_IO=3.3V, T_A=+25°C, unless otherwise specified.)						
Input High Voltage	V_{IH}	-	2.08			V
Input Low Voltage	V_{IL}	-	-0.3		0.89	V
Schmitt trig. Hysteresis	ΔV			0.29		V
Input current	I_I	V_{IN}=V_{IL} MAX, DVDD=MIN	-50			uA
		V_{IN}=V_{IH} MIN, DVDD=MIN			50	uA
Input leakage current	I_L	V_{IN}=VSS, DVDD=MIN	-10		10	uA
Output Low voltage	V_{OL}	I_{OL}=-4mA	0		0.4	V
Output High voltage	V_{OH}	I_{OH}=4mA	2.4		3.6	V
LDO output voltage	V_{LDO}	DVDD	1.08		1.32	V
Driver Block (PVDDXX=20V, T_A=+25°C, unless otherwise specified.)						
Current consumption	I_{CC}	VDD_IO=3.3V, No Input, No Load		27		mA
	I_{PVDD}	PVDD=18V, No Input, 6 Ω Load with 10uH inductor		30		
	I_{PVDD}	PVDD=24V, No Input, 8 Ω Load with 10uH		36		
	I_{PVDD}	PVDD=24V, Shutdown, 8 Ω Load with 10uH		0.2		uA
Peak current limit	OCP	-	5.0		8.0	A
Thermal shutdown temperature	OTP-			150		°C
Under voltage protection limit	UVP	-		3.9	4.15	V

4.4. Performance Specification

Speaker Amplifier					
Parameter	**Condition**	**Min**	**Typ**	**Max**	**Unit**
SNR	AES17, A-weighting filter		95		dB
THD+N	1W, 1kHz		0.1		%
Cross talk	PVDD=24V,Output Power=1W@ 8Ω		70		dB
Output noise voltage	No input		300		uV
Efficiency			90		%
PWM frequency			384		KHz

4.5. Switching Characteristics – I²C Control

Parameter	**Symbol**	**Condition**	**Min**		**Max**	**Unit**
I²C Control Port						
SCL clock frequency	F_{scl}		-		400	kHz
Hold time for START condition	T_{hdsta}		600		-	ns
Low period of the SCL clock	T_{low}		1300		-	ns
High period of the SCL clock	T_{high}		600		-	ns
Rise time of SDA and SCL signals	T_{rise}		-		300	ns
Fall time of SDA and SCL signals	T_{fall}		-		300	ns
Setup time for STOP condition	T_{susto}		600		-	ns

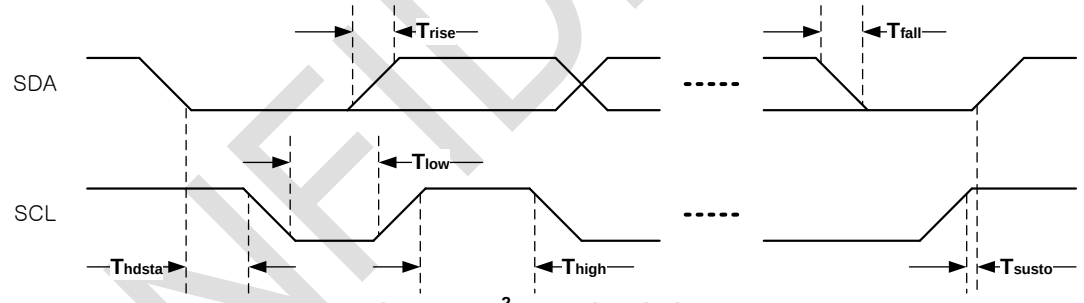


Figure 3. I²C Mode Timing

4.6. Switching Characteristics – Audio Interface

Parameters	**Symbol**	**Min**	**Max**	**Unit**
BCK high time	t_{bh}	20	-	ns
BCK low time	t_{bl}	20	-	ns
SDATA setup time before BCK rising edge	t_{ds}	10	-	ns
SDATA hold time after BCK rising edge	t_{dh}	10	-	ns
WCK setup time before BCK rising edge	t_{ws}	20	-	ns
BCK rising edge before WCK edge	t_{wh}	20	-	ns

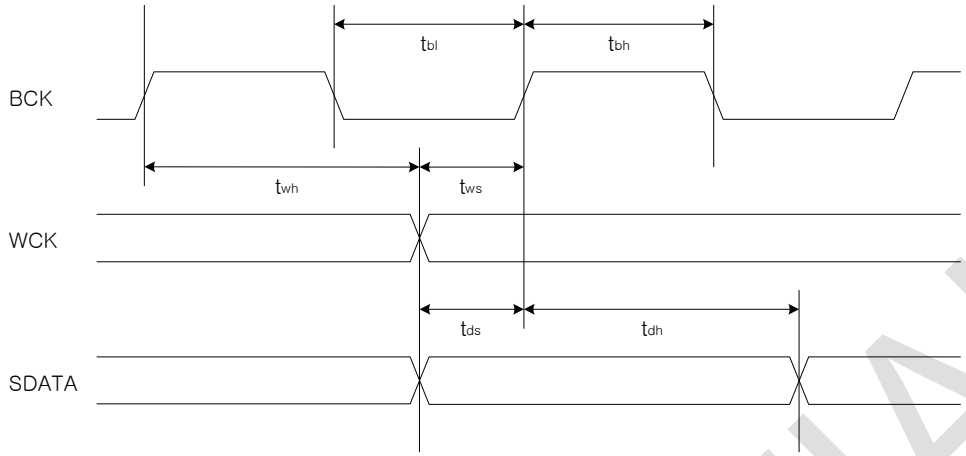


Figure 4. Audio Interface Timing

5. I²C BUS OF NTP8212G

The NTP8212G uses an industry standard Inter IC Control (I2C) bus to communicate with host IC. A host IC can write or read internal registers of the NTP8212G via the I2C bus.

5.1. General Description of I²C Bus

The I²C bus uses two signal lines – a serial clock line (SCL) and a serial data line (SDA). Because the SDA line is open-drain type port, both the NTP8212G and a host IC can only drive these pins low or leave them open.

In I²C bus, a master device means the device which generates serial clock on the SCL. A slave device means the device which receives serial clock. There can be many master and slave devices on an I²C bus. But, when one master device works on the bus, the other master devices should not generate signal on the lines. These unexpected interrupts can make other slave devices to fail to communicate with the mater device.

The NTP8212G supports only slave mode of I²C bus. So, the NTP8212G always receives serial clock from a host IC. The slave mode is enough to write/read data to/from the NTP8212G.

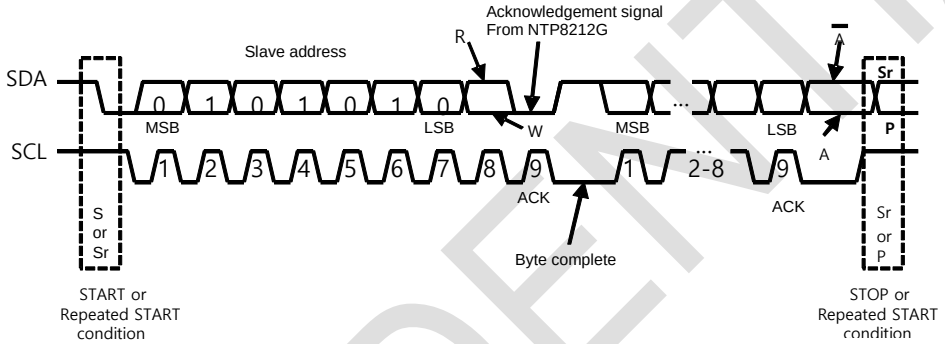


Figure 5. Basic Signaling Elements of I²C Bus

If there are no communication on I²C bus, lines must keep in high state. I²C bus begins communication with the start condition and ends communication with the stop condition. The start condition can be generated by changing the SDA state high to low, during the SCL state remains in high. The stop condition can be generated by changing the SDA state low to high during the SCL remains in high state. Be aware that the stop condition always reset the internal status of I²C bus control logic. Except these two conditions, the SDA may not change during the SCL in high state. Otherwise, abnormal start or stop condition will be generated.

I²C bus transfers the MSB of a byte on 1st data slot and the LSB of a byte on 8th data slot. I²C bus checks success or fail of transfer on every 1 byte transfer. The device which found an expected data on SDA must generate acknowledgement (keep low on SDA) on 9th clock. If there is no acknowledgement on 9th clock, the device which generated a data on SDA may stop transfer. The NTP8212G will generate acknowledgement for every successful data transfer of 1 byte in write mode. But, in read mode, because data is generated by the NTP8212G, the NTP8212G will not generate an acknowledgement. In this case, on the contrary, the NTP8212G will check SDA state on 9th clock that the master device received a read data properly.

Last 8th bit of the 1st byte is used to indicate whether the master device want to write or read data.

5.1.1. Writing Operation

When last 8th bit of the 1st byte is set to low state, the writing operation of bus begins. The NTP8212 supports 3 kind of writing operations which presented on **Figure 6.**

The type presented on **Figure 6-(a)** is single byte write operation. “Sub address” on 2nd byte means the internal register address of the NTP8212. The “Data” on 3rd byte will be written into the internal register address on “Sub address”. If stop condition is not generated, writing “data” on specific “sub address” can be repeated like **Figure 6-(b)**. “Data #n” will be written on “sub address #n”.

The type presented on **Figure 6-(c)** is burst byte write operation under address auto increment mode. The AIF is the address Auto Increment Flag which is 1st bit of 2nd byte of I²C packet. On SDA, if AIF is

set to high state, the NTP8212 starts auto incrementing the address with respect to given “sub address” and host send write data continuously over SDA. In AIF mode, access to the register addresses 0x3B~0x49, 0x4F and 0x5E are automatically skipped.

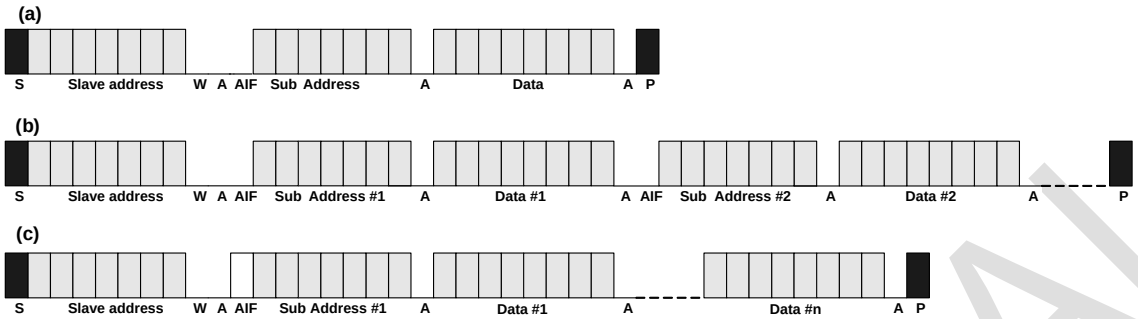


Figure 6. Single Byte Write Mode Sequence

Figure 7-(a), Figure 7-(b), and **Figure 7-(c)** represent 4 byte writing operations. Coefficient Mode Register address 0x00~0x6B are used to configure Bi-Quad filter coefficients, Low Shelf BQ filter coefficients, Loudness gains and DRC clip down gain. The data size of these coefficients and gains is 4 byte for each. The difference between 4byte writing operation and single byte writing operation is only the size of transferring data. So, after sending “Sub address”, 4 sequential bytes must be transferred from the MSB(most significant byte) to the LSB(least significant byte) sequence.
The type presented on **Figure 7-(c)** is quad byte write operation under address auto increment mode, AIF function. Please compare the data transfer size between **Figure 6** and **Figure 7.**

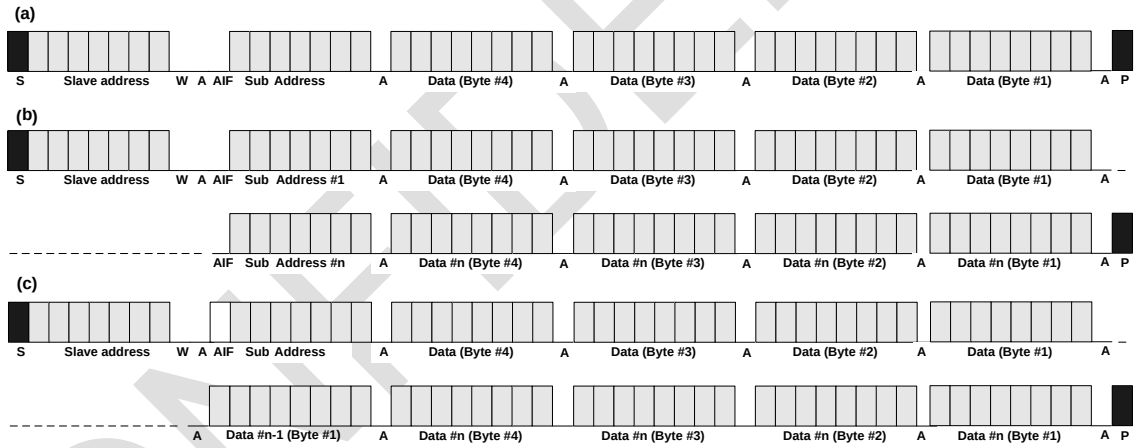


Figure 7. Quad Byte Write Mode Sequence

In write operation, the register 0x7E value needs to be set first for performing the configuration of the registers belong to all channels. The 0x7E register also support to configuring byte writes operation and word i.e. 4 byte writes operation.

If 0x7E register is configure to 0x00, it support byte write operation and for word i.e. 4 byte write operation for each channel it needs to configure as 0x01 for channel 1, 0x02 for channel 2 and 0x08 for PEQ coefficient. Also to configure channel1 and channel2 with the same values, the 0x7E register needs to configure as 0x03. So the same values get sets for both the channel with only one write operation.

The ROM BQ addresses from 0x00 to 0x09 and from 0x14 to 0x3B are used for the Bi-Quad filter coefficients in the coefficient mode. Each Bi-Quad filter uses 5 coefficients. Any unexpected coefficient value changes on any part of 5 coefficients can generate unstable Bi-Quad filter response. For example, if only one of 5 coefficients for a Bi-quad filter is changed and downloaded, its combined 5-coefficient set can have unstable operation while old and new coefficients are mixed together.

Therefore to prevent this kind of problem, the NTP8212G writes coefficients to coefficient registers only when the last 5th coefficients of each Bi-Quad filter are downloaded, which means all of 5 coefficients are fully ready. Please refer to 9.1 for more detailed operation.

5.1.2. Reading Operation

Figure 8-(a) represents single byte reading operation from the NTP8212G. To read data from the NTP8212G, generate start condition to start transfer. After then, send “slave address” with write mode flag and send the register address(sub address). By regenerating start condition (Sr) again and transferring “slave address” with read mode flag, reading operation begins. The NTP8212G will generate data on SDA signal synchronizing with serial clocks on the SCL. Because the SDA signal generated from the NTP8212G, the master device must generate ACK on 9th slot to confirm that the master received read 1 byte successfully. However, if this is just one byte reading operation, NAK (not acknowledged) signal must be generated. Then stop condition must be generated to end transfer.

When AIF set to high on sub address like **Figure 8-(b)**, data will be read continuously with register addresses which are increased from initial “sub address” for every byte. In continue reading operation, the master must generate ACK signal on every 9th bit of the packet to confirm that master has received 1 byte successfully. Otherwise, reading operation will be terminated.
At the end of AIF reading operation, the NAK should be generated on 9th bit of the last data read to stop the AIF continuous reading operation. Also in reading operation access to the register mention in the “Write Operation’ are skipped.

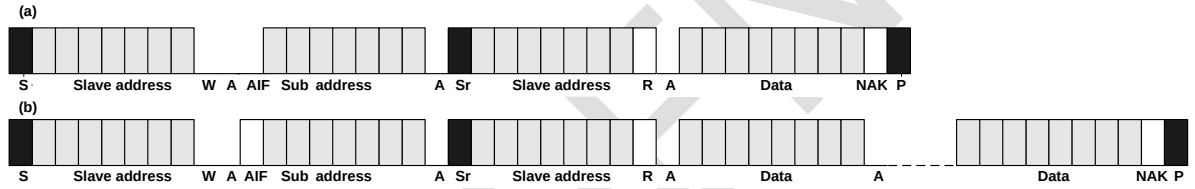


Figure 8. Single Byte Read Mode Sequence

Figure 9 represents quad byte reading operation. The difference between quad byte reading operation and single byte reading operation is only the size of receiving data. So, after sending “Sub address”, 4 sequential bytes must be received from the MSB to the LSB sequence.
The type presented on **Figure 9-(b)** is quad byte read operation under address auto increment mode, AIF function. Please compare the data receive size between **Figure 8** and **Figure 9.**

Before reading operation, the value of register 0x7E should be set first. In case single byte reading operation, set the register 0x7E to “0000”. In case 4 byte reading operation, set the register 0x7E to “0001” for channel1, “0010” for channel2 or “1000” for PEQ coefficient.

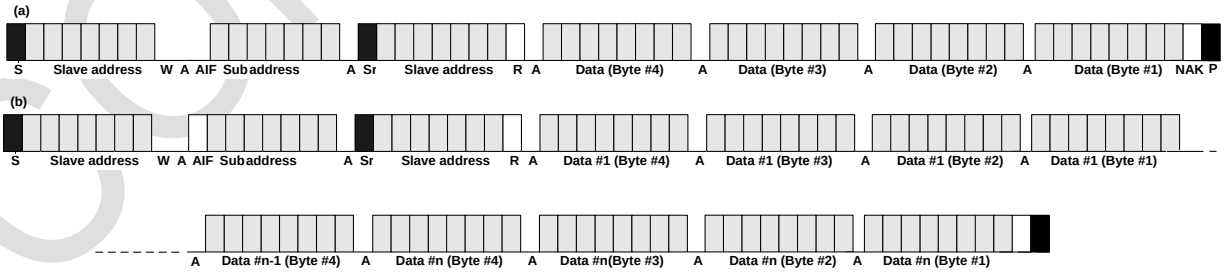


Figure 9. Quad Byte Read Mode Sequence

In read operation, the register 0x7E value needs to be set first for performing the configuration of the registers belong to all channels. The 0x7E register also support to configuring byte reads operation and word i.e. 4 byte reads operation.

If 0x7E register is configure to 0x00, it support byte read operation and for word i.e. 4 byte read operation for each channel it needs to configure as 0x01 for channel 1, 0x02 for channel 2 and 0x08 for PEQ. Also to configure channel1 and channel2 with the same values, the 0x7E register needs to configure as 0x03. So the same values get sets for both the channel with only one read operation.

5.2. I²C Glitch Filter

To clean out the threats of noise in today's high-speed-board system, the NTP8212G has a glitch elimination filter on the I²C ports. Glitches in the transmission lines of the I²C port can be safely removed with this function. Please refer to the register 0x39.

5.3. I²C Slave Address

The NTP8212G supports up to four slave address. So, four NTP8212G can be connected to the same MCU at the same time. For multi-chip operation, use the proper I2C slave address according to AD pin and the initial state of MONITOR_0 pin as shown in **Table 2**.

		MONITOR_0		
Pin name	Value	Pull-down ('L')	Pull-up ('H')	No pd / pu (default: 'L')
AD	0	Addr : 0x54	Addr : 0x58	Addr : 0x54
	1	Addr : 0x56	Addr : 0x5A	Addr : 0x56

Table 2. I²C Slave Address

6. CLOCK, RESET & CONTROL

6.1. System Clock

The internal system clock of the NTP8212G is generated from an external master clock by the on-chip PLL. The NTP8212G supports external master clock frequency from 2.048 MHz to 24.576MHz. For proper operation, the registers for the PLL should be set correctly according to master clock frequency (Address 0x02).

6.2. Timing Sequence

For proper power up, initialization and power down of NTP8212G, it is recommend to use the following sequence as shown in **Figure 10**.

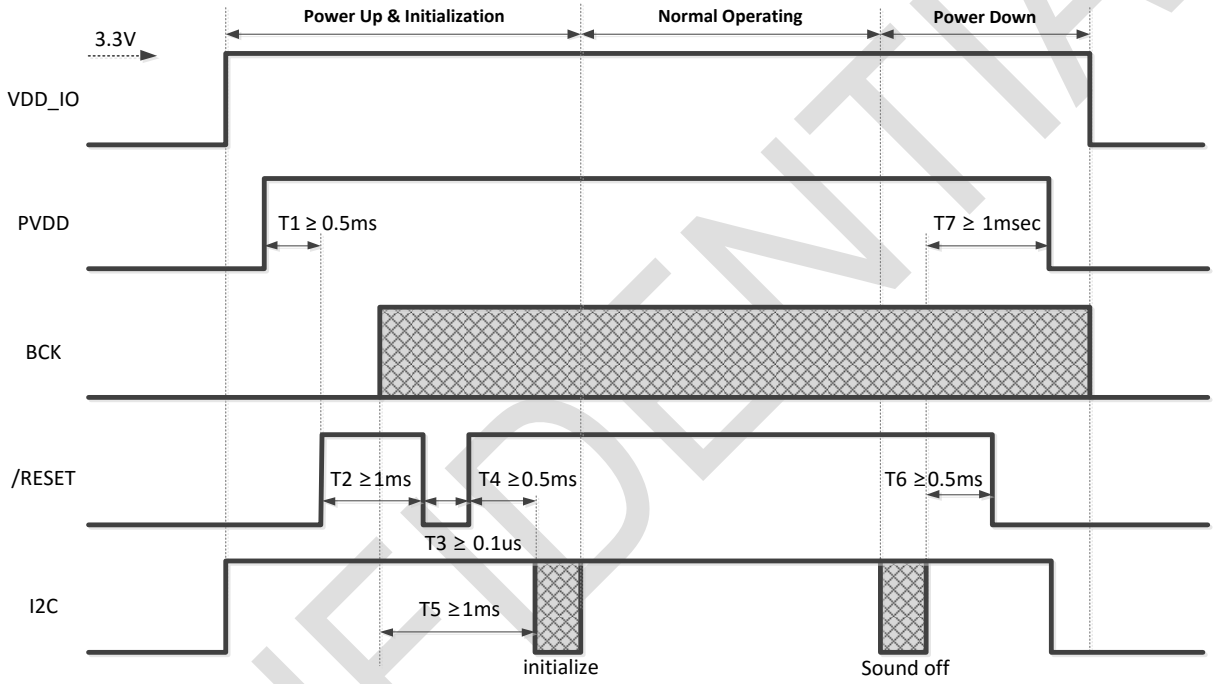


Figure 10. Recommended Timing Sequence

6.2.1. Power-Up & Initialization Sequence

1) Ramp up VDD_IO to at least 3.3V.
2) Ramp up PVDD.
3) After 0.5msec (T1≥0.5msec), drive /RESET = High, and then wait for at least 1msec (T2≥1msec).
4) Hold /RESET Low for at least 0.1usec (T3≥1usec)
5) Drive /RESET = High, and then wait for at least 0.5msec for I^2C communication (T4≥0.5msec).
6) BCK signal should arrive at least 1msec before I^2C initialization sequence (T5≥1msec).
7) Execute both amp initialization sequence (e.g. clock, volume, DRC, PEQ setup) and Sound on sequence.

6.2.2. Power-Down Sequence

1) When both DC and AC power are off, make sure to execute sound off sequence.
2) Switch /RESET to Low after sound off sequence (T6≥0.5msec).
3) BCK and I^2C should be Low after sound off sequence (T7≥0.5msec).
4) After I^2C is Low, ramp down VDD_IO.

6.3. Sound On/Off Sequence

For proper sound on/off of NTP8212G, use the following sequence as shown in **Figure 11**.

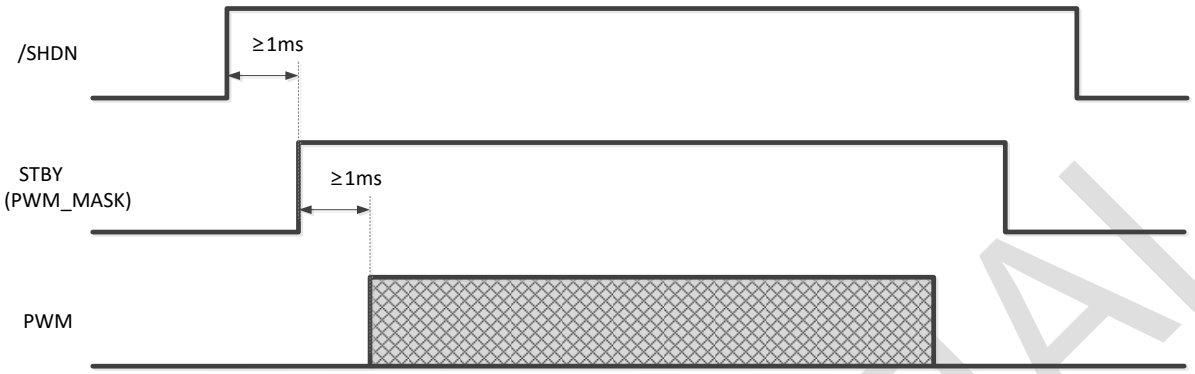


Figure 11. Sound On & Off Sequence

7. AUDIO INPUT

7.1. I²S and Serial Audio Interface

NTP8212G receives audio data through digital audio interface. There are 2 different formats generally used in digital audio interface - the Inter-IC Sound (I^2S) Interface and General Serial Audio Interface (GSA). These two interfaces have some common features.

These interfaces use 2 clock lines and 1 data line to transfer audio data. One of these clock lines is the WCK. A period of the WCK is same with sampling period of audio data. This property enables the clock receiving device to synchronize data word-wise transmitting or receiving timing with clock generating device. Another functional aspect of the WCK is indication of current channel. In I^2S mode, low state of the WCK indicates 1st channel or left channel, and high state of the WCK means 2nd channel or right channel.

The other clock line is BCK. This clock line is used to synchronize bit-wise timing. The number of clock for one WCK period can be selected on BCKS(Bit Clock Size Select) of register address 0x01.

NTP8212G functions as a slave on the bus. In slave mode, NTP8212G receives WCK and BCK from external source. The data transfer is done via SDATA line. The data being synchronized with the BCK must be loaded on this line. NTP8212G reads data on the rising edge of the BCK. NTP8212G reads data from defined bit range of WCK period. The bit range is selected by the interface type.

The bit range for I^2S is predefined. GSA interface can select a bit range with LRJ, MLF and BS of register address 0x01. Please refer to in **Figure 12.**

7.1.1. I²S Glitch Filter

To clean out the threats of noise in today's high-speed-board system, the NTP8212G has a glitch elimination filter on the I^2S ports. Glitches in the transmission lines of the I^2S port can be safely removed with this function. Please refer to the register 0x61.

7.2. SDATA Generator

The SDATA generator of NTP8212G sends out I2S out signal. In order for SDATA out process to function stably, the falling of BCK should either synchronize or occur ahead of falling or rising of WCK.

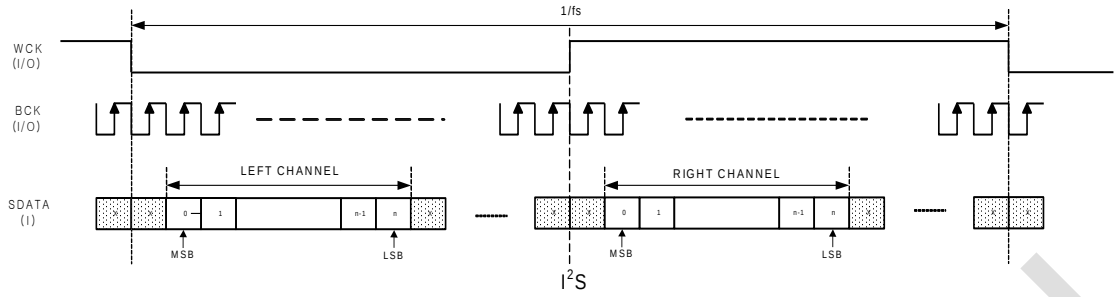
Refer to the register Address 0x5F in the **Appendix A** and refer to the **4.6. Switching Characteristics – Audio Interface**.

7.3. Asynchronous Sample Rate Conversion

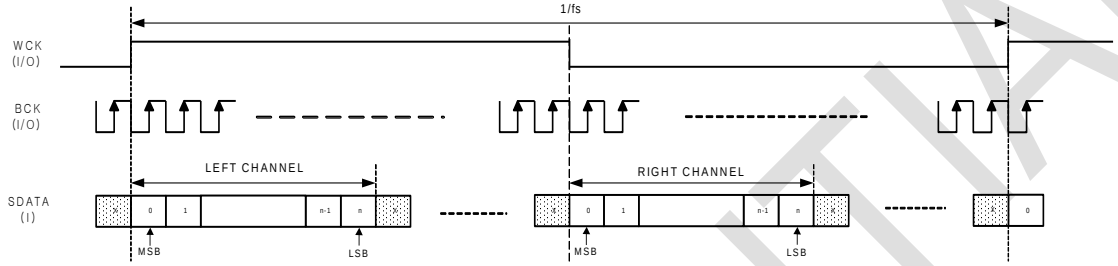
NTP8212G provides ASRC(Asynchronous Sample Rate Conversion) for input data sample rate from 8kHz to 192kHz.

ASRC can give seamless data continuity when clock sources of input I^2S and MCLK are different. Another benefit of ASRC is audio processing can be done without any change of register settings when there happens an alteration in the input sample rate.

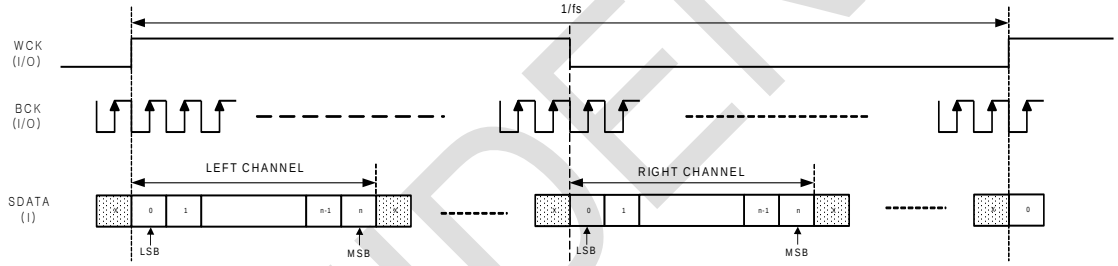
If ASRC is to be used, the LSB of 0x56 register, i.e. BYPASS, should be set as '0'. The default setting of BYPASS in the 0x56 register is '1', which means ASRC is disabled and synchronous conversion is applied.



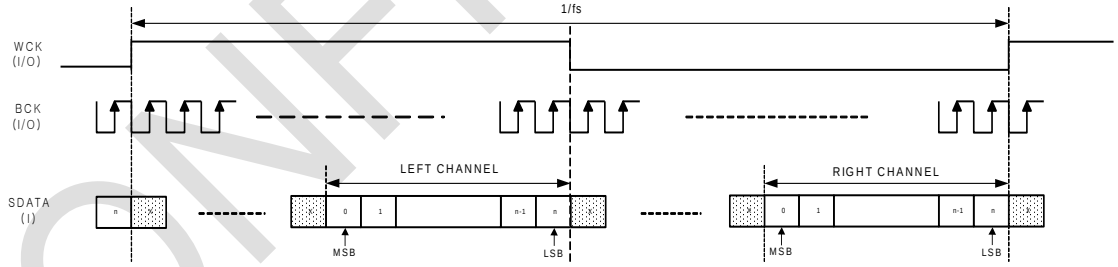
I^2S



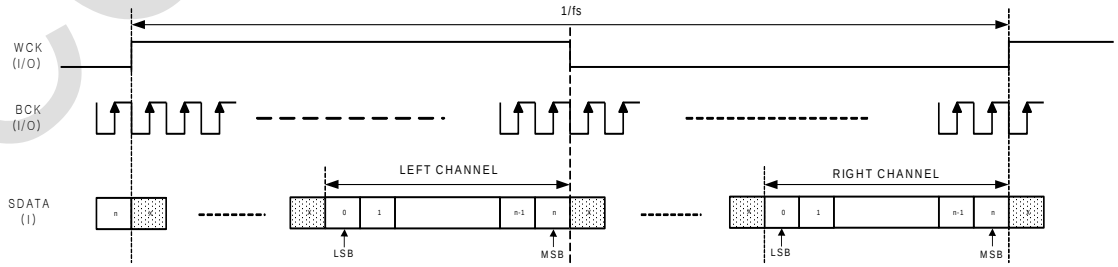
GSA, Left Justified, MSB first



GSA, Left Justified, LSB first



GSA, Right Justified, MSB first



GSA, Right Justified, LSB first

Figure 12. Serial Audio Interface Format

8. MIXER

Channel mixer can be used in lots of application needs like pseudo stereo and etc. User can mix input channels into each output channels with designated gains and polarity. Step size of mixer gain is variable according to the gain level as shown below.

Volume Range (dB)	Step (dB)
+18 ~ +6	1
+5.5 ~ -5.5	0.5
-6 ~ -32	1
≤ 32	-∞

Table 3. Variable Step Mixing Gain

In total, 4 mixing gain coefficients denoted as M[0x03], M[0x04], M[0x05], M[0x06] are defined as shown in the equation below. Each Mxx stores volume value in dB scale, and the number values versus gain in dB are shown in the **Appendix C**. There are some places in the mixing matrix that are considered as trivial connections and thus predefined as -∞ dB.

[Output Channels] = [Mixer Matrix] x [Input Channels]

$$\begin{bmatrix} \text{CH1 OUT} \\ \text{CH2 OUT} \end{bmatrix} = \begin{bmatrix} \text{M[0x03]} & \text{M[0x04]} \\ \text{M[0x05]} & \text{M[0x06]} \end{bmatrix} \cdot \begin{bmatrix} \text{CH1 IN} \\ \text{CH2 IN} \end{bmatrix}$$

Figure 13. Mixer Matrix

In order to load mixer coefficients into internal memory, send the index value in the gain value table to the register address 0x03~ 0x06.

9. PRE-PROCESSING

9.1. Pre Bi-Quad Filter Chain

NTP8212G has two kinds of Bi-Quad filter chains. One is Pre Bi-Quad filter chain and the other is Post Bi-Quad filter chain for bass management, loudness control, loud-speaker EQ, etc.
The former is called pre Bi-Quad filter chain and two 2nd order floating point Bi-Quad filters are connected serially to all the three channels. The structure is shown in **Figure 14**.

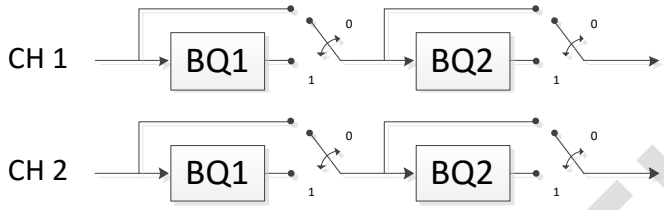


Figure 14. Pre Bi-Quad Filter Structure

Filter coefficients are 32-bit floating point numbers and can be downloaded thru I^2C interface. To download the pre Bi-Quad filter coefficients to internal memory of NTP8212G, designer should change the flags of register Address 0x7E to 'enable coefficient write' status.
When CH1(or CH2) Flag of register Address 0x7E is set to 1, coefficient mode register address 0x00~0x04 designates coefficients of 1st pre Bi-Quad filter chain of channel 1(or channel 2) and indicates b0, b1, b2, a1, a2 respectively. coefficient mode register address 0x05~0x09 designates the coefficients of 2nd chain of channel 1(channel 2).
The Bi-Quad filter structure is shown in **Figure 15**.

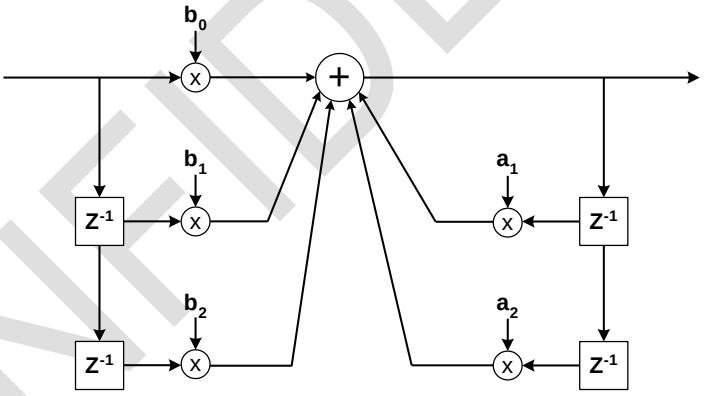


Figure 15. Bi-Quad Filter Structure

9.2. 3D Surround

3D surround expands the sound field of two channel stereo to the extent that is wider than the actual speaker spacing. Because this feature is acoustically valid for two channel signal, no other channels except channel 1/2 have this internal block.
NTP8212G realizes the 3D effect by combining delay and band-pass filter. At first, define the size of delay by using register Address 0x0D. Possible maximum delay is 40 samples delay and this is about 0.4msec based on 96kHz signal input.
And then download the band-pass filter coefficients to internal memory of NTP8212G (same with the Bi-Quad filter coefficient download procedure). The BPF is two 2nd order IIR filter. Each channel can have different BPF. Change the 3D flag status of register Address 0x7E to 'enable coefficient write' status and write the actual coefficient values to ten register Addresses 0x0A~ 0x13. Also, internal 2x2 mixer helps ease of design. For using 3D mixer, download the gain values to two coefficient mode register addresses 0x3C~0x3D.

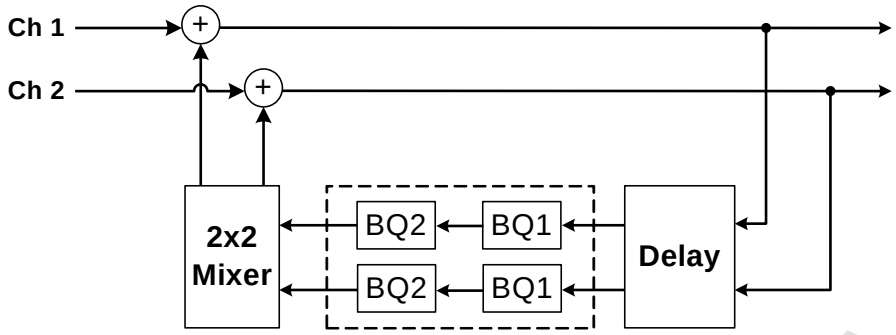


Figure 16. 3D Surround Structure

9.3. Configurable Graphic Equalizer

NTP8212G provides 5 band graphic equalizer and PEQ to 1/2 channel. EQ on/off can be selected by EQ flag of register Address 0x0F.
The gains for each band can be controlled by writing the gain values (refer Graphic equalizer band gain table in **Appendix C**) to register Addresses 0x10~14 respectively.
In PEQ the BQ1 ~ BQ5 can be used as programmable Bi-Quad filters.

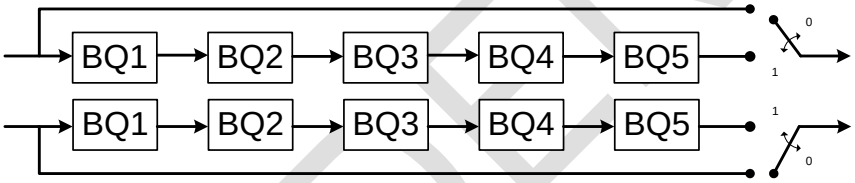


Figure 17. Configurable Graphic Equalizer

9.4. Post Bi-Quad Filter Chain

The post Bi-Quad filter chains of NTP8212G can be used in various purposes - bass management, loudness control, parametric EQ, loud-speaker EQ, etc. Independent filter design for 1, 2 channels are possible and five 2nd order floating point parametric filters are linked serially. Especially for loudness control, as shown in **Figure 18**, last 3 filters are different from first 2 filters.
Filter coefficients are 32-bit floating point numbers and can be downloaded thru I^2C interface. To download post Bi-Quad filter coefficients to NTP8212G, select download channel by using CH flag in register Address 0x7E first. And then write actual coefficient values, from 0x14 to 0x3B for Ch1&2 Control in the coefficient mode register address.
coefficient mode register address 0x14~0x18 designates 1st chain coefficients and means b0, b1, b2, a1, a2 in sequence. Address 0x19~0x1D designates 2nd chain, and so on. The enable/disable operation of these Bi-Quads can be made by using BQF flag in register Addresses 0x17~0x1A.
(refer register Address table in **Appendix A** and refer coefficient mode register address table in **Appendix B**)

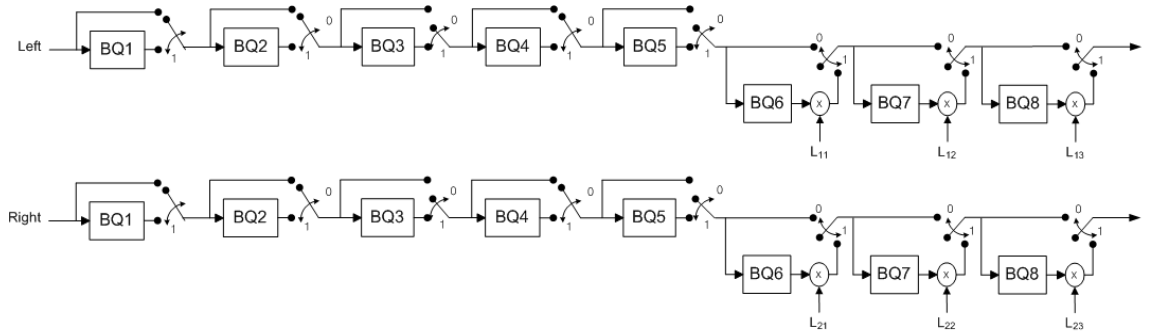


Figure 18. Post Bi-Quad Filter Structure

9.5. Loudness Control

NTP8212G provides loudness control function using post Bi-Quad filter chains. Loudness control means the compensation of frequency characteristics in low volume level to fit the acoustic characteristics of human ears

There are 3 Bi-Quad filters for loudness gain per each channel. To download a loudness gain of each Bi-Quad, the page flag register 0x7E should be set as same in the case of downloading the filter coefficients. The loudness gain values are applied for both channel 1 and 2 and when downloading the loudness gain values, a user should set the register 0x7E as 0x03.

loudness gains of CH1/CH2	Coefficient mode register Address		
	0x3E	0x3F	0x40
register Address 0x7E= 0x03 case	L1	L2	L3

Table 4. Address for Loudness Gain

10. VOLUME & DYNAMIC RANGE CONTROL

Master and channel volumes of the NTP8212G are independently controlled and softly changed. The system register address 0x2E is the master volume control that affects 2 channels simultaneously and the address 0x2F and 0x30 correspond to the channel volume control register for channel 1 and 2 respectively.
The possible Maximum Gain is +48.375dB with using master volume fine control, master volume and channel volume because the master volume applies the gain to an input signal independent from a channel volume. However, in such a case, a clipping might occur to prevent a signal overflow error if the magnitude of the input signal is large enough to exceed 0dB under the combined volume setting.

10.1. Master Volume Control

By setting volume control register (address 0x2E), master volume is controlled from negative infinity through 24dB with selectable step size as follows. For details on the master volume setting, see the register value table shown in **Appendix C**.

Step	Range
0.5 dB	+24 ~ -100 dB
10 dB	-100 ~ -150 dB

Table 5. Level Dependent Master Volume Steps

10.2. Channel Volume Control

By setting volume control registers (address 0x2F~0x30), channel volumes are independently controlled from negative infinity through +24dB with two selectable step sizes as described below, and in the **Appendix C**, exact values for channel volume setting are described.

Step	Range
0.5 dB	+24 ~ -100 dB
10 dB	-100 ~ -150 dB

Table 6. Level Dependent Channel Volume Steps

10.3. Master Volume Fine Control

Fine control for master volume is possible (+0.0625dB step up to maximum +0.4375dB boost). Refer the system register Address 0x2D in the **Appendix A**.

10.4. Mute and Soft Volume Change

The NTP8212G enters mute state by setting soft mute flag of register Address 0x26. Soft mute is implemented so that the volume gradually increases or decreases when mute is turned off or on respectively. Also the soft mute speed and soft volume change speed rates are programmable. Designers can minimize the pop noise by controlling the soft mute speed and volume change intervals. Refer SMH flag of register Address 0x26 and SVI flag of register Address 0x32.

10.5. Auto Mute

The NTP8212G can mute the sound automatically when the level of input audio signal is lower than the register-controlled threshold value. The mute can be done PWM switching with 50 % duty ratio.
Auto mute is supported for internal channels 1~3 after 2x3 mixer block. Refer register Address 0x33 and 0x34.

10.6. Dynamic Range Control

Dynamic range control can be turned on or off with programmable compression threshold and attack/release rates. The threshold parameters of DRC can be controlled separately for channel 1/2. For detailed setting, please refer to the system register Addresses 0x1C~0x25 and refer to the coefficient mode register addresses in Table 7.

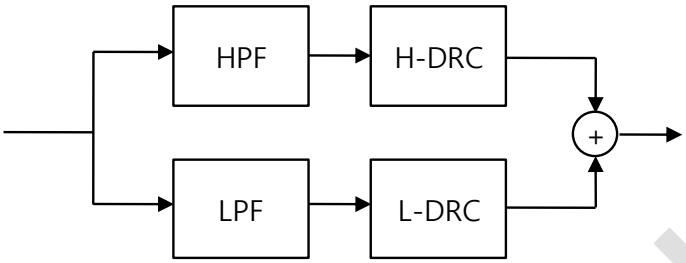


Figure 19. Block Diagram of Dynamic Range Control

2B' DRC Coefficient Mode Register Address	0x46 ~ 0x4A	0x4B ~ 0x4F	0x50 ~ 0x54	0x55 ~ 0x59	0x5A ~ 0x5E	0x5F ~ 0x63
When System Register Address 0x7E = 0x03	BQ1_Low	BQ2_Low	BQ3_High	BQ4_High	Attack Low	Attack High

2B' DRC System Address	0x1D	0x1F	0x1C	0x1E
When system address 0x7E = 0x00	Attack/ Release time control of L-DRC	Attack/ Release Time control of H-DRC	THD gain low	THD gain high

Table 7. DRC Coefficient Mode Register Map & System Register Map for Dynamic Range Control

11. OUTPUT INTERFACE

11.1. Output Configuration

The output mode of NTP8212G is 2.0 stereo reproduction mode. To produce proper output signal, register 0x35~0x37 should be set to appropriate values.

11.2. AM Interference Relief Mode

The NTP8212G has AM interference reduction mode. In this mode SNR performance of NTP8212G can be degrade down to 90 dB and the PWM switching frequency is spread from 384kHz through 768kHz.

11.3. Switching Output Mode

There are two selectable switching output modes in NTP8212G. The difference between two output modes lies in the relationship of the relative signal pattern between PWM OUTxA and PWM OUTxB for a channel x. The first one is called as AD mode. This AD mode can be applied to both half bridge and full bridge output stage.

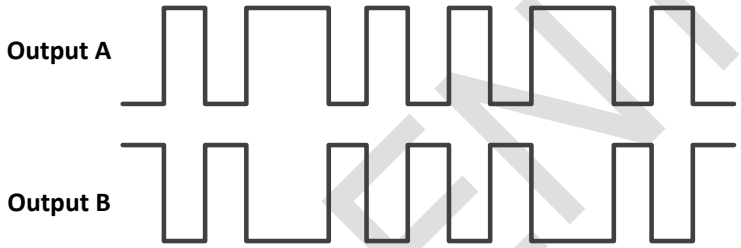


Figure 20. PWM Output Signals in AD Mode

AD asynchronous pair means the normal AD mode PWM output. In other words, An output and B output of each PWM output pair are mutually complementary. In the case of AD synchronous pair, An output and B output is perfectly identical, and its relation is not complementary. This is useful in some special case including single-ended power stage design.
The other one is called as NTX (Neo Trinity Amplification), which is D-BTL mode. This mode is applied only for BTL, and its operation is dynamically-biased BTL, compared to the normal BTL. An example of output signals in D-BTL mode is shown in **Figure 21.**

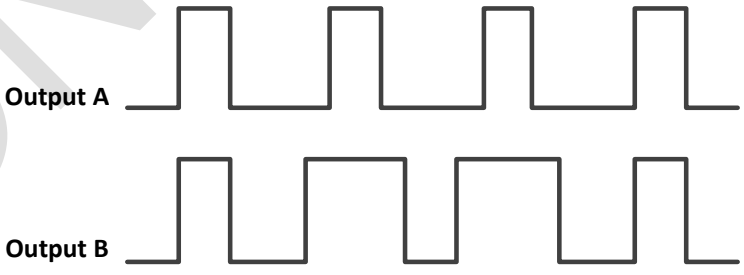


Figure 21. PWM Output Signals in D-BTL Mode

For D-BTL mode, there are two additional parameters, which is MLP (Minimum Linear Pulse Length). MLP defines the minimum pulse length that can guarantee a linear relationship between the input and output pulse length. Generally, the width of the output pulse is proportional to that of the input pulse. However, as the width of input pulse becomes narrower, such linear relation is not maintained due to the characteristic of a power device. The minimum MLP value is preferred as long as linear relationship between the input and the output pulse is satisfied. In addition, in terms of power consumption, a minimal MLP value is preferred.
This compensation is illustrated in **Figure 22**.

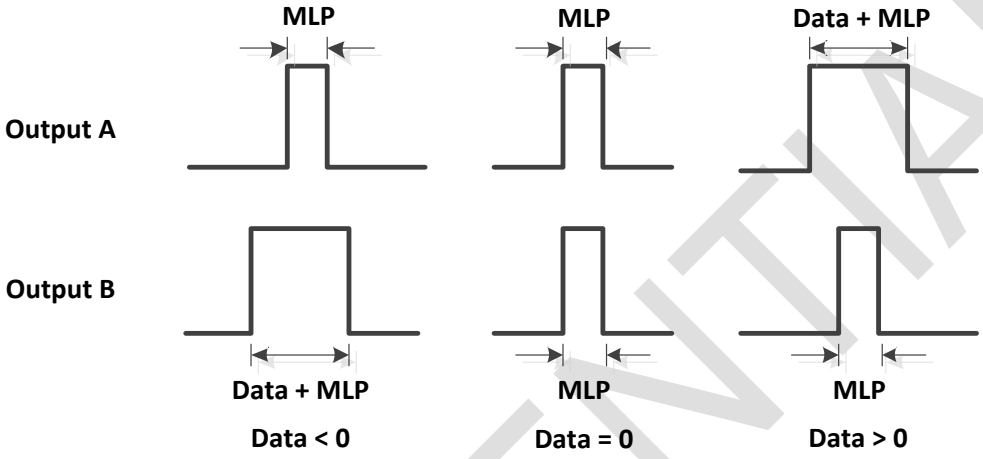


Figure 22. Compensation by MLP

11.4. Soft Start

The soft_start reduces pop noise by controlling rapidly increased energy of PWM.
To begin soft_start operation, PWM soft start enable register (0x52: PSE) should be set to high, and then PWM switching on/off register (0x27: POF) should be set to low. The duty ratio of PWM output increases from 127:1 (Low:High) to 50:50 (Low:High). Step repeat time register (0x52: SRT) means repeat number of PWM output. Soft_start operation with 17 repetitions is shown in the **Figure 23**.

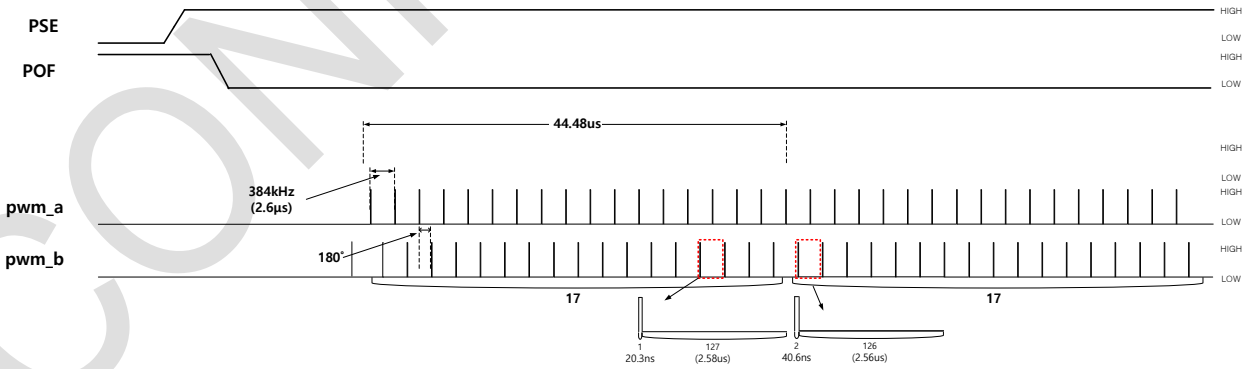
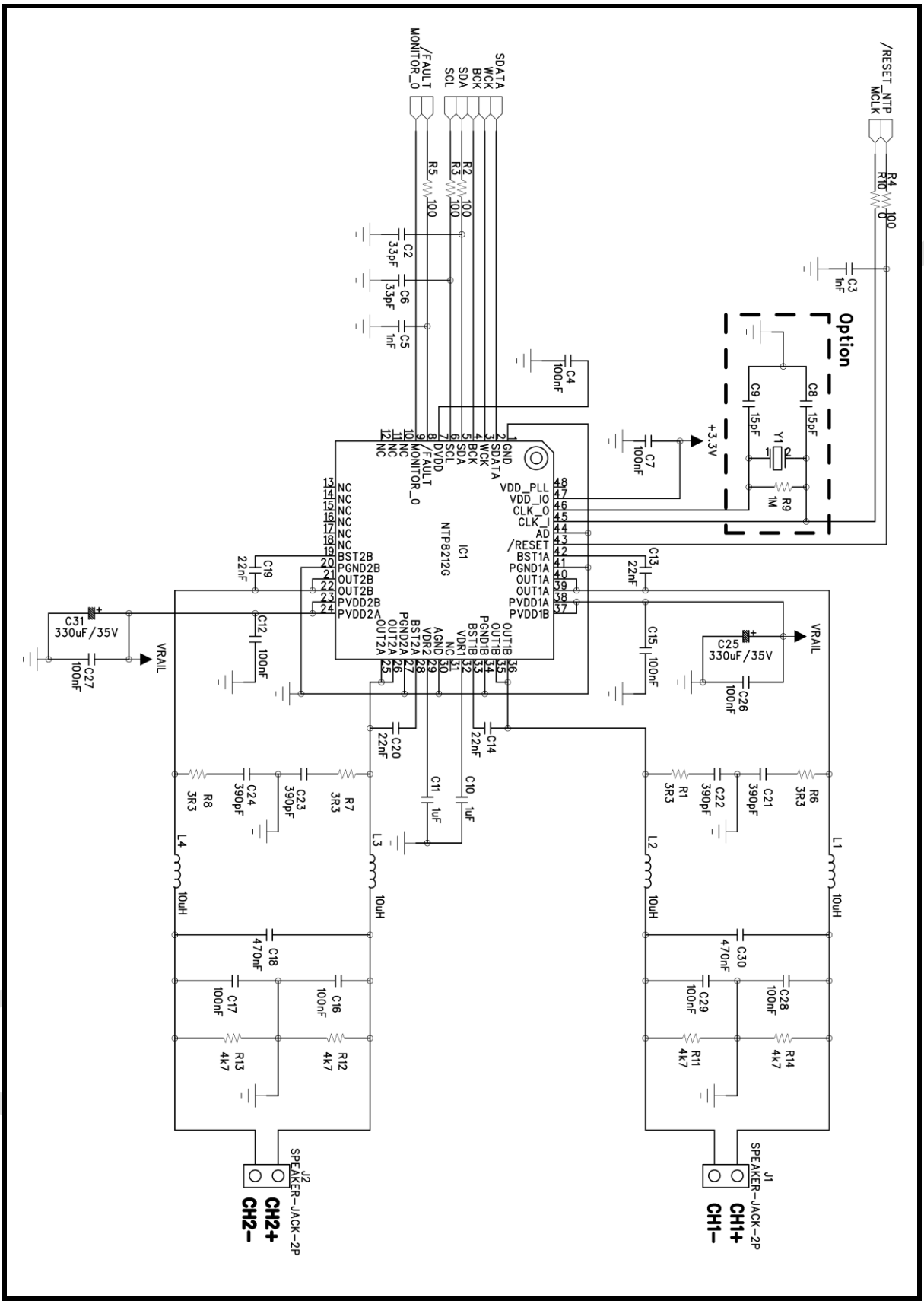


Figure 23. Soft Start Operation Timing

12. TYPICAL APPLICATION SCHEMATICS (2CH Stereo)



13. APPENDIX

A. Configuration Register Summary

Addr 0x00: Audio Input Format

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	FSM			INS	

Name	Description	Value	Meaning	Ref.
INS	Input format	**b'00**	I^2S, slave mode	
		b'01	I^2S, master mode	
		b'10	General serial audio, slave mode	
		b'11	General serial audio, master mode	
FSM	Sampling Frequency in Master mode I^2S	b'**000**	48 kHz	
		b'001	8 kHz	
		b'010	16 kHz	
		b'011	32 kHz	
		b'100	12 kHz	
		b'101	24 kHz	
		b'110	96 kHz	
		b'111	192 kHz	

Addr 0x01: General Serial Audio Format

Bit	7	6	5	4	3	2	1	0
Name	X	X	BCKS		BS		MLF	LRJ

Name	Description	Value	Meaning	Ref.
LRJ	Serial data justify	**b'0**	Left justify	
		b'1	Right justify	
MLF	Serial bit order	**b'0**	MSB first	
		b'1	LSB first	
BS	Serial bit size	**b'00**	24 bit	
		b'01	20 bit	
		b'10	18 bit	
		b'11	16 bit	
BCKS	Bit clock size select	**b'00**	64 BCK/WCK	
		b'01	48 BCK/WCK	
		b'10	32 BCK/WCK	

Addr 0x02: Master Clock Frequency Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	MCF	

Name	Description	Value	Meaning	Ref.
MCF	Master Clock Frequency	**b'00**	12.288 MHz	
		b'01	24.576 MHz	
		b'10	18.432 MHz	
		b'11	User defined frequency.	

Addr 0x03~0x06: Mixer Gain

Bit	7	6	5	4	3	2	1	0
Name	X	MG						

Name	Description	Value	Meaning	Ref.
MG	Mixer gain	h'00 ~ h'7F	Mixer gain (refer to gain table)	

Reserved Addr 0x07~0x0B

Addr 0x0C: Front Bi-quad Filter Chain (FBQ) Configurations for Ch 1&2

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	FBQ22	FBQ21	FBQ12	FBQ11

Name	Description	Value	Meaning	Ref.
FBQ11	1st FBQ flag for CH1	**b'0**	Bypass	
		b'1	Enable	
FBQ12	2nd FBQ flag for CH1	**b'0**	Bypass	
		b'1	Enable	
FBQ21	1st FBQ flag for CH2	**b'0**	Bypass	
		b'1	Enable	
FBQ22	2nd FBQ flag for CH2	**b'0**	Bypass	
		b'1	Enable	

Addr 0x0D: 3D Delay Amount

Bit	7	6	5	4	3	2	1	0
Name	X	X	3D_Delay					

Name	Description	Value	Meaning	Ref.
3D_Delay	3D_Delay	**h'01**	0 ~ 40 (unsigned decimal)	

Addr 0x0E: 3D Effect Control Configuration

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	X	3DEN

Name	Description	Value	Meaning	Ref.
3DEN	3D Bypass Flag	**b'0**	3D off	
		b'1	3D on	

Addr 0x0F: Equalizer (EQ) Configuration

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	EQ	

Name	Description	Value	Meaning	Ref.
EQ	Graphic equalizer configuration	**b'00**	**Bypass**	
		b'01	5-band graphic equalizer (GEQ) mode (0x10~0x14 let GEQ choose preset BQ coeffs)	
		b'11	Programmable Graphic Equalizer (PEQ) 5 biquad chain is programmed for application-specific equalizer (refer to 0x7E register to program)	

Addr 0x10~0x14: GEQ Gain for Band 1 ~ 5

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	BG				

Name	Description	Value	Meaning	Ref.
BG	Band Gain		See register value table.	

Name	Address	Band	Default	GEQ Default frequency	Ref.
BG	0x10	BQ1	b'00000	100Hz	
	0x11	BQ2	b'00000	300Hz	
	0x12	BQ3	b'00000	1kHz	
	0x13	BQ4	b'00000	3kHz	
	0x14	BQ5	b'00000	10kHz	

Addr 0x15: CH1&CH2 Prescaler Value Configuration

Bit	7	6	5	4	3	2	1	0
Name	PS							

Name	Description	Value	Meaning	Ref.
PS	Prescaler	h'00 ~ h'FF	208 (**0xD0**)default	

Reserved Addr 0x16

Addr 0x17~0x18: Post Biquad Filter (PBQ) Configuration0 for Ch 1 and Ch 2, respectively

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	BQ5	BQ4	BQ3	BQ2	BQ1

Name	Description	Value	Meaning	Ref.
BQ1	On/off Bi-Quad 1 of ch. n (n= 1,2)	**b'0**	Bypass Bi-Quad 1 of channel n	
		b'1	Enable Bi-Quad 1 of channel n	
BQ2	On/off Bi-Quad 2 of ch. n (n= 1,2)	**b'0**	Bypass Bi-Quad 2 of channel n	
		b'1	Enable Bi-Quad 2 of channel n	
BQ3	On/off Bi-Quad 3 of ch. n (n = 1,2)	**b'0**	Bypass Bi-Quad 3 of channel n	
		b'1	Enable Bi-Quad 3 of channel n	
BQ4	On/off Bi-Quad 4 of ch. n (n = 1,2)	**b'0**	Bypass Bi-Quad 4 of channel n	
		b'1	Enable Bi-Quad 4 of channel n	
BQ5	On/off Bi-Quad 5 of ch. n (n = 1,2)	**b'0**	Bypass Bi-Quad 5 of channel n	
		b'1	Enable Bi-Quad 5 of channel n	

Addr 0x19~0x1A: Post Biquad Filter (PBQ) Configuration1 for Ch 1 and Ch 2, respectively

Bit	7	6	5	4	3	2	1	0
Name	X	X	BQ8		BQ7		BQ6	

Name	Description	Value	Meaning	Ref.
BQ6	On/off Bi-Quad 6 of ch. n (n = 1,2)	**b'00**	Bypass Bi-Quad 6 of channel n	
		b'01	Enable Bi-Quad 6 of channel n	
		b'10	Enable Bi-Quad 6 as Loudness Filter	
BQ7	On/off Bi-Quad 7 of ch. n (n = 1,2)	**b'00**	Bypass Bi-Quad 7 of channel n	
		b'01	Enable Bi-Quad 7 of channel n	
		b'10	Enable Bi-Quad 7 as Loudness Filter	
BQ8	On/off Bi-Quad 8 of ch. n (n = 1,2)	**b'00**	Bypass Bi-Quad 8 of channel n	
		b'01	Enable Bi-Quad 8 of channel n	
		b'10	Enable Bi-Quad 8 as Loudness Filter	

Reserved Addr 0x1B

Addr 0x1C: DRC Control 0

Bit	7	6	5	4	3	2	1	0
Name	CPR_L	CTS_L						

Name	Description	Value	Meaning	Ref.
CTS_L	DRC threshold for low band	**b'000 0000** ~ b'111 1111	-57 ~ 12dB unsigned 7-bit DRC threshold for 1 band mode. In 2 band mode, it will control the threshold of low band. Refer to DRC threshold value table for threshold values.	
CPR_L	DRC enable for low band	**b'0**	Dynamic Range Compression off	
		b'1	Dynamic Range Compression on	

Addr 0x1D: DRC Control 1

Bit	7	6	5	4	3	2	1	0
Name	X	C1C_L			X	A1C_L		

Name	Description	Value	Meaning	Ref.
A1C_L	DRC attack time (low band)	b'000 ~ b'111	Attack time control for 1 band mode. In 2 band mode, it will control the attack time of low band. (See attack time table below.) (**default = b'001**)	
C1C_L	DRC release time (low band)	**b'000** ~ b'111	Release time control for 1 band mode. In 2 band mode, it will control the release time of low band. (See release time table below.)	

Value of Register	Attack time 6dB, fs = 96,000
011	30 msec
010	15 msec
001	8 msec
000	4 msec
111	2 msec
110	1 msec
101	0.5 msec
100	0.25 msec

Table 8. DRC Attack Time Table

Value of Register	Release time 6dB, fs = 96,000
011	5.0 sec
010	2.0 sec
001	1.0 sec
000	0.5 sec
111	0.2 sec
110	0.1 sec
101	0.05sec
100	0.025sec

Table 9. DRC Release Time Table

Addr 0x1E: DRC Control 2

Bit	7	6	5	4	3	2	1	0
Name	CPR_H	CTS_H						

Name	Description	Value	Meaning	Ref.
CTS_H	DRC threshold for high band	**b'000 0000** ~ b'111 1111	-57 ~ 12dB unsigned 7-bit DRC threshold for high band. It has effect only in 2 band mode. Refer to DRC threshold value table for threshold values.	
CPR_H	DRC enable for high band	**b'0**	Dynamic Range Compression off	
		b'1	Dynamic Range Compression on	

Addr 0x1F: DRC Control3

Bit	7	6	5	4	3	2	1	0
Name	X	C1C_H			X	A1C_H		

Name	Description	Value	Meaning	Ref.
A1C_H	DRC attack time (high band)	b'000 ~ b'111	Attack time control for high band mode. It has effect only in 2 band mode. (**default = b'001**) (See attack time table in Addr 0x1D.)	
C1C_H	DRC release time (high band)	**b'000** ~ b'111	Release time control for high band mode. It has effect only in 2 band mode. (See release time table in Addr 0x1D.)	

Reserved Addr 0x20~0x21

Addr 0x22: DRC Control 6

Bit	7	6	5	4	3	2	1	0
Name	CPR_P	CTS_P						

Name	Description	Value	Meaning	Ref.
CTS_P	DRC threshold for post- band	**b'000 0000** ~ b'111 1111	-57 ~ 12dB unsigned 7-bit DRC threshold Refer to DRC threshold value table.	
CPR_P	DRC enable for post-band	**b'0**	Dynamic Range Compression off	
		b'1	Dynamic Range Compression on	

Addr 0x23: DRC Control 7

Bit	7	6	5	4	3	2	1	0
Name	X	C1C_P			X	A1C_P		

Name	Description	Value	Meaning	Ref.
A1C_P	DRC attack time (post-DRC)	b'000 ~ b'111	Attack time (**default = b'001**)	
C1C_P	DRC release time (post-DRC)	b'000 ~ b'111	Release time (**default = b'100**)	

Addr 0x24: DRC Control 8

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	DLL				

Name	Description	Value	Meaning	Ref.
DLL	Delay line length	h'00 ~ **h'14**	Delay line length. 0~20(decimal)	

Addr 0x25: DRC Control 9

Bit	7	6	5	4	3	2	1	0
Name	CCO	DTS1	DTS2	2BM	ASB	RSB	TSB	CAS

Name	Description	Value	Meaning	Ref.
CAS	Coupled Allpass Structure enable	**b'0**	Enable coupled allpass structure	
		b'1	Disable coupled allpass structure	
TSB	Threshold parameter select bit	**b'0**	Uses Threshold parameters in Table	
		b'1	Uses Threshold parameters from external loading	
RSB	Release parameter select bit	**b'0**	Uses Release parameters in Table	
		b'1	Uses Release parameters from external loading	
ASB	Attack parameter select bit	**b'0**	Uses Attack parameters in Table	
		b'1	Uses Attack parameters from external loading	
2BM	2band mode enable	**b'0**	1 band DRC	
		b'1	2 band DRC	
DTS2	P-DRC type select	**b'0**	P-DRC new mode	
		b'1	P-DRC old mode	
DTS1	LH-DRC type select	**b'0**	LH-DRC new mode	
		b'1	LH-DRC old mode	
CCO	Clip control option	**b'0**	Clip on	
		b'1	Clip off	

※ case. 1band DRC : CAS must be enabled.

Addr 0x26: Soft Mute Control 0

Bit	7	6	5	4	3	2	1	0
Name	SMH	X	X	X	X	X	SM2	SM1

Name	Description	Value	Meaning	Ref.
SMn	Softmute	b'0	increase for channel n	
		b'1	decrease for channel n	
SMH	Softmute speed	**b'0**	42/46 msec(at 96/88.2kHz))	
		b'1	Hard change	

Addr 0x27: PWM Switching On/Off Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	POF2	POF1

Name	Description	Value	Meaning	Ref.
POFn	Switching output On/off control	b'0	Channel n PWM switching on	
		b'1	Channel n PWM switching off	

Addr 0x28: PWM_MASK Control 0

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	SRD	FPMLD	PWMM	

Name	Description	Value	Meaning	Ref.
PWMM	PWM MASK register	**b'10**	PWM MASK output is low. (reset default)	
		otherwise	PWM MASK output is high.	
FPMLD	Permanent PWM_MASK Low disable flag	**b'0**	No effect	
		b'1	Reset the auto_PWM_MASK_restore_counter to 0	
SRD	FAULT disable	**b'0**	FAULT is effect for PROTECT	
		b'1	FAULT is ineffective for PROTECT	

Addr 0x29: PWM_MASK Control 1

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	APM	POF

Name	Description	Value	Meaning	Ref.
POF	PWM off flag	**b'0**	Even if Auto PWM_MASK condition is met, the PWM output of all channel is not affected.	
		b'1	When Auto PWM_MASK condition is met, the PWM output of all channel goes to the defined state which is set by the PWM off state control register (Addr 0x38).	
APM	PWM_MASK flag	**b'0**	Even if Auto PWM_MASK condition is met, the PWM_MASK output of all channel is not affected.	
		b'1	When Auto PWM_MASK condition is met, the PWM_MASK output goes to Low state.	

Addr 0x2A: PWM_MASK Control 2

Bit	7	6	5	4	3	2	1	0
Name	VMSK3	VMSK2	VMSK1	VMSK0	PMSK3	PMSK2	PMSK1	PMSK0

Name	Description	Value	Meaning	Ref.
PMSK	Masking bit of PWM off control	**b'0**	Mask bit indicating the validity of n-th bit of Addr 0x5E system register: If the n-th bit of this register is zero, the n-th bit of Addr 0x5E system register is invalid. The n-th bit of Addr 0x5E is valid only when the n-th mask bit is one.	
		b'1		
VMSK	Masking bit of PWM_MASK signal	**b'0**		
		b'1		

Addr 0x2B: PWM_MASK Control 3

Bit	7	6	5	4	3	2	1	0
Name	IRC		AVRCT			PHT		

Name	Description	Value	Meaning	Ref.
PHT	PWM_MASK Low Hold Time	b'000	0.5 msec Hold Time	
		b'001	1 msec Hold Time	
		b'010	2 msec Hold Time	
		b'011	4 msec Hold Time (Default)	
		b'100	8 msec Hold Time	
		b'101	16msec Hold Time	
AVRCT	Auto PWM_MASK Restore Counter Threshold	b'000	2	
		b'001	5 (Default)	
		b'010	10	
		b'011	15	
		b'100	20	
		b'101	25	
		b'110	30	
		b'111	Infinity	
IRC	Auto PWM_MASK Restore Interval Ratio Control	**b'00**	2 (Default)	
		b'01	4	

Addr 0x2C: PWM_MASK Control 4

Bit	7	6	5	4	3	2	1	*0*
Name	SHE	POE	X	X	X	HT2		

Name	Description	Value	Meaning	*Ref.*
HT2	Hold Time 2 apply start point (restore counter)	b'000	100 msec Hold Time	
		b'001	200 msec Hold Time	
		b'010	400 msec Hold Time	
		b'011	600 msec Hold Time (Default)	
		b'100	800 msec Hold Time	
		b'101	1 sec Hold Time	
		b'110	2 sec Hold Time	
POE	PWM off when PWM_MASK off and PWM on when PWM_MASK Recovers	b'0	Disable	
		b'1	Enable (Default)	
SHE	Second Hold time Enable	**b'0**	Disable (Default)	
		b'1	Enable	

Addr 0x2D: Master Volume Fine Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	MVFC		

Name	Description	Value	Meaning	Ref.
MVFC	Master volume fine control	**h'0** ~ h'7	0 dB ~ 0.5 dB with 0.0625 dB step	

Addr 0x2E~0x30: Master Volume, and Ch1/2 Volume, respectively

Bit	7	6	5	4	3	2	1	0
Name	VOL							

Name	Description	Value	Meaning	Ref.
VOL	Volume control	h'00 ~ h'FF	See volume control register tables. Reset default is 0 (**0x00**) (= −∞ dB)for Master and 207 (**0xCF**) for Channel	

Reserved Addr 0x31

Addr 0x32: Soft Volume Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	SVI	

Name	Description	Value	Meaning	Ref.
SVI	Soft volume change	**b'00**	Medium speed	
		b'01	High speed	
		b'10	Low speed	
		b'11	soft volume change disable	

Addr 0x33: Auto-Mute Control for CH1 & CH2

Bit	7	6	5	4	3	2	1	0
Name	X	EAMC	II		AT			

Name	Description	Value	Meaning	Ref.
AT	Auto-mute detection threshold	**b'0000** ~ b'1111	Unsigned integer between 0 and 15	
II	Auto-mute response time	**b'00**	5 msec	
		b'01	50 msec	
		b'10	500 msec	
		b'11	2 sec	
EAMC	Effect of Auto-mute condition	**b'0**	Auto mute disable(No-Effect)	
		b'1	Continue switching if auto-mute	

Reserved Addr 0x34~0x37

Addr 0x38: Miscellaneous PWM Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	BHL	AHL	MD	

Name	Description	Value	Meaning	Ref.
MD	PWM output mode	**b'00**	AD mode with asynchronous signal pair	
		b'01	AD mode with synchronous signal pair	
		b'10	PWM D-BTL MODE (see 0x4E)	
		b'11	AM Interference mode	
AHL	A-out state When switching off	**b'0**	Low	
		b'1	High	
BHL	B-out state when switching off	**b'0**	Low	
		b'1	High	

Addr 0x39: I2C Glitch Filter

Bit	7	6	5	4	3	2	1	0
Name	GFO	DUR						

Name	Description	Value	Meaning	Ref.
DUR	glitch width	b'000 0000 ~ b'111 1111	minimum pulse width = DUR + 20 ns reset default = 15 * 10 ns (DUR default = **b'0001111**)	
GFO	Glitch filter enable/disable	**b'0**	Glitch filter on	
		b'1	Bypass	

Reserved Addr 0x3A~0x4D

Addr 0x4E: PWM D-BTL MODE Control 0

Bit	7	6	5	4	3	2	1	0
Name	X	MLP						

Name	Description	Value	Meaning	Ref.
MLP	Minimum Linear pulse length	**h'08**	Range : Minimum Pulse Width ~ 640ns, 20ns step.(refer Addr 0x55 for Minimum Pulse Width)	

Reserved Addr 0x4F

Addr 0x50: PWM D-BTL Mode Control 1

Bit	7	6	5	4	3	2	1	0
Name	X						NSS	

Name	Description	Value	Meaning	Ref.
NSS	NS Select	**b'00**	7bits NS (AD mode)	
		b'01	Reserved	
		b'10	8bits NS	
		b'11	New 8bits NS (D-BTL mode)	

Reserved Addr 0x51

Addr 0x52: PWM Soft Start

Bit	7	6	5	4	3	2	1	0
Name	PSE	SRT						

Name	Description	Value	Meaning	Ref.
SRT	Step Repeat Time	b'000 0000 ~ b'111 1111	The repeat time of each step (default : **b'0010000** – means repeat 17 times)	
PSE	BTL PWM soft start Enable	b'0	Disable	
		b'1	Enable (Default)	

Addr 0x53: Power Meter Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	PDPOS	X	X	PDCH	

Name	Description	Value	Meaning	Ref.
PDCH	Power meter Detect Channel	**b'00**	L+R (default)	
		b'01	L channel	
		b'10	R channel	
		b'11	reserved	
PDPOS	Power meter Detect Position	**b'0**	After volume (default)	
		b'1	Before volume	

Addr 0x54: Power Meter (read-only)

Bit	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0

Addr 0x55: Modulation Index & NS-Type Control

Bit	7	6	5	4	3	2	1	0
Name	X	M0		NT	X	X	MD12	

Name	Description	Value	Meaning	Ref.
MD12	Modulation index control by Minimum pulse width for Ch 1&2	b'00	Minimum pulse width = 80ns	
		b'01	Minimum pulse width = 60ns	
		b'10	Minimum pulse width = 40ns	
		b'11	Minimum pulse width = 20ns	
NT	Noise shaping Type for Ch 1&2	**b'0**	Type 1 (fourth order)	
		b'1	Type 2 (fifth order)	
M0	Dither Position Selector	**b'00**	No left shift on dither value = Dither off	
		b'01	1bit left shift on dither value	
		b'10	2bit left shift on dither value	
		b'11	3bit left shift on dither value	

Addr 0x56: ASRC Control 0

Bit	*7*	*6*	*5*	*4*	*3*	*2*	*1*	*0*
Name	X	X	DCESW	X	FSFHM	FSFSM	X	BYPASS

Name	Description	Value	Meaning	*Ref.*
BYPASS	Bypass	b'0	Normal operation	
		b'1	Bypass	
FSFSM	frequency stable effect on soft mute flag	**b'0**	no effect on soft mute flag	
		b'1	soft mute flag = 1 when unstable state	
FSFHM	frequency stable effect on hard mute flag	**b'0**	no effect on hard mute flag	
		b'1	hard mute flag = 1 when unstable state	
DCESW	DC Check Enable of SRC WCK	b'0	DC Check Disable in SRC WCK	
		b'1	DC Check Enable in SRC WCK	

Reserved Addr 0x57~0x58

Addr 0x59 Watch Dog Error System Status (read only)

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	X	WDE

Name	Description	Value	Meaning	Ref.
WDE	Watch Dog Ratio Error	b'0		
		b'1	Watch Dog Error	

Addr 0x5A: POP CONF0

Bit	7	6	5	4	3	2	1	0
Name	RST							

Name	Description	Value	Meaning	Ref.
RST	Release Time	**unsigned 0x10**	CLK error should not occur during RST Unit in 10msec	

Addr 0x5B: POP CONF1

Bit	7	6	5	4	3	2	1	0
Name	ULM[15:8]							

Name	Description	Value	Meaning	Ref.
ULM	Upper Limit	**Unsigned 0x01**	Upper limit on ratio of BCK to CLK_FR	

Addr 0x5C: POP CONF2

Bit	7	6	5	4	3	2	1	0
Name	ULM[7:0]							

Name	Description	Value	Meaning	Ref.
ULM	Upper Limit	**unsigned 0x00**	Upper limit on ratio of BCK to CLK_FR	

Addr 0x5D: POP CONF3

Bit	7	6	5	4	3	2	1	0
Name	LLM[3:0]				X	X	X	WON

Name	Description	Value	Meaning	Ref.
WON	Watch-dog On	**1'b0**	OFF	
		1'b1	ON	
LLM	Lower Limit	**unsigned 'b0100**	Lower limit on ratio of BCK to CLK_FR	

Reserved Addr 0x56~0x5D

Addr 0x5E: System Error Status (read-only)

Bit	7	6	5	4	3	2	1	0
Name	FSI				MPW	LSRC	ULCK	PPM

Name	Description	Value	Meaning	Ref.
PPM	Permanent PWM_MASK Indication flag	b'0		
		b'1	Indicated that PWM_MASK is in Permanent LOW state	
ULCK	Sampled PLL Unlock error	b'0	PLL is locked state.	
		b'1	PLL is unlocked state.	
LSRC	SRC lock status	b'0	SRC is unlocked state.	
		b'1	SRC is locked state	
MPW	MCK/WCK Ratio error	b'0	Ratio is incorrect.	
		b'1	Ratio is correct.	
FSI	Sampling Frequency Information	b'0000	8 KHz	
		b'0010	12 kHz	
		b'0011	16 kHz	
		b'0100	22.025kHz	
		b'0101	24 kHz	
		b'0110	32 kHz	
		b'0111	44.1 kHz	
		b'1000	48 kHz	
		b'1001	88.2 kHz	
		b'1010	96 kHz	
		b' 1100	192 kHz	

Addr 0x5F: Monitor

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	Monitor 0			

Name	Description	Value	Meaning	Ref.
Monitor 0		b'0000	Soft_reset => Monitor 0 pin	
		b'0001	Pwm1a=> Monitor 0 pin	
		b'0010	Pwm1b => Monitor 0 pin	
		b'0011	Pwm2a => Monitor 0 pin	
		b'0100	Pwm2b => Monitor 0 pin	
		b'0111	Pwm_mask => Monitor 0 pin	
		b'1000	SDATA OUT => Monitor 0 pin	

Reserved Addr 0x60

Addr 0x61: I2S Glitch Filter

Bit	7	6	5	4	3	2	1	0
Name	GFE	WTH						

Name	Description	Value	Meaning	Ref.
WTH	glitch width	b'0000000 ~ b'1111111	minimum pulse width = DUR + 20 ns reset default = 1 * 10 ns (DUR default = **b'0000001**)	
GFE	Glitch filter enable/disable	**b'0**	Glitch filter on	
		b'1	Bypass	

Addr 0x62: Driver Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	SB			KMS	SHDN

Name	Description	Value	Meaning	Ref.
SHDN	Shutdown	**b'0**	SHDN pin go to high	
		b'1	SHDN pin go to low	
KMS	STBY signal output mode	**b'0**	STBY : SB & PWM_MASK	
		b'1	STBY : SB	
SB	Stand-by	b'010	Power Device: Stand-by operation	
		b'110	Power Device: Normal operation	

Reserved Addr 0x63~0x65

Addr 0x66: Power-Die Status (Read-Only)

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	PDS	

Name	Description	Value	Meaning	Ref.
PDS	Power-Die Status	**b'00**	Normal State	
		b'01	Temperature Protection Error	
		b'10	Voltage Protection Error	
		b'11	Current Protection Error	

Reserved Addr 0x67~0x7B

Addr 0x7C: I2S Sdata_Out Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	X	POS_SEL

Name	Description	Value	Meaning	Ref.
POS_SEL	Select Data Position	**b'0**	Output data of Pre-Processor	
		b'1	Input data of Mixer	

Reserved Addr 0x7D

Addr 0x7E: Bi-Quad Filter Coefficient Page

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	PEQ	X	CH2	CH1

Name	Description	Value	Meaning	Ref.
CH1	Coefficient write enable	**b'0**	Disable coefficient write for ch1	
		b'1	Enable coefficient write for ch1	
CH2	Coefficient write enable	**b'0**	Disable coefficient write for ch2	
		b'1	Enable coefficient write for ch2	
PEQ	Coefficient write enable	**b'0**	Disable coefficient write for PEQ	
		b'1	Enable coefficient write for PEQ	

Ref) In convenience, a device programmer can write same biquad filter coefficients for CH1 and CH2 at a single time by setting Reg 0x7E as "x03". See the next pages to know register map and biquad filter.

Addr 0x7F: Chip ID 0x98

B. ROM Address for BiQuads Coefficients and Parameters (Refer to Reg 0x7E)

CH1&CH2 BiQuad Coefficients & Parameters

The value of Reg 0x7E should be 0x01, 0x02 to program BiQuad coefficients and parameters only for channel 1 and channel 2, respectively. In case of Reg 0x7E = "0x03", same values will be applied to channel 1 and 2.

Caution! To program one BiQuad filter, five coefficients (b0,b1,b2,a1,a2) should be written consecutively in incremental address. Otherwise, the chip may be in malfunction mode.

Address (Decimal)	Address (Hexadecimal)	REG 0x7E			Description	Default in Hex
		CH1 only	CH2 only	Both		
0	0x00	0x01	0x02	x03	FBQ1 b0	0x11000000
1	0x01	0x01	0x02	x03	FBQ1 b1	0x20000000
2	0x02	0x01	0x02	x03	FBQ1 b2	0x20000000
3	0x03	0x01	0x02	x03	FBQ1 a1	0x20000000
4	0x04	0x01	0x02	x03	FBQ1 a2	0x20000000
5	0x05	0x01	0x02	x03	FBQ2 b0	0x11000000
6	0x06	0x01	0x02	x03	FBQ2 b1	0x20000000
7	0x07	0x01	0x02	x03	FBQ2 b2	0x20000000
8	0x08	0x01	0x02	x03	FBQ2 a1	0x20000000
9	0x09	0x01	0x02	x03	FBQ2 a2	0x20000000
10	0x0A	0x01	0x02	x03	3D BQ1 b0	0x11000000
11	0x0B	0x01	0x02	x03	3D BQ1 b1	0x20000000
12	0x0C	0x01	0x02	x03	3D BQ1 b2	0x20000000
13	0x0D	0x01	0x02	x03	3D BQ1 a1	0x20000000
14	0x0E	0x01	0x02	x03	3D BQ1 a2	0x20000000
15	0x0F	0x01	0x02	x03	3D BQ2 b0	0x11000000
16	0x10	0x01	0x02	x03	3D BQ2 b1	0x20000000
17	0x11	0x01	0x02	x03	3D BQ2 b2	0x20000000
18	0x12	0x01	0x02	x03	3D BQ2 a1	0x20000000
19	0x13	0x01	0x02	x03	3D BQ2 a2	0x20000000
20	0x14	0x01	0x02	x03	PBQ1 b0	0x11000000
21	0x15	0x01	0x02	x03	PBQ1 b1	0x20000000
22	0x16	0x01	0x02	x03	PBQ1 b2	0x20000000
23	0x17	0x01	0x02	x03	PBQ1 a1	0x20000000
24	0x18	0x01	0x02	x03	PBQ1 a2	0x20000000
25	0x19	0x01	0x02	x03	PBQ2 b0	0x11000000
26	0x1A	0x01	0x02	x03	PBQ2 b1	0x20000000
27	0x1B	0x01	0x02	x03	PBQ2 b2	0x20000000
28	0x1C	0x01	0x02	x03	PBQ2 a1	0x20000000
29	0x1D	0x01	0x02	x03	PBQ2 a2	0x20000000
30	0x1E	0x01	0x02	x03	PBQ3 b0	0x11000000
31	0x1F	0x01	0x02	x03	PBQ3 b1	0x20000000
32	0x20	0x01	0x02	x03	PBQ3 b2	0x20000000
33	0x21	0x01	0x02	x03	PBQ3 a1	0x20000000
34	0x22	0x01	0x02	x03	PBQ3 a2	0x20000000
35	0x23	0x01	0x02	x03	PBQ4 b0	0x11000000
36	0x24	0x01	0x02	x03	PBQ4 b1	0x20000000
37	0x25	0x01	0x02	x03	PBQ4 b2	0x20000000
38	0x26	0x01	0x02	x03	PBQ4 a1	0x20000000
39	0x27	0x01	0x02	x03	PBQ4 a2	0x20000000
40	0x28	0x01	0x02	x03	PBQ5 b0	0x11000000
41	0x29	0x01	0x02	x03	PBQ5 b1	0x20000000
42	0x2A	0x01	0x02	x03	PBQ5 b2	0x20000000

Address (Decimal)	Address (Hexadecimal)	REG 0x7E			Description	Default in Hex
		CH1 only	CH2 only	Both		
43	0x2B	0x01	0x02	x03	PBQ5 a1	0x20000000
44	0x2C	0x01	0x02	x03	PBQ5 a2	0x20000000
45	0x2D	0x01	0x02	x03	PBQ6 b0	0x11000000
46	0x2E	0x01	0x02	x03	PBQ6 b1	0x20000000
47	0x2F	0x01	0x02	x03	PBQ6 b2	0x20000000
48	0x30	0x01	0x02	x03	PBQ6 a1	0x20000000
49	0x31	0x01	0x02	x03	PBQ6 a2	0x20000000
50	0x32	0x01	0x02	x03	PBQ7 b0	0x11000000
51	0x33	0x01	0x02	x03	PBQ7 b1	0x20000000
52	0x34	0x01	0x02	x03	PBQ7 b2	0x20000000
53	0x35	0x01	0x02	x03	PBQ7 a1	0x20000000
54	0x36	0x01	0x02	x03	PBQ7 a2	0x20000000
55	0x37	0x01	0x02	x03	PBQ8 b0	0x11000000
56	0x38	0x01	0x02	x03	PBQ8 b1	0x20000000
57	0x39	0x01	0x02	x03	PBQ8 b2	0x20000000
58	0x3A	0x01	0x02	x03	PBQ8 a1	0x20000000
59	0x3B	0x01	0x02	x03	PBQ8 a2	0x20000000
60	0x3C	0x01	0x02	x03	3D Mixer M1	0x20000000
61	0x3D	0x01	0x02	x03	3D Mixer M2	0x20000000
62	0x3E	0x01	0x02	x03	Loudness gain 1	0x20000000
63	0x3F	0x01	0x02	x03	Loudness gain 2	0x20000000
64	0x40	0x01	0x02	x03	Loudness gain 3	0x20000000
70	0x46			x03	QMF_BQ1 b0	0x0D31EAD7
71	0x47			x03	QMF_BQ1 b1	0x0B1404D4
72	0x48			x03	QMF_BQ1 b2	0x0A140503
73	0x49			x03	QMF_BQ1 a1	0x1164C41A
74	0x4A			x03	QMF_BQ1 a2	0x10D27EE0
75	0x4B			x03	QMF_BQ2 b0	0x0D31EAD7
76	0x4C			x03	QMF_BQ2 b1	0x0D31EA65
77	0x4D			x03	QMF_BQ2 b2	0x20000000
78	0x4E			x03	QMF_BQ2 a1	0x10521801
79	0x4F			x03	QMF_BQ2 a2	0x20000000
80	0x50			x03	QMF_BQ3 b0	0x10680650
81	0x51			x03	QMF_BQ3 b1	0x11E8069C
82	0x52			x03	QMF_BQ3 b2	0x106806E8
83	0x53			x03	QMF_BQ3 a1	0x1164C41A
84	0x54			x03	QMF_BQ3 a2	0x10D27EE0
85	0x55			x03	QMF_BQ4 b0	0x10680650
86	0x56			x03	QMF_BQ4 b1	0x10E805B8
87	0x57			x03	QMF_BQ4 b2	0x20000000
88	0x58			x03	QMF_BQ4 a1	0x10521801
89	0x59			x03	QMF_BQ4 a2	0x20000000
90	0x5A			x03	Attack_low BQ b0	0x0318B4A4
91	0x5B			x03	Attack_low BQ b1	0x0418B4A4
92	0x5C			x03	Attack_low BQ b2	0x0318B4A4
93	0x5D			x03	Attack_low BQ a1	0x117BA189
94	0x5E			x03	Attack_low BQ a2	0x10F75628
95	0x5F			x03	Attack_high BQ b0	0x0318B4A4
96	0x60			x03	Attack_high BQ b1	0x0418B4A4
97	0x61			x03	Attack_high BQ b2	0x0318B4A4
98	0x62			x03	Attack_high BQ a1	0x117BA189
99	0x63			x03	Attack_high BQ a2	0x10F75628
104	0x68			x03	PowerMeter_Gain	0x107FFB49

BiQuad Coefficients for Programmable Equalizer (PEQ)

PEQ BiQuad filters are programmed after setting Reg 0x7E as “0x08”. Also, five coefficients should be consecutively in incremental address form to program one BiQuad filter.

Address (Decimal)	Address (Hexadecimal)	REG 0x7E	Description	Default in Hex
		PEQ		
0	0x00	0x08	PEQ CH1 BQ1 b0	0x11000000
1	0x01	0x08	PEQ CH1 BQ1 b1	0x20000000
2	0x02	0x08	PEQ CH1 BQ1 b2	0x20000000
3	0x03	0x08	PEQ CH1 BQ1 a1	0x20000000
4	0x04	0x08	PEQ CH1 BQ1 a2	0x20000000
5	0x05	0x08	PEQ CH1 BQ2 b0	0x11000000
6	0x06	0x08	PEQ CH1 BQ2 b1	0x20000000
7	0x07	0x08	PEQ CH1 BQ2 b2	0x20000000
8	0x08	0x08	PEQ CH1 BQ2 a1	0x20000000
9	0x09	0x08	PEQ CH1 BQ2 a2	0x20000000
10	0x0A	0x08	PEQ CH1 BQ3 b0	0x11000000
11	0x0B	0x08	PEQ CH1 BQ3 b1	0x20000000
12	0x0C	0x08	PEQ CH1 BQ3 b2	0x20000000
13	0x0D	0x08	PEQ CH1 BQ3 a1	0x20000000
14	0x0E	0x08	PEQ CH1 BQ3 a2	0x20000000
15	0x0F	0x08	PEQ CH1 BQ4 b0	0x11000000
16	0x10	0x08	PEQ CH1 BQ4 b1	0x20000000
17	0x11	0x08	PEQ CH1 BQ4 b2	0x20000000
18	0x12	0x08	PEQ CH1 BQ4 a1	0x20000000
19	0x13	0x08	PEQ CH1 BQ4 a2	0x20000000
20	0x14	0x08	PEQ CH1 BQ5 b0	0x11000000
21	0x15	0x08	PEQ CH1 BQ5 b1	0x20000000
22	0x16	0x08	PEQ CH1 BQ5 b2	0x20000000
23	0x17	0x08	PEQ CH1 BQ5 a1	0x20000000
24	0x18	0x08	PEQ CH1 BQ5 a2	0x20000000
25	0x19	0x08	PEQ CH2 BQ1 b0	0x11000000

Address (Decimal)	Address (Hexadecimal)	REG 0x7E	Description	Default in Hex
		PEQ		
26	0x1A	0x08	PEQ CH2 BQ1 b1	0x20000000
27	0x1B	0x08	PEQ CH2 Baaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaa aaaaaaaaaaaaaaaaaaaaaasQ1 b2	0x20000000
28	0x1C	0x08	PEQ CH2 BQ1 a1	0x20000000
29	0x1D	0x08	PEQ CH2 BQ1 a2	0x20000000
30	0x1E	0x08	PEQ CH2 BQ2 b0	0x11000000
31	0x1F	0x08	PEQ CH2 BQ2 b1	0x20000000
32	0x20	0x08	PEQ CH2 BQ2 b2	0x20000000
33	0x21	0x08	PEQ CH2 BQ2 a1	0x20000000
34	0x22	0x08	PEQ CH2 BQ2 a2	0x20000000
35	0x23	0x08	PEQ CH2 BQ3 b0	0x11000000
36	0x24	0x08	PEQ CH2 BQ3 b1	0x20000000
37	0x25	0x08	PEQ CH2 BQ3 b2	0x20000000
38	0x26	0x08	PEQ CH2 BQ3 a1	0x20000000
39	0x27	0x08	PEQ CH2 BQ3 a2	0x20000000
40	0x28	0x08	PEQ CH2 BQ4 b0	0x11000000
41	0x29	0x08	PEQ CH2 BQ4 b1	0x20000000
42	0x2A	0x08	PEQ CH2 BQ4 b2	0x20000000
43	0x2B	0x08	PEQ CH2 BQ4 a1	0x20000000
44	0x2C	0x08	PEQ CH2 BQ4 a2	0x20000000
45	0x2D	0x08	PEQ CH2 BQ5 b0	0x11000000
46	0x2E	0x08	PEQ CH2 BQ5 b1	0x20000000
47	0x2F	0x08	PEQ CH2 BQ5 b2	0x20000000
48	0x30	0x08	PEQ CH2 BQ5 a1	0x20000000
49	0x31	0x08	PEQ CH2 BQ5 a2	0x20000000

C. Configuration Register Value Reference

Master & Channel Volume

Index	dB	Index	dB	Index	dB	Index	dB	Index	dB	Index	dB
FF	24	D4	2.5	A9	-19	7E	-40.5	53	-62	28	-83.5
FE	23.5	D3	2	A8	-19.5	7D	-41	52	-62.5	27	-84
FD	23	D2	1.5	A7	-20	7C	-41.5	51	-63	26	-84.5
FC	22.5	D1	1	A6	-20.5	7B	-42	50	-63.5	25	-85
FB	22	D0	0.5	A5	-21	7A	-42.5	4F	-64	24	-85.5
FA	21.5	CF	0	A4	-21.5	79	-43	4E	-64.5	23	-86
F9	21	CE	-0.5	A3	-22	78	-43.5	4D	-65	22	-86.5
F8	20.5	CD	-1	A2	-22.5	77	-44	4C	-65.5	21	-87
F7	20	CC	-1.5	A1	-23	76	-44.5	4B	-66	20	-87.5
F6	19.5	CB	-2	A0	-23.5	75	-45	4A	-66.5	1F	-88
F5	19	CA	-2.5	9F	-24	74	-45.5	49	-67	1E	-88.5
F4	18.5	C9	-3	9E	-24.5	73	-46	48	-67.5	1D	-89
F3	18	C8	-3.5	9D	-25	72	-46.5	47	-68	1C	-89.5
F2	17.5	C7	-4	9C	-25.5	71	-47	46	-68.5	1B	-90
F1	17	C6	-4.5	9B	-26	70	-47.5	45	-69	1A	-90.5
F0	16.5	C5	-5	9A	-26.5	6F	-48	44	-69.5	19	-91
EF	16	C4	-5.5	99	-27	6E	-48.5	43	-70	18	-91.5
EE	15.5	C3	-6	98	-27.5	6D	-49	42	-70.5	17	-92
ED	15	C2	-6.5	97	-28	6C	-49.5	41	-71	16	-92.5
EC	14.5	C1	-7	96	-28.5	6B	-50	40	-71.5	15	-93
EB	14	C0	-7.5	95	-29	6A	-50.5	3F	-72	14	-93.5
EA	13.5	BF	-8	94	-29.5	69	-51	3E	-72.5	13	-94
E9	13	BE	-8.5	93	-30	68	-51.5	3D	-73	12	-94.5
E8	12.5	BD	-9	92	-30.5	67	-52	3C	-73.5	11	-95
E7	12	BC	-9.5	91	-31	66	-52.5	3B	-74	10	-95.5
E6	11.5	BB	-10	90	-31.5	65	-53	3A	-74.5	0F	-96
E5	11	BA	-10.5	8F	-32	64	-53.5	39	-75	0E	-96.5
E4	10.5	B9	-11	8E	-32.5	63	-54	38	-75.5	0D	-97
E3	10	B8	-11.5	8D	-33	62	-54.5	37	-76	0C	-97.5
E2	9.5	B7	-12	8C	-33.5	61	-55	36	-76.5	0B	-98
E1	9	B6	-12.5	8B	-34	60	-55.5	35	-77	0A	-98.5
E0	8.5	B5	-13	8A	-34.5	5F	-56	34	-77.5	9	-99
DF	8	B4	-13.5	89	-35	5E	-56.5	33	-78	8	-99.5
DE	7.5	B3	-14	88	-35.5	5D	-57	32	-78.5	7	-100
DD	7	B2	-14.5	87	-36	5C	-57.5	31	-79	6	-110
DC	6.5	B1	-15	86	-36.5	5B	-58	30	-79.5	5	-120
DB	6	B0	-15.5	85	-37	5A	-58.5	2F	-80	4	-130
DA	5.5	AF	-16	84	-37.5	59	-59	2E	-80.5	3	-140
D9	5	AE	-16.5	83	-38	58	-59.5	2D	-81	2	-150
D8	4.5	AD	-17	82	-38.5	57	-60	2C	-81.5	1	-150
D7	4	AC	-17.5	81	-39	56	-60.5	2B	-82	0	-150
D6	3.5	AB	-18	80	-39.5	55	-61	2A	-82.5		
D5	3	AA	-18.5	7F	-40	54	-61.5	29	-83		

Mixer Gain & Polarity

Index	Polarity	dB	Index	Polarity	dB	Index	Polarity	dB	Index	Polarity	dB
7E	+	18	7D	-	18	3E	+	-4	3D	-	-4
7C	+	17	7B	-	17	3C	+	-4.5	3B	-	-4.5
7A	+	16	79	-	16	3A	+	-5	39	-	-5
78	+	15	77	-	15	38	+	-5.5	37	-	-5.5
76	+	14	75	-	14	36	+	-6	35	-	-6
74	+	13	73	-	13	34	+	-7	33	-	-7
72	+	12	71	-	12	32	+	-8	31	-	-8
70	+	11	6F	-	11	30	+	-9	2F	-	-9
6E	+	10	6D	-	10	2E	+	-10	2D	-	-10
6C	+	9	6B	-	9	2C	+	-11	2B	-	-11
6A	+	8	69	-	8	2A	+	-12	29	-	-12
68	+	7	67	-	7	28	+	-13	27	-	-13
66	+	6	65	-	6	26	+	-14	25	-	-14
64	+	5.5	63	-	5.5	24	+	-15	23	-	-15
62	+	5	61	-	5	22	+	-16	21	-	-16
60	+	4.5	5F	-	4.5	20	+	-17	1F	-	-17
5E	+	4	5D	-	4	1E	+	-18	1D	-	-18
5C	+	3.5	5B	-	3.5	1C	+	-19	1B	-	-19
5A	+	3	59	-	3	1A	+	-20	19	-	-20
58	+	2.5	57	-	2.5	18	+	-21	17	-	-21
56	+	2	55	-	2	16	+	-22	15	-	-22
54	+	1.5	53	-	1.5	14	+	-23	13	-	-23
52	+	1	51	-	1	12	+	-24	11	-	-24
50	+	0.5	4F	-	0.5	10	+	-25	0F	-	-25
4E	+	0	4D	-	0	0E	+	-26	0D	-	-26
4C	+	-0.5	4B	-	-0.5	0C	+	-27	0B	-	-27
4A	+	-1	49	-	-1	0A	+	-28	09	-	-28
48	+	-1.5	47	-	-1.5	08	+	-29	07	-	-29
46	+	-2	45	-	-2	06	+	-30	05	-	-30
44	+	-2.5	43	-	-2.5	04	+	-31	03	-	-31
42	+	-3	41	-	-3	02	+	-32	01	-	-32
40	+	-3.5	3F	-	-3.5	00	+	-150			

Dynamic Range Control Threshold

dB	Value	dB	Value	dB	Value	dB	Value
-57	FF	-5.5	DF	-2.3	BF	0.9	9F
-54	FE	-5.4	DE	-2.2	BE	1	9E
-51	FD	-5.3	DD	-2.1	BD	1.25	9D
-48	FC	-5.2	DC	-2	BC	1.5	9C
-45	FB	-5.1	DB	-1.9	BB	1.75	9B
-42	FA	-5	DA	-1.8	BA	2	9A
-39	F9	-4.9	D9	-1.7	B9	2.25	99
-36	F8	-4.8	D8	-1.6	B8	2.5	98
-33	F7	-4.7	D7	-1.5	B7	2.75	97
-30	F6	-4.6	D6	-1.4	B6	3	96
-27	F5	-4.5	D5	-1.3	B5	3.25	95
-24	F4	-4.4	D4	-1.2	B4	3.5	94
-21	F3	-4.3	D3	-1.1	B3	3.75	93
-18	F2	-4.2	D2	-1	B2	4	92
-15	F1	-4.1	D1	-0.9	B1	4.25	91
-12	F0	-4	D0	-0.8	B0	4.5	90
-11.5	EF	-3.9	CF	-0.7	AF	4.75	8F
-11	EE	-3.8	CE	-0.6	AE	5	8E
-10.5	ED	-3.7	CD	-0.5	AD	5.5	8D
-10	EC	-3.6	CC	-0.4	AC	6	8C
-9.5	EB	-3.5	CB	-0.3	AB	6.5	8B
-9	EA	-3.4	CA	-0.2	AA	7	8A
-8.5	E9	-3.3	C9	-0.1	A9	7.5	89
-8	E8	-3.2	C8	0	A8	8	88
-7.5	E7	-3.1	C7	0.1	A7	8.5	87
-7	E6	-3	C6	0.2	A6	9	86
-6.5	E5	-2.9	C5	0.3	A5	9.5	85
-6	E4	-2.8	C4	0.4	A4	10	84
-5.9	E3	-2.7	C3	0.5	A3	10.5	83
-5.8	E2	-2.6	C2	0.6	A2	11	82
-5.7	E1	-2.5	C1	0.7	A1	11.5	81
-5.6	E0	-2.4	C0	0.8	A0	12	80

※ CPR bit = 1

Auto Mute Detection Threshold Table

Name	Description	Value	dB
AT	Auto-mute Detection threshold	0000	-126
		0001	-120
		0010	-114
		0011	-108
		0100	-102
		0101	-96
		0110	-90
		0111	-84
		1000	-78
		1001	-72
		1010	-66
		1011	-60
		1100	-54
		1101	-48
		1110	-42
		1111	**Auto-mute**

※ Do not use value 1111.

Graphic Equalizer Band Gain

Value(HEX)	dB
14	-12
15	-11
16	-10
17	-9
18	-8
19	-7
1A	-6
1B	-5
1C	-4
1D	-3
1E	-2
1F	-1
00	0
01	1
02	2
03	3
04	4
05	5
06	6
07	7
08	8
09	9
0A	10
0B	11
0C	12

Power Meter Reading Table

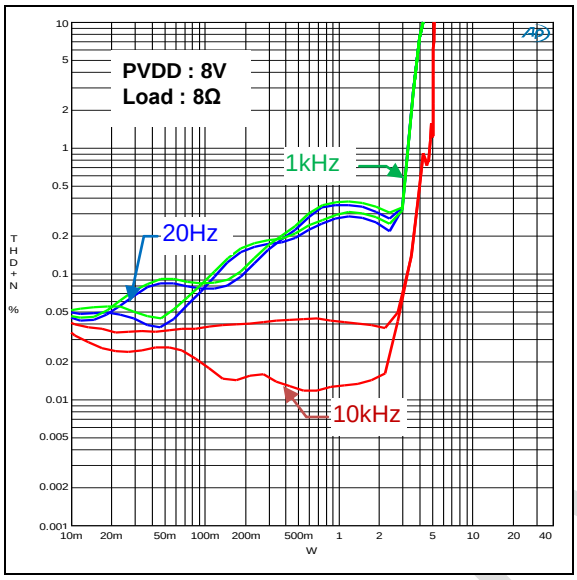
addr 0x54 (Decimal)	addr 0x54 (Hex)	dB	addr 0x54 (Decimal)	addr 0x54 (Hex)	dB	addr 0x54 (Decimal)	addr 0x54 (Hex)	dB	addr 0x54 (Decimal)	addr 0x54 (Hex)	dB
0	0x00	-0.0	64	0x40	-32.0	128	0x80	-64.0	192	0xC0	-96.0
1	0x01	-0.5	65	0x41	-32.5	129	0x81	-64.5	193	0xC1	-96.5
2	0x02	-1.0	66	0x42	-33.0	130	0x82	-65.0	194	0xC2	-97.0
3	0x03	-1.5	67	0x43	-33.5	131	0x83	-65.5	195	0xC3	-97.5
4	0x04	-2.0	68	0x44	-34.0	132	0x84	-66.0	196	0xC4	-98.0
5	0x05	-2.5	69	0x45	-34.5	133	0x85	-66.5	197	0xC5	-98.5
6	0x06	-3.0	70	0x46	-35.0	134	0x86	-67.0	198	0xC6	-99.0
7	0x07	-3.5	71	0x47	-35.5	135	0x87	-67.5	199	0xC7	-99.5
8	0x08	-4.0	72	0x48	-36.0	136	0x88	-68.0	200	0xC8	-100.0
9	0x09	-4.5	73	0x49	-36.5	137	0x89	-68.5	201	0xC9	-100.5
10	0x0A	-5.0	74	0x4A	-37.0	138	0x8A	-69.0	202	0xCA	-101.0
11	0x0B	-5.5	75	0x4B	-37.5	139	0x8B	-69.5	203	0xCB	-101.5
12	0x0C	-6.0	76	0x4C	-38.0	140	0x8C	-70.0	204	0xCC	-102.0
13	0x0D	-6.5	77	0x4D	-38.5	141	0x8D	-70.5	205	0xCD	-102.5
14	0x0E	-7.0	78	0x4E	-39.0	142	0x8E	-71.0	206	0xCE	-103.0
15	0x0F	-7.5	79	0x4F	-39.5	143	0x8F	-71.5	207	0xCF	-103.5
16	0x10	-8.0	80	0x50	-40.0	144	0x90	-72.0	208	0xD0	-104.0
17	0x11	-8.5	81	0x51	-40.5	145	0x91	-72.5	209	0xD1	-104.5
18	0x12	-9.0	82	0x52	-41.0	146	0x92	-73.0	210	0xD2	-105.0
19	0x13	-9.5	83	0x53	-41.5	147	0x93	-73.5	211	0xD3	-105.5
20	0x14	-10.0	84	0x54	-42.0	148	0x94	-74.0	212	0xD4	-106.0
21	0x15	-10.5	85	0x55	-42.5	149	0x95	-74.5	213	0xD5	-106.5
22	0x16	-11.0	86	0x56	-43.0	150	0x96	-75.0	214	0xD6	-107.0
23	0x17	-11.5	87	0x57	-43.5	151	0x97	-75.5	215	0xD7	-107.5
24	0x18	-12.0	88	0x58	-44.0	152	0x98	-76.0	216	0xD8	-108.0
25	0x19	-12.5	89	0x59	-44.5	153	0x99	-76.5	217	0xD9	-108.5
26	0x1A	-13.0	90	0x5A	-45.0	154	0x9A	-77.0	218	0xDA	-109.0
27	0x1B	-13.5	91	0x5B	-45.5	155	0x9B	-77.5	219	0xDB	-109.5
28	0x1C	-14.0	92	0x5C	-46.0	156	0x9C	-78.0	220	0xDC	-110.0
29	0x1D	-14.5	93	0x5D	-46.5	157	0x9D	-78.5	221	0xDD	-110.5
30	0x1E	-15.0	94	0x5E	-47.0	158	0x9E	-79.0	222	0xDE	-111.0
31	0x1F	-15.5	95	0x5F	-47.5	159	0x9F	-79.5	223	0xDF	-111.5
32	0x20	-16.0	96	0x60	-48.0	160	0xA0	-80.0	224	0xE0	-112.0
33	0x21	-16.5	97	0x61	-48.5	161	0xA1	-80.5	225	0xE1	-112.5
34	0x22	-17.0	98	0x62	-49.0	162	0xA2	-81.0	226	0xE2	-113.0
35	0x23	-17.5	99	0x63	-49.5	163	0xA3	-81.5	227	0xE3	-113.5
36	0x24	-18.0	100	0x64	-50.0	164	0xA4	-82.0	228	0xE4	-114.0
37	0x25	-18.5	101	0x65	-50.5	165	0xA5	-82.5	229	0xE5	-114.5
38	0x26	-19.0	102	0x66	-51.0	166	0xA6	-83.0	230	0xE6	-115.0
39	0x27	-19.5	103	0x67	-51.5	167	0xA7	-83.5	231	0xE7	-115.5
40	0x28	-20.0	104	0x68	-52.0	168	0xA8	-84.0	232	0xE8	-116.0
41	0x29	-20.5	105	0x69	-52.5	169	0xA9	-84.5	233	0xE9	-116.5
42	0x2A	-21.0	106	0x6A	-53.0	170	0xAA	-85.0	234	0xEA	-117.0
43	0x2B	-21.5	107	0x6B	-53.5	171	0xAB	-85.5	235	0xEB	-117.5
44	0x2C	-22.0	108	0x6C	-54.0	172	0xAC	-86.0	236	0xEC	-118.0
45	0x2D	-22.5	109	0x6D	-54.5	173	0xAD	-86.5	237	0xED	-118.5
46	0x2E	-23.0	110	0x6E	-55.0	174	0xAE	-87.0	238	0xEE	-119.0
47	0x2F	-23.5	111	0x6F	-55.5	175	0xAF	-87.5	239	0xEF	-119.5
48	0x30	-24.0	112	0x70	-56.0	176	0xB0	-88.0	240	0xF0	-120.0
49	0x31	-24.5	113	0x71	-56.5	177	0xB1	-88.5	241	0xF1	-120.5
50	0x32	-25.0	114	0x72	-57.0	178	0xB2	-89.0	242	0xF2	-121.0
51	0x33	-25.5	115	0x73	-57.5	179	0xB3	-89.5	243	0xF3	-121.5
52	0x34	-26.0	116	0x74	-58.0	180	0xB4	-90.0	244	0xF4	-122.0
53	0x35	-26.5	117	0x75	-58.5	181	0xB5	-90.5	245	0xF5	-122.5
54	0x36	-27.0	118	0x76	-59.0	182	0xB6	-91.0	246	0xF6	-123.0
55	0x37	-27.5	119	0x77	-59.5	183	0xB7	-91.5	247	0xF7	-123.5
56	0x38	-28.0	120	0x78	-60.0	184	0xB8	-92.0	248	0xF8	-124.0
57	0x39	-28.5	121	0x79	-60.5	185	0xB9	-92.5	249	0xF9	-124.5
58	0x3A	-29.0	122	0x7A	-61.0	186	0xBA	-93.0	250	0xFA	-125.0
59	0x3B	-29.5	123	0x7B	-61.5	187	0xBB	-93.5	251	0xFB	-125.5
60	0x3C	-30.0	124	0x7C	-62.0	188	0xBC	-94.0	252	0xFC	-126.0
61	0x3D	-30.5	125	0x7D	-62.5	189	0xBD	-94.5	253	0xFD	-126.5
62	0x3E	-31.0	126	0x7E	-63.0	190	0xBE	-95.0	254	0xFE	-127.0
63	0x3F	-31.5	127	0x7F	-63.5	191	0xBF	-95.5	255	0xFF	-127.5 under

Output 8bit value : (-dB * 2), n dB = output 8bit *0.5

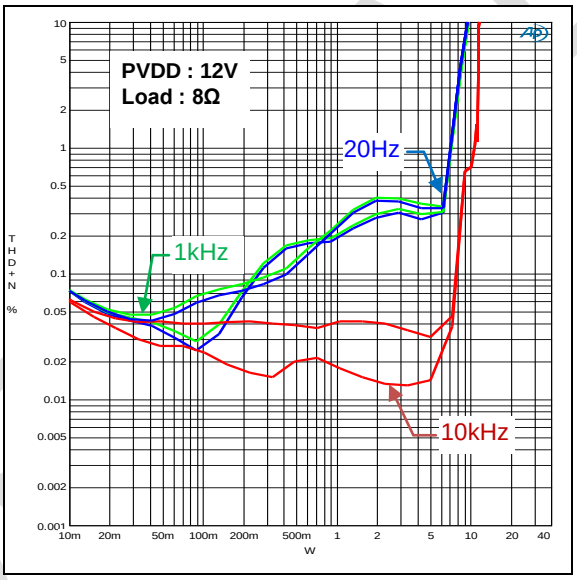
D. Typical Characteristics Graph

Total Harmonic Distortion + Noise vs. Power, BTL Configuration, 8Ω

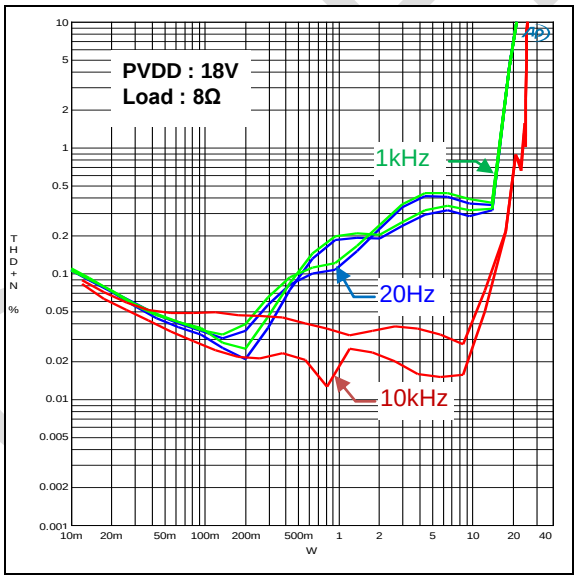
THD+N vs. Power



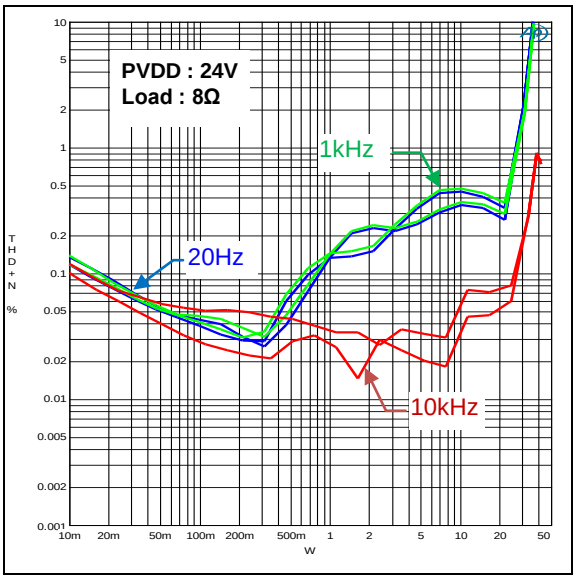
THD+N vs. Power



THD+N vs. Power

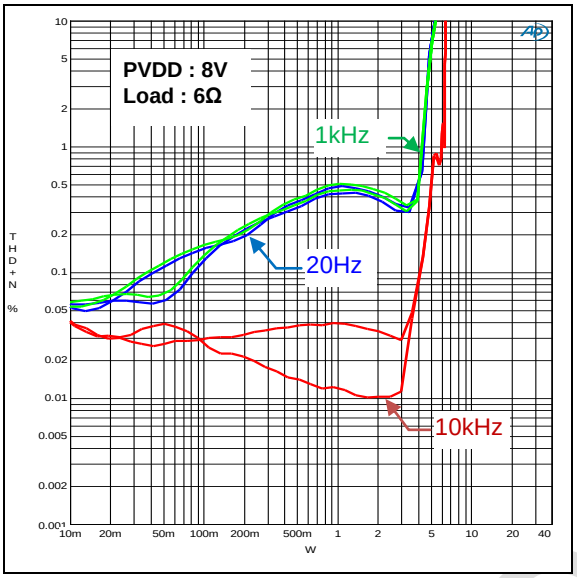


THD+N vs. Power

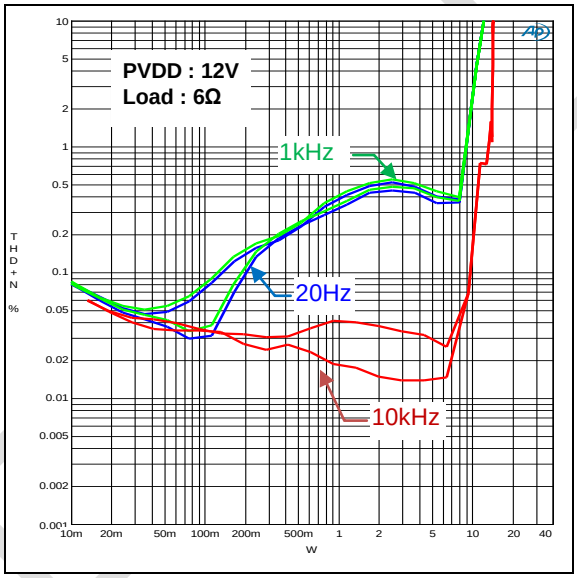


Total Harmonic Distortion + Noise vs. Power, BTL Configuration, 6Ω

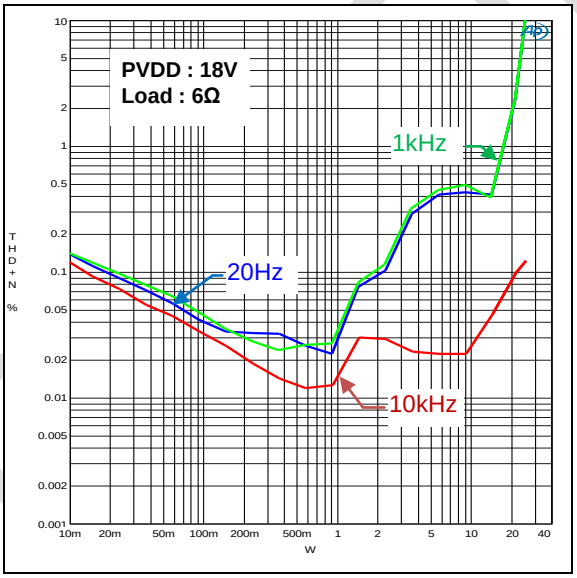
THD+N vs. Power



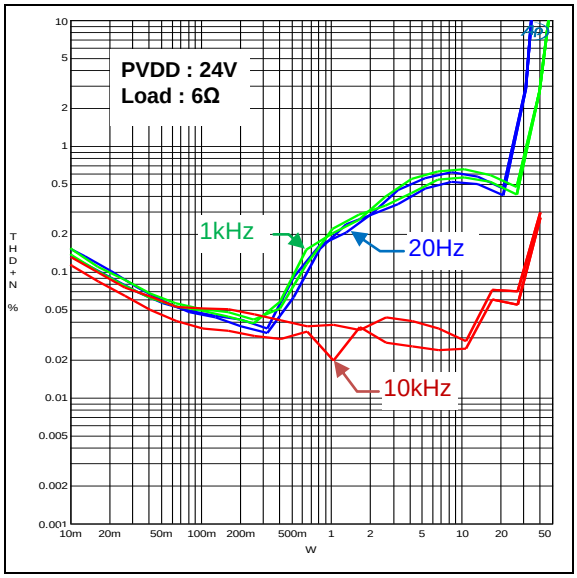
THD+N vs. Power



THD+N vs. Power

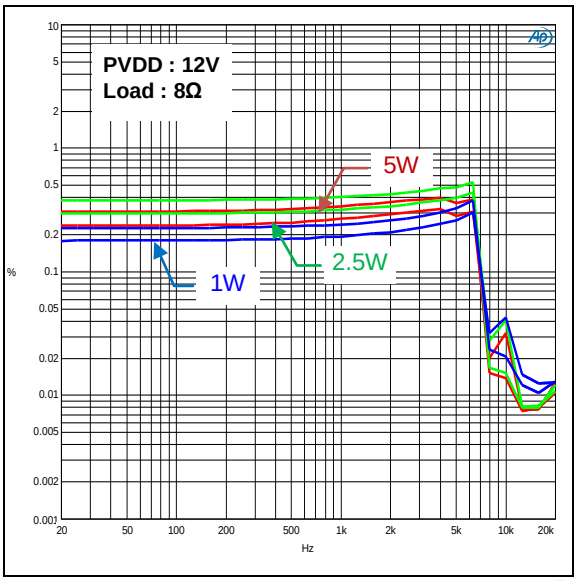


THD+N vs. Power

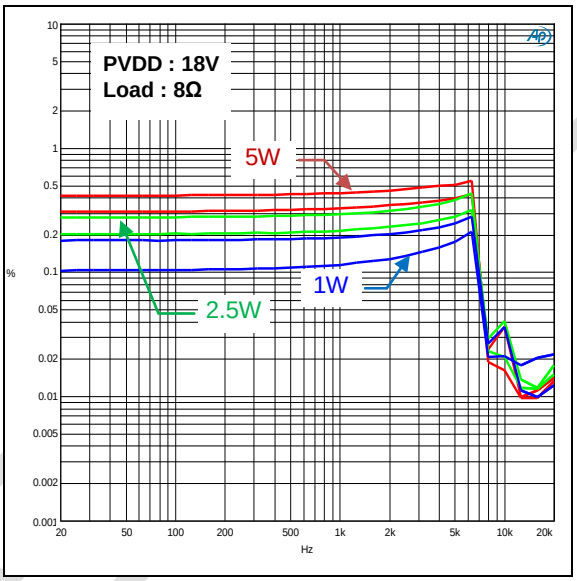


Total Harmonic Distortion + Noise vs. Frequency, BTL Configuration, 8Ω

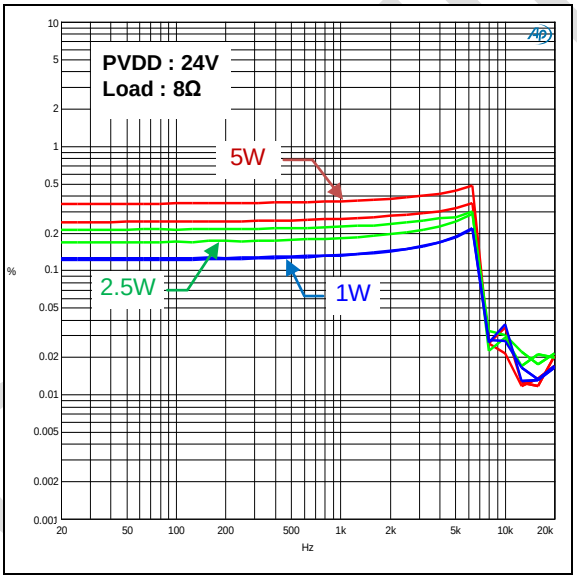
THD+N vs. Frequency



THD+N vs. Frequency

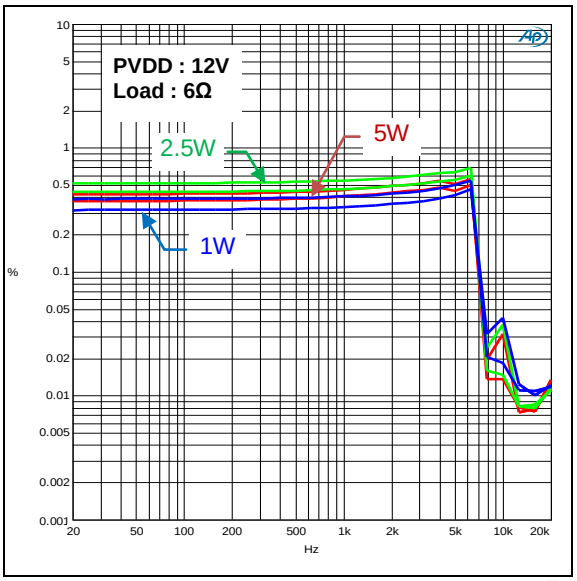


THD+N vs. Frequency

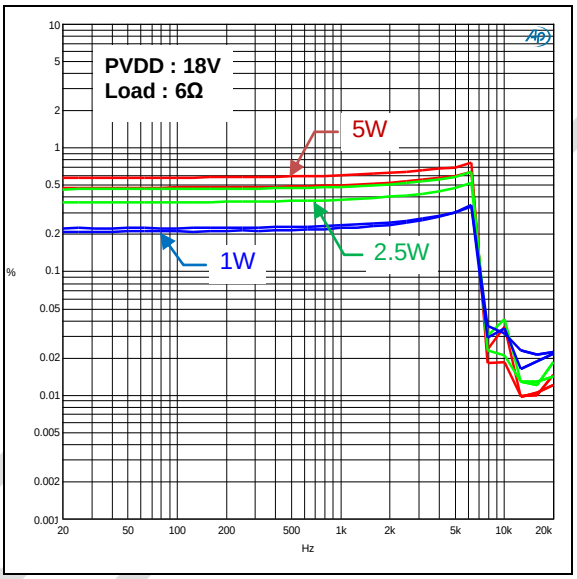


Total Harmonic Distortion + Noise vs. Frequency, BTL Configuration, 6Ω

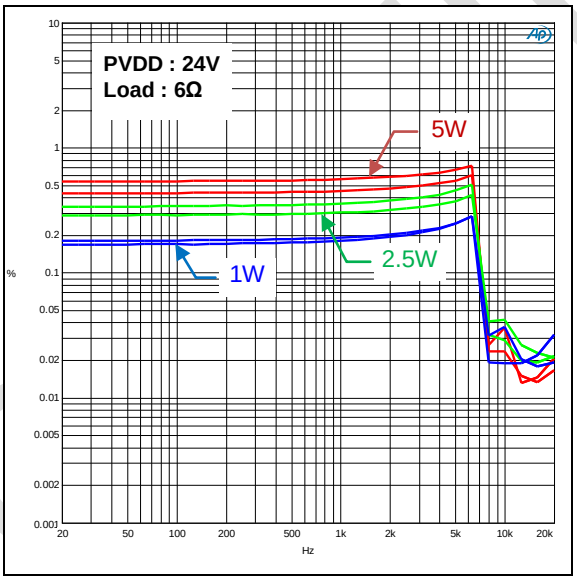
THD+N vs. Frequency



THD+N vs. Frequency

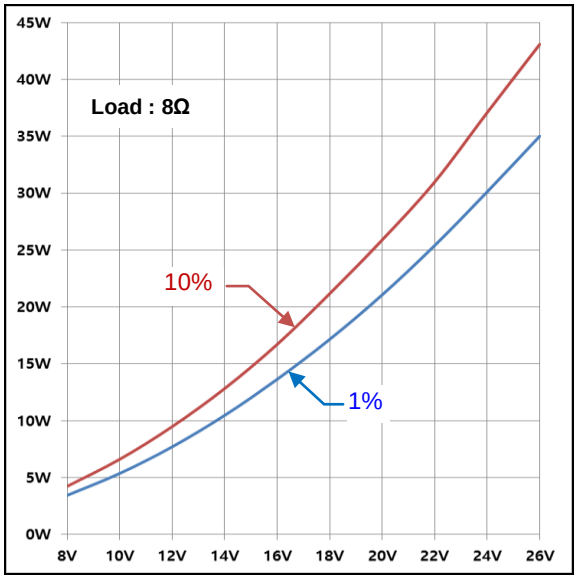


THD+N vs. Frequency

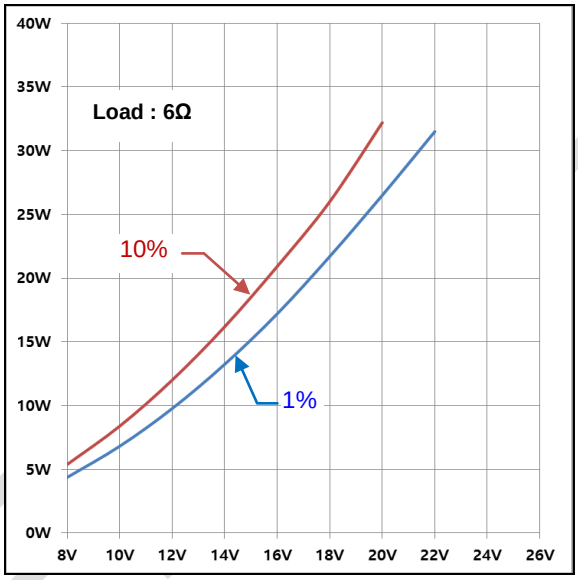


Output Power vs. PVDD, BTL Configuration

Output Power vs. PVDD

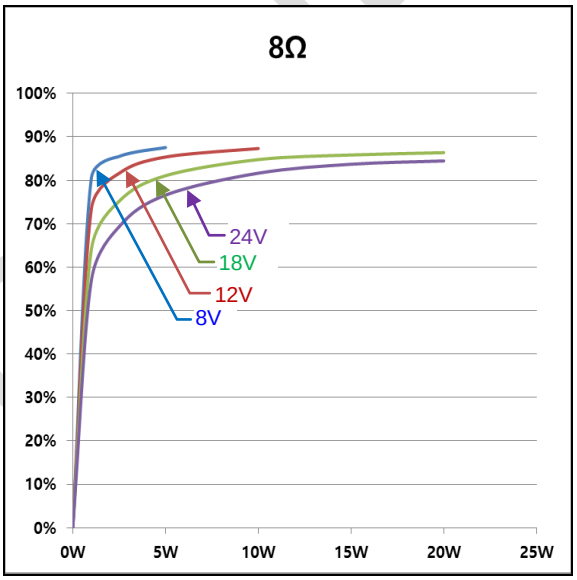


Output Power vs. PVDD

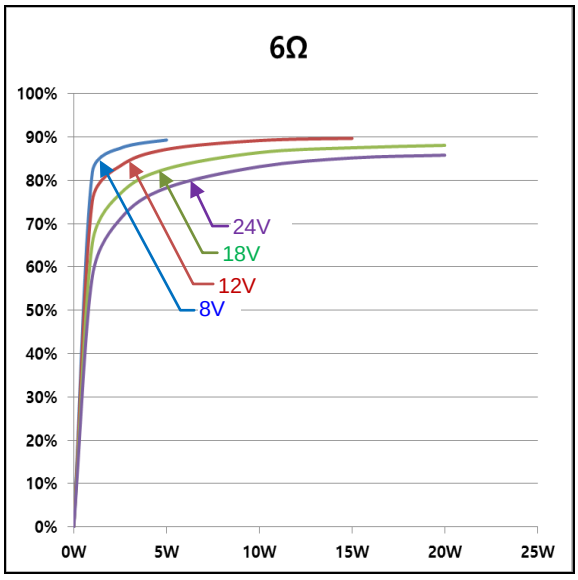


Efficiency vs. Total Power, BTL Configuration

Efficiency vs. Output Power

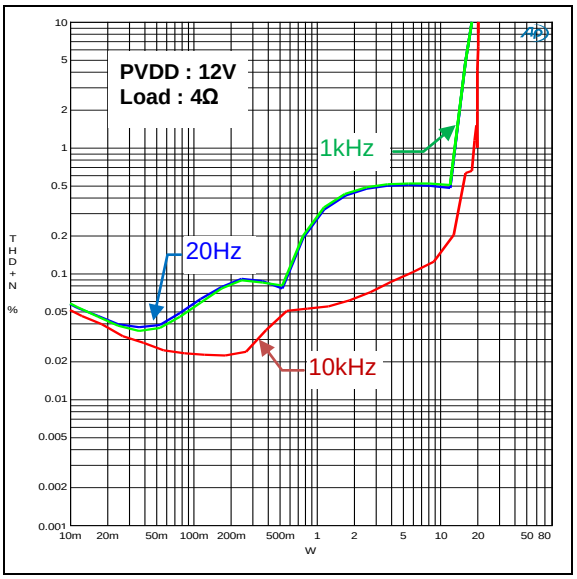


Efficiency vs. Output Power

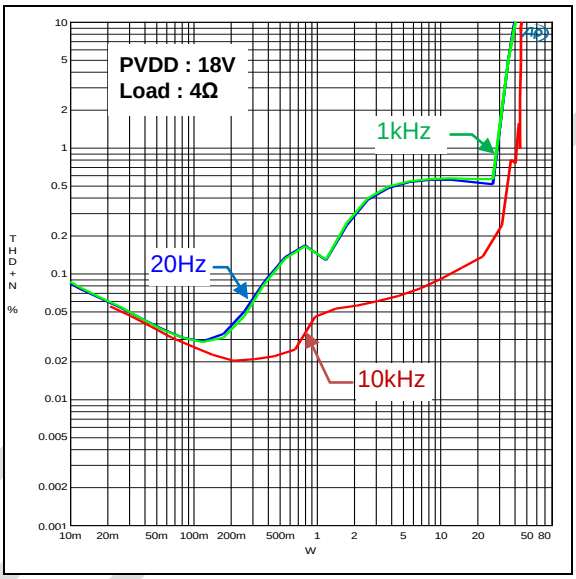


Total Harmonic Distortion + Noise vs. Power, PBTL Configuration, 4Ω

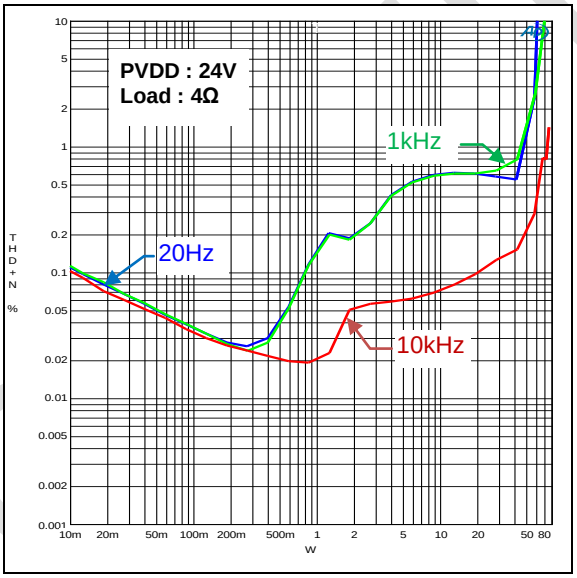
THD+N vs. Power



THD+N vs. Power

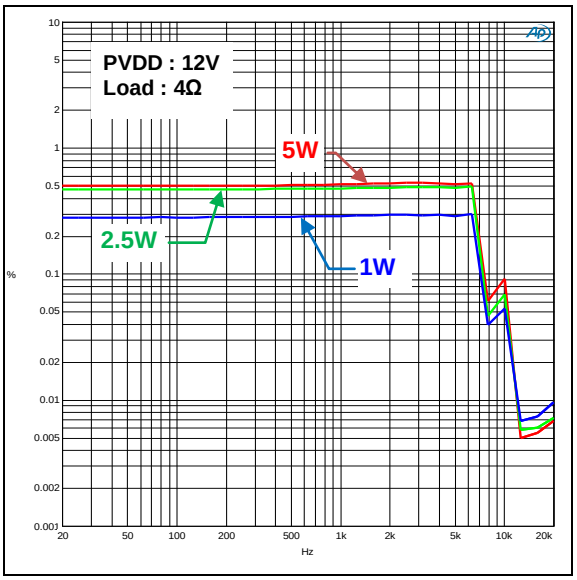


THD+N vs. Power

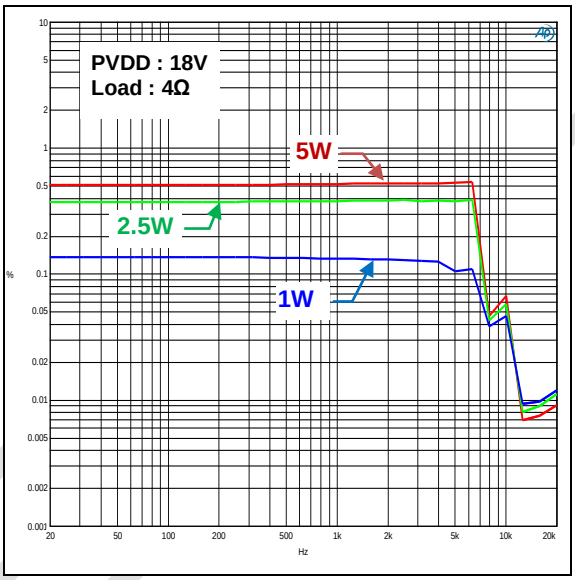


Total Harmonic Distortion + Noise vs. Frequency, PBTL Configuration, 4Ω

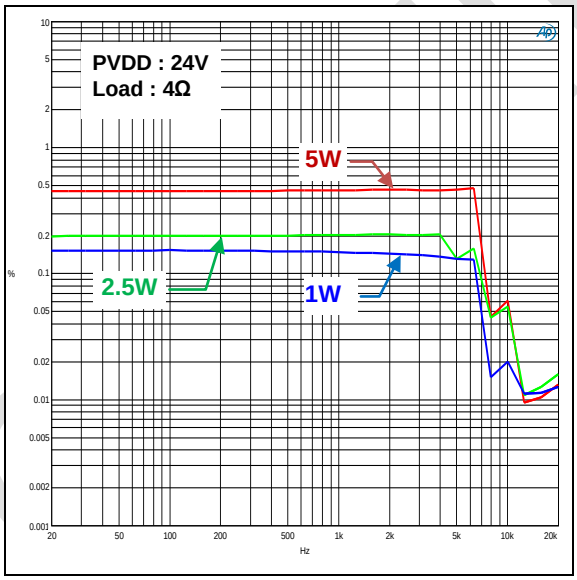
THD+N vs. Frequency



THD+N vs. Frequency

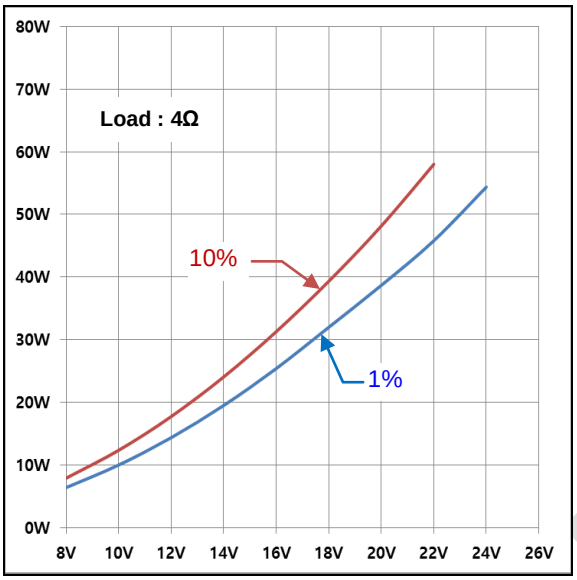


THD+N vs. Frequency



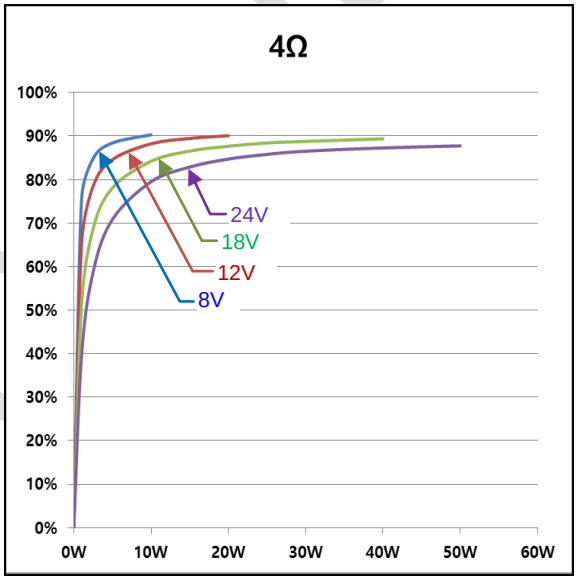
Output Power vs. PVDD, PBTL Configuration

Output Power vs. PVDD

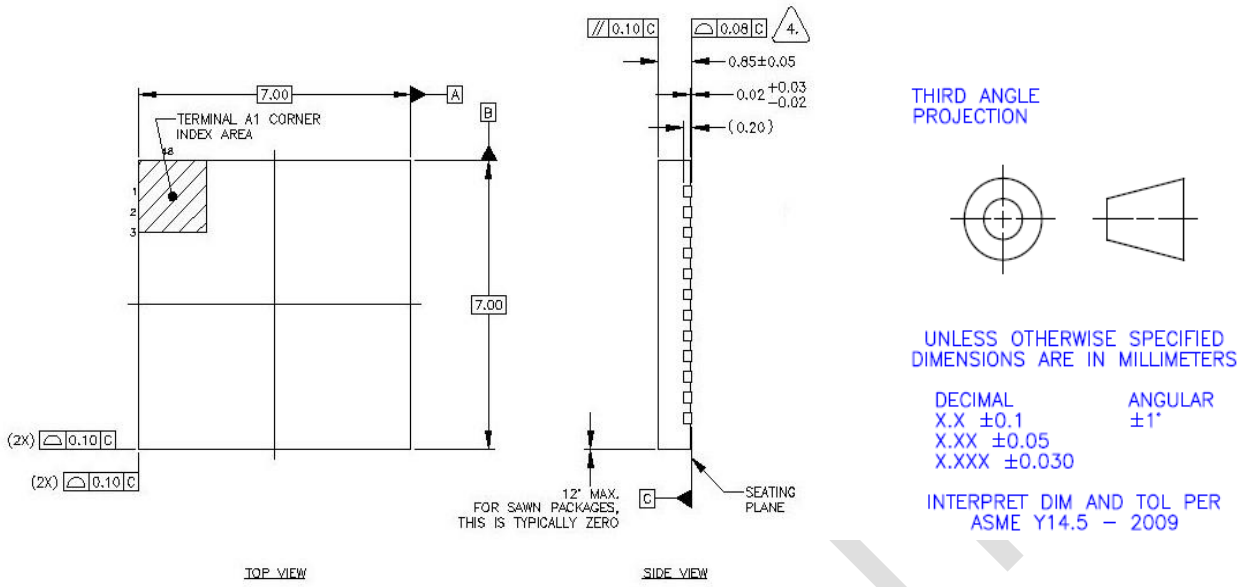


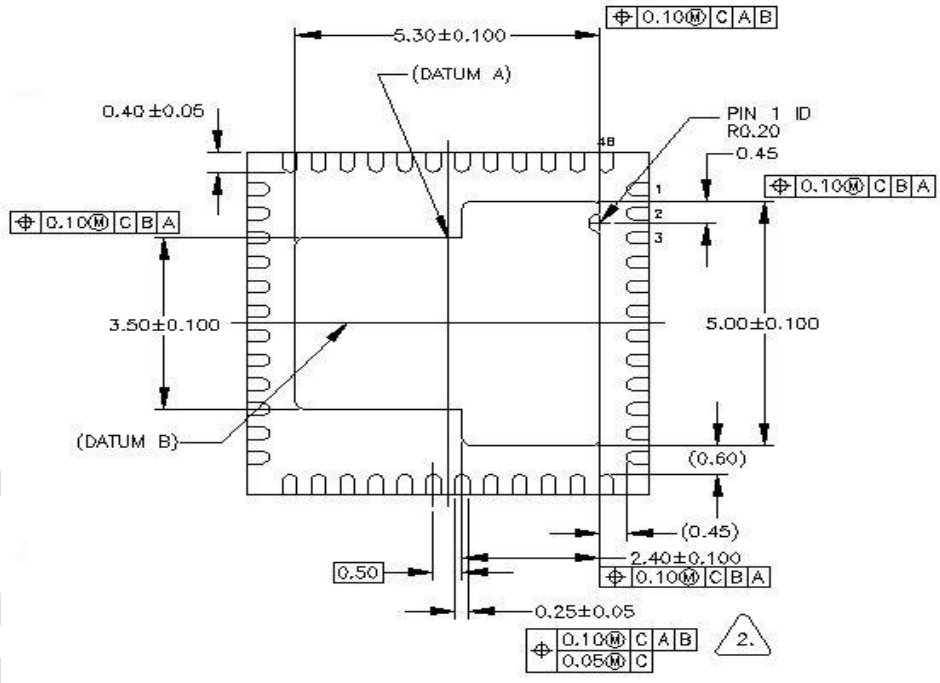
Efficiency vs. Total Power, PBTL Configuration

Efficiency vs. Output Power



E. Outline and Mechanical Data





4. UNILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

3. THE PIN #1 IDENTIFIER MUST EXIST ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTION MARK OR OTHER FEATURE OF PACKAGE BODY.

2. DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5 – 2009

NOTES: UNLESS OTHERWISE SPECIFIED